

# Proposed C2M AUI Loss Budget

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**Plenary Meeting**

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# List of Supporters

- Matt Brown – Alphawave**
- Jim Weaver – Arista**
- Arash Farhoodfar – Marvell**
- Mike Dudek – Marvell.**

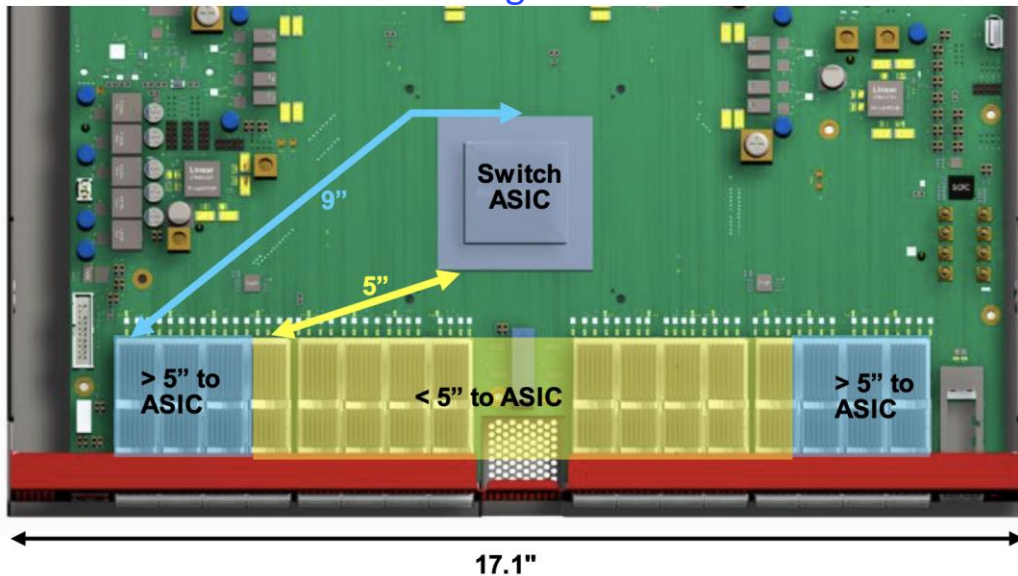
# Overview

- ❑ C2M reference application model
- ❑ Defining two host packages
- ❑ C2M hosts loss considering package A and B
- ❑ Bottom C2M loss with package A and B
- ❑ Increasing C2M loss doesn't come for free
- ❑ Proposed C2M loss budget
- ❑ Summary.

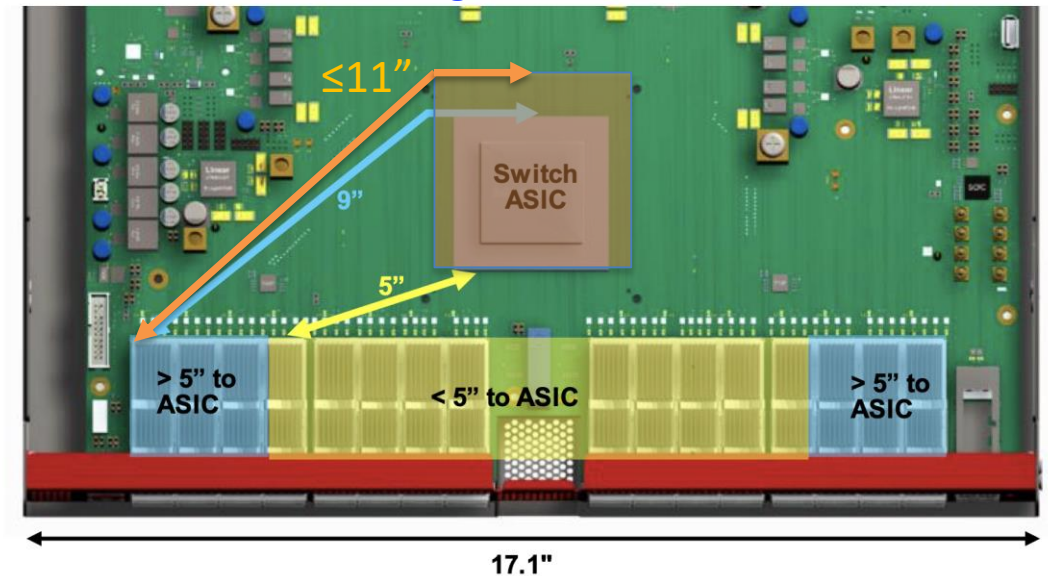
# Most Common Switch Implementation

- ❑ In 802.3ck max C2M PCB length assumed was 9" per recommendation [stone 3ck 01a 0518](#)
  - In CL120G max host PCB loss was 11.9 dB based on above recommendation for PCB with loss ~1.2 dB/in
  - [weaver 3dj elec 01 230831](#) C2M channel go up to 9" and was stated during Q&A the upper limit of <10"
    - Any application needing more than 10" has the option to use cabled host or retimers
  - PCB length 10 to 11" expect to cover most common 512 lanes switch implementations!

Stone Hypothetical 256 Lane Switch  
Package ~69x69



Hypothetical 512 lane (102T) Switch  
Package ~90x90



# DJ Host Package Type A and Type B

- **Class A package loss is 0.15 dB/mm @ 90 °C and Class B loss is 0.21 dB/mm @ 90 °C**
  - See [lim 3dj 02 2307](#) and the consensus presentation [lusted 3dj elec 01 230817](#)
  - [lusted 3dj 04 2309](#) assume 6 dB for class A package and 9.0 dB for class B, but this analysis assumes 6.75 dB loss for class A and 9.45 dB loss for class B based on 90 °C assumption

## Comparison of Key Design/Material Characteristics of “Class A” vs “Class B” PKGs

Package	“Class A”	“Class B”
ABF (Ajinomoto build-up film) material	GL107 Like	NA
Cross-section	8-2-8, or 10-2-10	6-2-6, to 9-2-9
Core thickness	~1000 μm	800-1200 μm
Trace routing lengths	33 mm max	30-40 mm max
Surface treatment	CZ8401 Like	NA
BGA ball pitch	0.8 mm	> 1.0 mm
Skip Layer	Yes (x%)	No
Trace line / space	~30 / 60 / 30 μm	27-45-27 μm
Trace line / space (Skip Layer)	~80 / 80 / 80 μm	NA
Impedance	~87.5 ohms	90-92 ohms
ABF height	35 μm	40 μm

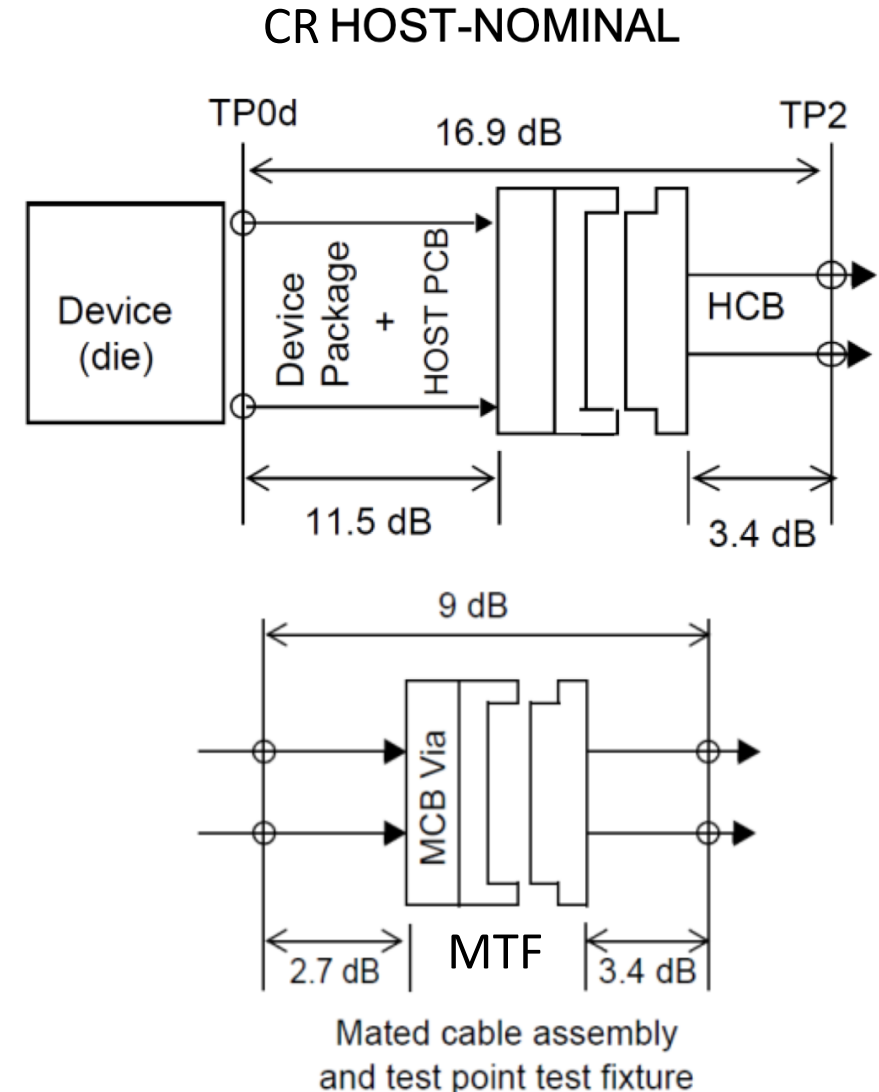
Package Trace	Class A Loss (dB)	Class B Loss (dB)
15 mm	2.25	3.15
30 mm	4.5	6.3
45 mm	6.75	9.45

# HCB and MCB Losses

## ❑ Motion #5 during September 2023 Interim

- Move to adopt the the CR host and cable assembly insertion loss budget proposed in [diminico 3dj 01a 2309](#), slide 7 for the symmetrical CR use case
- Slide 7 defines the CR channel loss and allocates 3.4 dB to the HCB loss as shown here

## ❑ Next will construct the C2M channel with addition of test points based on adopted HCB loss and proposed [diminico 3dj 01 2311](#) MCB loss of 2.7 dB.



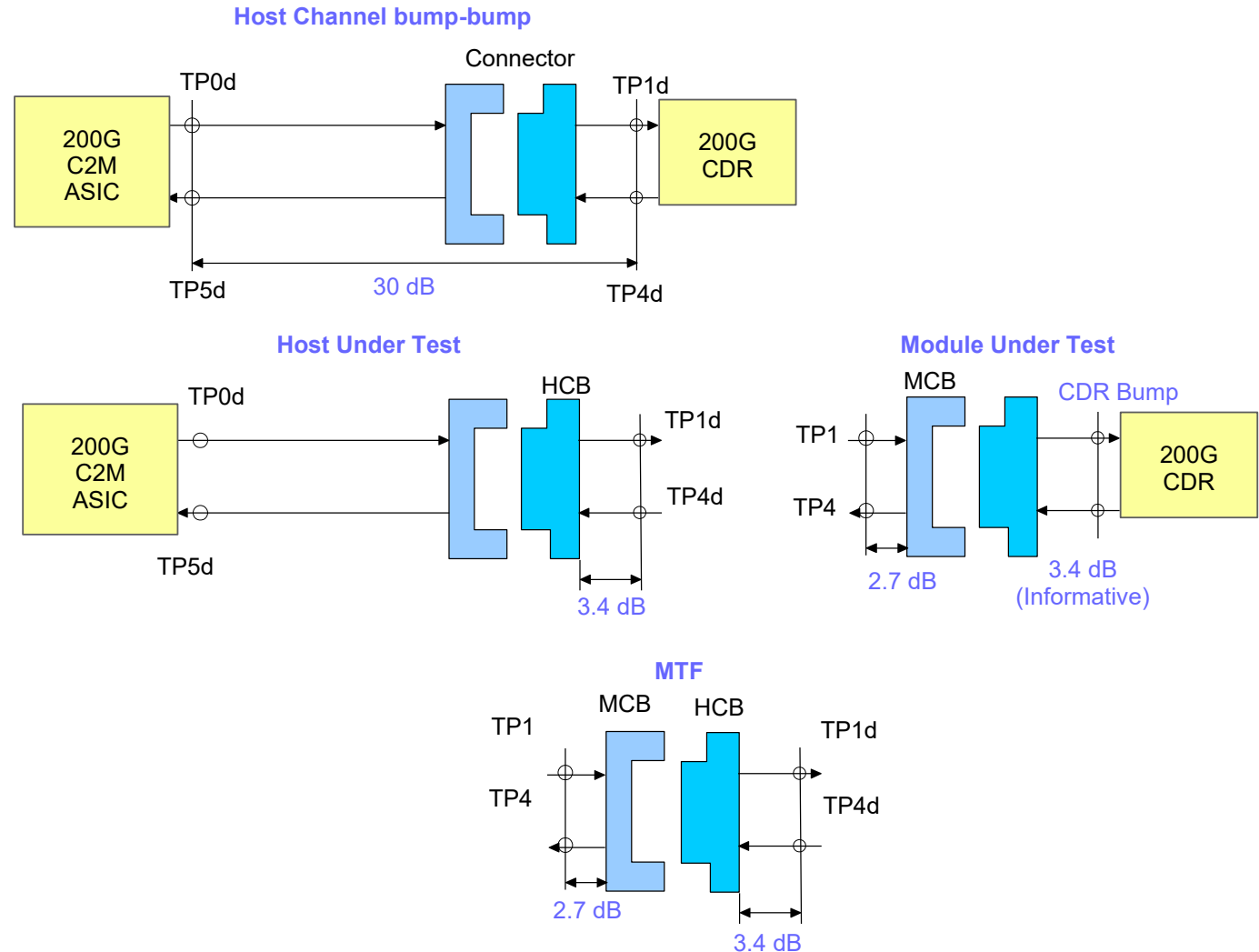
# Summary of AUI C2M Test Points and Losses

## 200G CDR/DSPs dies are mounted directly on the module plug HDI board without BGA package

- The end of HCB CR test point TP2 is also the AUI test point TP1d/TP4d for compliance
- Proposal is to make the module plug board loss equal to HCB loss (3.4 dB)
- HCB loss being equal to plug board would be an ideal test point for measurement at the CDR/DSP bump TP1d/TP4d

## Measurement at TP1d/TP4d with HCB will have the correct loss but will not include DC block pads/via transition degradation

- Need to allocate some margin for DC blocks in COM (0.25-0.5 dB?)/VEC.



# DC Blocks Loss in the Module

- ❑ **Does 3.4 dB HCB/module plug loss sufficient to support a short module PCB and DC blocks?**
- ❑ **Following companies have ultra-broadband DC blocks with following loss property that may be suitable for optical module DC blocks**
  - Vendor A offer RF/Microwave ceramic 0.1  $\mu\text{F}$  in 0201 size with loss of <0.6 dB up to 60 GHz
  - Vendor B offers silicon 0.047  $\mu\text{F}$  in 0201 with loss of 0.3 dB up to 60 GHz
  - Vendor C offer ceramic 0.1  $\mu\text{F}$  in 0201 and 0402 size with loss of <0.5 dB up to 50 GHz
- ❑ **Capacitors suppliers above offer specialized broadband DC blocks for optical modules**
  - Based on the above 3 suppliers offering DC blocks estimated loss for 802.3dj PMDs is < 0.6 dB up to Nyquist frequency
  - Some of the capacitors offered operate up to 110 GHz
  - Increasing low frequency corner frequency above 50 kHz (require 0.1  $\mu\text{F}$ ) increases supply option and may allow using smaller capacitor sizes.



# AUI Bottom-Up Analysis with Package Class A and B

□ Updated bottom-up analysis include PKG A (0.15 dB/mm) with updated package type B loss (0.195 dB/mm) per [benartsi 3dj 01 2311](#)

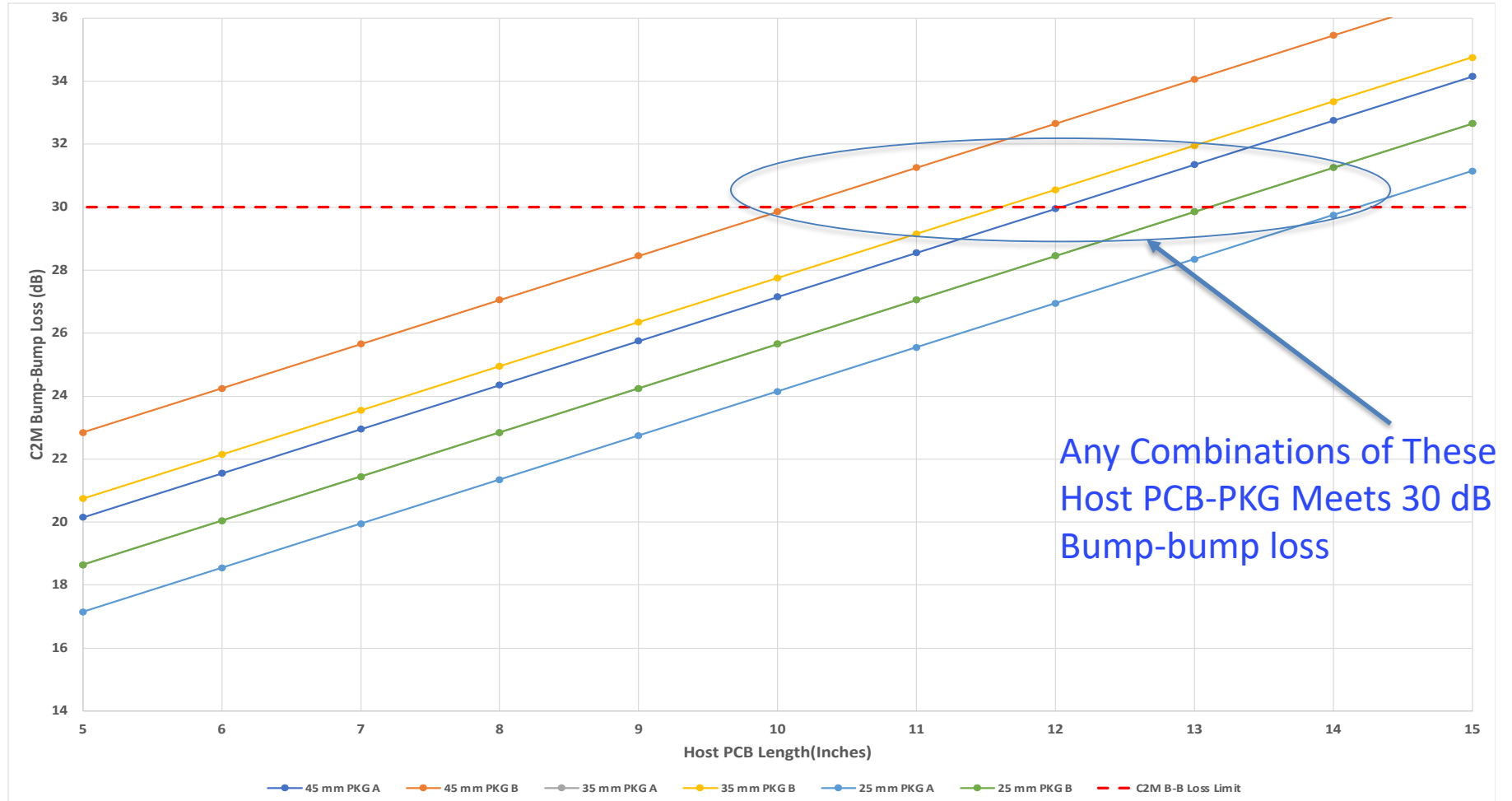
- Previously extracted package type B loss was 0.21 dB/mm
- 1 dB excess via loss is added on top of [weaver 3dj elec 01 230831](#) 1.4 dB/in channel loss @80 °C for > 3 mm vias
- With 30 dB bump-bump loss PKG A support 12" of PCB and PKG B supports 10.6" of PCB
- Proposed common AUI application for all front pluggable TP0b-TP1b loss ≤30 dB.

Loss Parameters @ 53 GHz A. Ghiasi - Rev 1.4 11/7/2023	Host1 with PKG A	Host2 with PKG B	Length or # PKG A	Length or # PKG B	AUI Conventional PCB PKG A	AUI Conventional PCB PKG B	AUI Cabled Host PKG A	AUI Cabled Host PKG B
Host PCB Loss (dB/in)	1.4	1.4	12	10.6	16.8	14.84	NA	NA
Cabled Host PCB Loss (dB/in)	1.4	1.4	2	2	NA	NA	2.8	2.8
Cable Loss (dB/in)	0.3		18	18	NA	NA	5.4	5.4
Plug Board/PIC/HCB Loss (dB/in)	1.55	1.55	2.2	2.2	3.41	3.41	3.41	3.41
AUI Connector Loss (dB)	2	2	NA	NA	2	2	2	2
Excess Host Via Loss (dB)	1	1	NA	NA	1	1	1	1
Host Package Loss (dB/mm)	0.15	0.195	45	45				
Host PKG Mode Con. Loss (dB)	0	0	NA	NA				
CDR Package Loss (dB/mm)	0	0	10	10				
CDR PKG Mode Con. Loss (dB)	0	0	NA	NA				
Total Host PKG Loss (dB)					6.75	8.775	6.75	8.775
Total CDR PKG Loss (dB)					0	0	0	0
TGA Connector Loss (dB)	0.3	0.3	NA	NA	NA	NA	0.3	0.3
Socket Loss (dB)	0.2	0.2	NA	NA	NA	NA	0.2	0.2
TP0-TP1a Loss (dB)	NA	NA	NA	NA	23.21	21.25	15.11	15.11
Bump-TP1a* (dB)	NA	NA	NA	NA	29.96	30.025	21.86	23.885
Bump-Bump Loss (dB)	NA	NA	NA	NA	29.96	30.025	21.86	23.885

\* TP1a=TP1d since there is no CDR package.

# AUI C2M at 30 dB Bump-Bump Loss has Greater Reach than CL120G

- AUI C2M at 30 dB on 45 mm package supports ~12.0" with PKG A and ~10.6" with PKG B
  - With modest care avoiding to connect longest PCB and package trace 12+ inches is feasible !



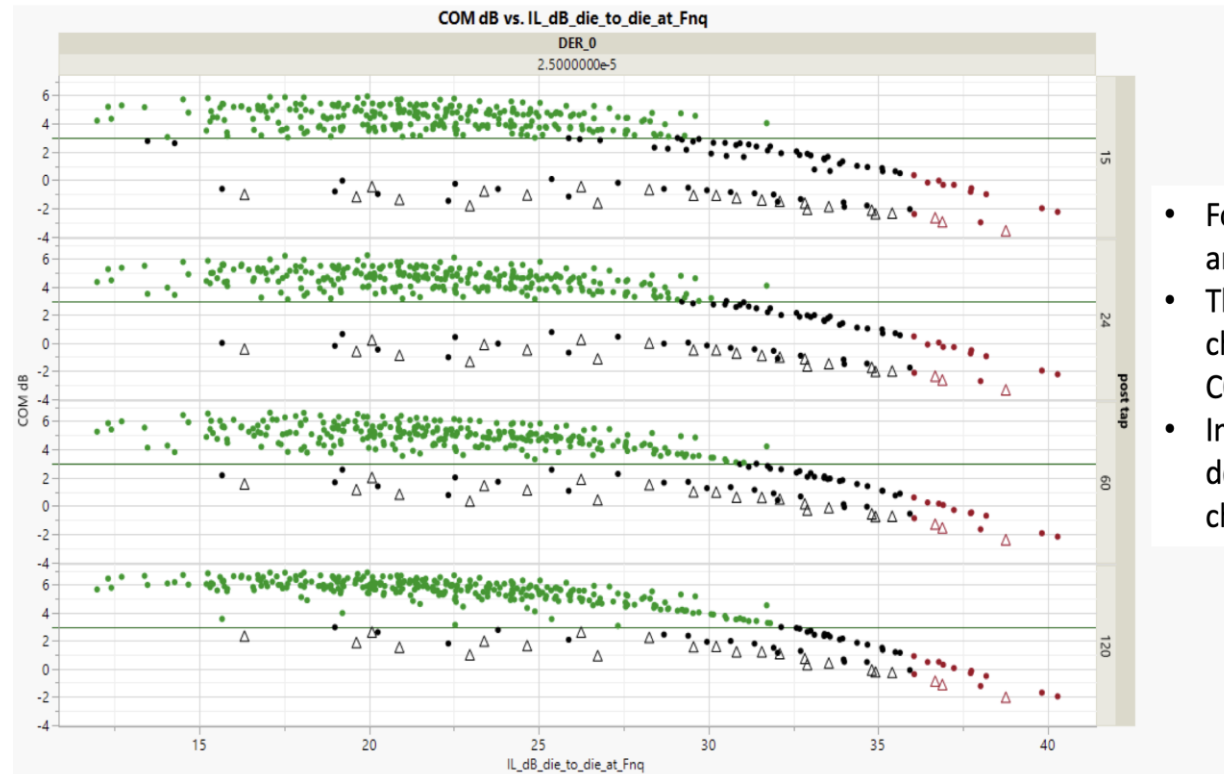
# Unless the 100G Channels Improve the 200G AUI Link Would be Too Power Hungary!

## □ [mellitz 3dj elec 01 231026](#)

### COM analysis indicates

- Steep penalty beyond 30 dB bump to bump loss with COM failing
- At 30 dB the AUI equalizer can be 24-30 taps FFE+1T DFE
- Pushing the loss to 32-36 dB would require 60-120 taps FFE+1T DFE and MLSE
- For number of [kareti 3dj 01 2309](#) channels (black open triangle) there is no conventional equalizer solution unless these channels improve
  - [kareti 3dj 01 2309](#) channels up to 30 GHz have much higher ILD compared to [lim 3ck 02 0719](#) 100G channel!

COM Results for 15, 24, 60, and 120 taps FFE + 1T DFE

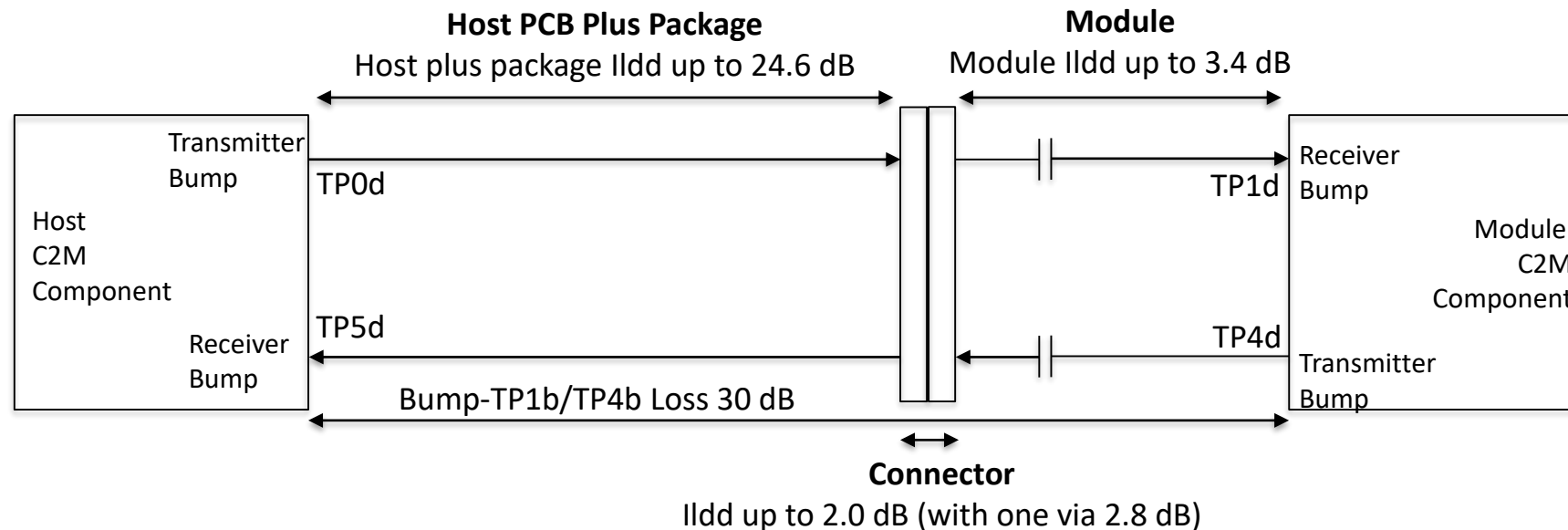


- For this set of data, DER=2.5e-5 and  $\eta_0=1.25e-8 \text{ V}^2/\text{GHz}$
- The takeaway is that a lot of channels comfortably exceed 3 dB COM with 24 taps or less
- Increasing number of taps to 120 doesn't make 33 to 36dB loss channels pass

# AUI C2M Application Reference Model

## □ AUI C2M total loss for DJ proposed to be from TP0b(bump) -TP1a

- Recommend to use TP0d for host ASIC Tx bump and TP1b for HCB output test point
- Recommend to use TP5d for host ASIC Rx bump and TP4b for HCB input test point
- Max TP0-TP1d (TP4d-TP5) including two vias  $\leq 23.25$  dB (package A) and  $\leq 21.25$  dB (package B)
  - CL120G 100G-AUI equivalent loss defined to be  $\leq 16$  dB
- C2M max bump-bump TP0d -TP1d (TP4d-TP5d) loss  $\leq 30$  dB at 53.125 GHz.



# Summary

- ❑ **Proposed AUI C2M with max bump-bump loss of 30 dB on 45 mm package trace supports 12” of PCB with PKG A and 10.6” with PKG B assuming worst PCB-PKG pair combination**
  - At 30 dB bump-bump the DJ C2M AUI will provide greater PCB length than CK CL 120G
  - AUI C2M at 30 allow increasing PCB traces beyond 12” with modest pairing of PKG traces with PCB traces
  - Assumed package type A loss is 6.75 dB and for Type B 8.75 dB [lusted 3dj 04 2309](#) assume (6 dB for Type A and 9 dB for Type B)
- ❑ **Proposed AUI C2M to have max bump-bump loss of  $\leq 30$  dB**
  - Informative C2M loss specifications from TP0d-TP1d and TP4d-TP5d with a loss of  $\leq 30$  dB
- ❑ **Pushing the C2M AUI loss to 36 dB with about an order of magnitude lower BER than KR then for all practical purpose the C2M SerDes technology is the same as 40 dB KR**
  - [mellitz 3dj elec 01 231026](#) data show that there is no solution for many of the 32-36 dB channels
- ❑ **Back up slide show 32 dB budget extending host PCB to 12” with package B (8.75 dB) so there is no reason to go beyond 32 dB!**

# AUI Bottom-Up Analysis with Package Class A and B (Back up)

## □ Based on 32 dB channel assuming CDR die direct attach to HDI board

- 1 dB excess via loss is added on top of [weaver 3dj elec 01 230831](#) 1.4 dB/in channel loss @80 °C for > 3 mm vias
- With 32 dB bump-bump loss PKG A support 13.5” of PCB and PKG B supports 12” of PCB
- 32 dB loss budget supports 12” of host PCB over worst case package B (45 mm @ high temp) so there is no justification to push the loss to 36 dB!

Loss Parameters @ 53 GHz A. Ghiasi - Rev 1.4 11/7/2023	Host1 with PKG A	Host2 with PKG B	Length or # PKG A	Length or # PKG B	AUI Conventional PCB PKG A	AUI Conventional PCB PKG B	AUI Cabled Host PKG A	AUI Cabled Host PKG B
Host PCB Loss (dB/in)	1.4	1.4	13.5	12	18.9	16.8	NA	NA
Cabled Host PCB Loss (dB/in)	1.4	1.4	2	2	NA	NA	2.8	2.8
Cable Loss (dB/in)	0.3		18	18	NA	NA	5.4	5.4
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AUI Connector Loss (dB)	2	2	NA	NA	2	2	2	2
Excess Host Via Loss (dB)	1	1	NA	NA	1	1	1	1
Host Package Loss (dB/mm)	0.15	0.195	45	45				
Host PKG Mode Con. Loss (dB)	0	0	NA	NA				
CDR Package Loss (dB/mm)	0	0	10	10				
CDR PKG Mode Con. Loss (dB)	0	0	NA	NA				
Total Host PKG Loss (dB)					6.75	8.775	6.75	8.775
Total CDR PKG Loss (dB)					0	0	0	0
TGA Connector Loss (dB)	0.3	0.3	NA	NA	NA	NA	0.3	0.3
Socket Loss (dB)	0.2	0.2	NA	NA	NA	NA	0.2	0.2
TP0-TP1a Loss (dB)	NA	NA	NA	NA	25.31	23.21	15.11	15.11
Bump-TP1a* (dB)	NA	NA	NA	NA	32.06	31.985	21.86	23.885
Bump-Bump Loss (dB)	NA	NA	NA	NA	32.06	31.985	21.86	23.885

\* TP1a=TP1d since there is no CDR package.