DER_0 for 200 Gb/s per lane backplane and copper cable PHYs

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Introduction

- DER_0 is the target detector error ratio used for the calculation of Channel Operating Margin (COM)
- It should correspond to the performance required for the link to meet the Frame Loss Ratio (FLR) requirement
- This presentation seeks to justify a choice of DER_0 for 200 Gb/s per lane backplane and copper cable PHYs

An important question

- DER_0 = 1e−4 has commonly been used to calculate COM for 200 Gb/s per lane backplane and copper cable PHYs
- The same value has been used for prior generations of these PHYs

- However, the multiplexing scheme for a 200 Gb/s lane is different from what was used in prior generations
- The changes are expected to have a positive impact on performance
- In addition, the relationship between DER_0 and the PAM-4 symbol error ratio has recently been clarified (see kirkland_3dj_elec_01_230406)

- Considering these developments, what value of DER_0 is appropriate for these new PHYs?

First, some terminology...

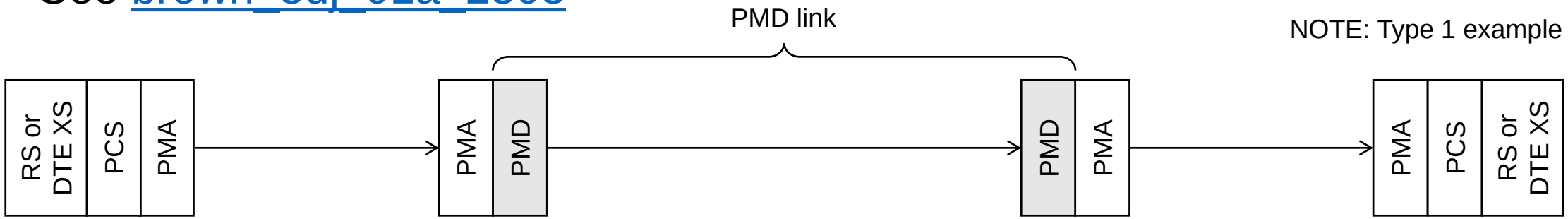
Symbol	Description
DER	Detector error ratio
DER_0	Target detector error ratio
SER_1	Probability of a PAM-4 symbol error event i.e., the initial error in an error burst
SNR	Signal-to-noise ratio corresponding to SER_1 (or BER_1)
a	Probability of PAM-4 symbol error given an error in previous symbol
SER	PAM-4 symbol error ratio that would be observed in a measurement
BER_1	Probability of a bit error event i.e., the initial error in a burst
BER	Bit error ratio that would be observed in the measurement

Relationship between terms for PAM-4

$SER_1 = 1.5\ DER$	See back-up for detailed explanation
$SER_1 = \frac{3}{4}\ \mathrm{erfc}\left(\sqrt{\frac{SNR}{10}}\right)$	Normalize SNR to PAM-4 signal power (5)
$SER = SER_1 / (1 - a)$	Average length of a burst is $1 / (1 - a)$, $0 \leq a \leq 0.75$
$SER = 2\ SER_1$	When precoding is used (regardless of a)
$BER_1 = SER_1 / 2 = 0.75\ DER$	Gray mapping, 1 bit error per PAM-4 symbol error
$BER = SER / 2 = BER_1 / (1 - a)$	Average BER as measured by an error checker
$BER = SER = 2\ BER_1$	When precoding is used

More terminology

- See brown_3dj_01a_2303

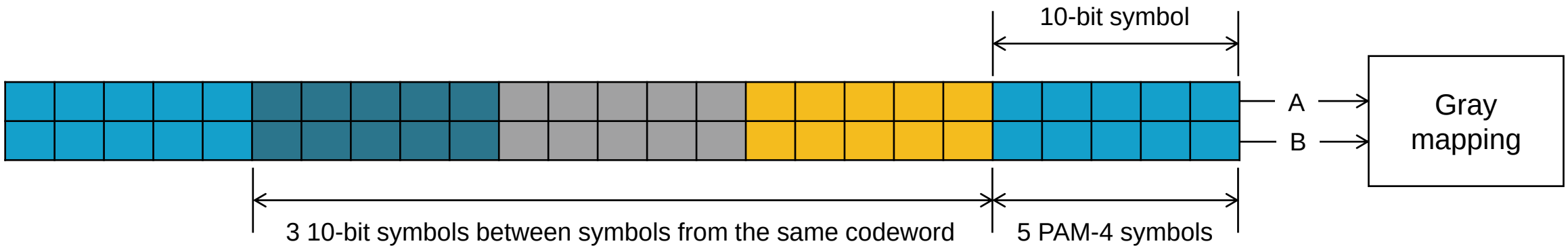


PHY type	Forward Error Correction (FEC) approach
1	Single code spans one or more Attachment Unit Interfaces (AUI) and the PMD link
2	Outer code spans one or more AUIs and the PMD link Inner code provides additional protection for the PMD link
3	Single code dedicated to the PMD link (no AUIs, but extenders may still be used)

- Backplane and copper cable PHYs may not be Type 2 (refer to May 2023 motion #6)
- However, it was not decided whether they are Type 1 or Type 3

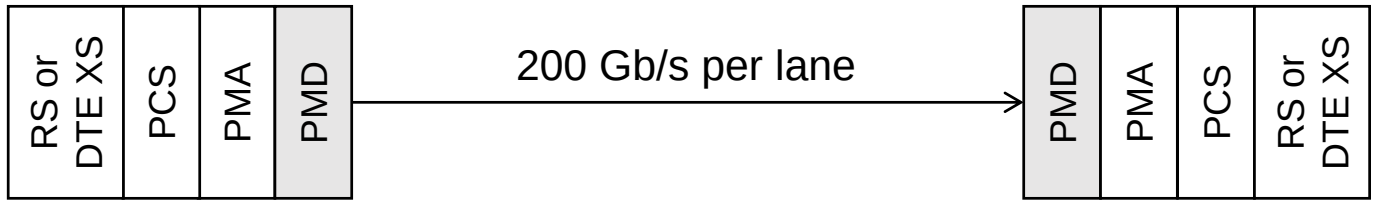
Multiplexing scheme for 200 Gb/s lanes

- Baseline proposals ran_3dj_01a_2303 and he_3dj_02a_2307 result in the following multiplexing pattern on each 200 Gb/s PMD and AUI lane



- This is referred to as “CI4+SM” on subsequent slides

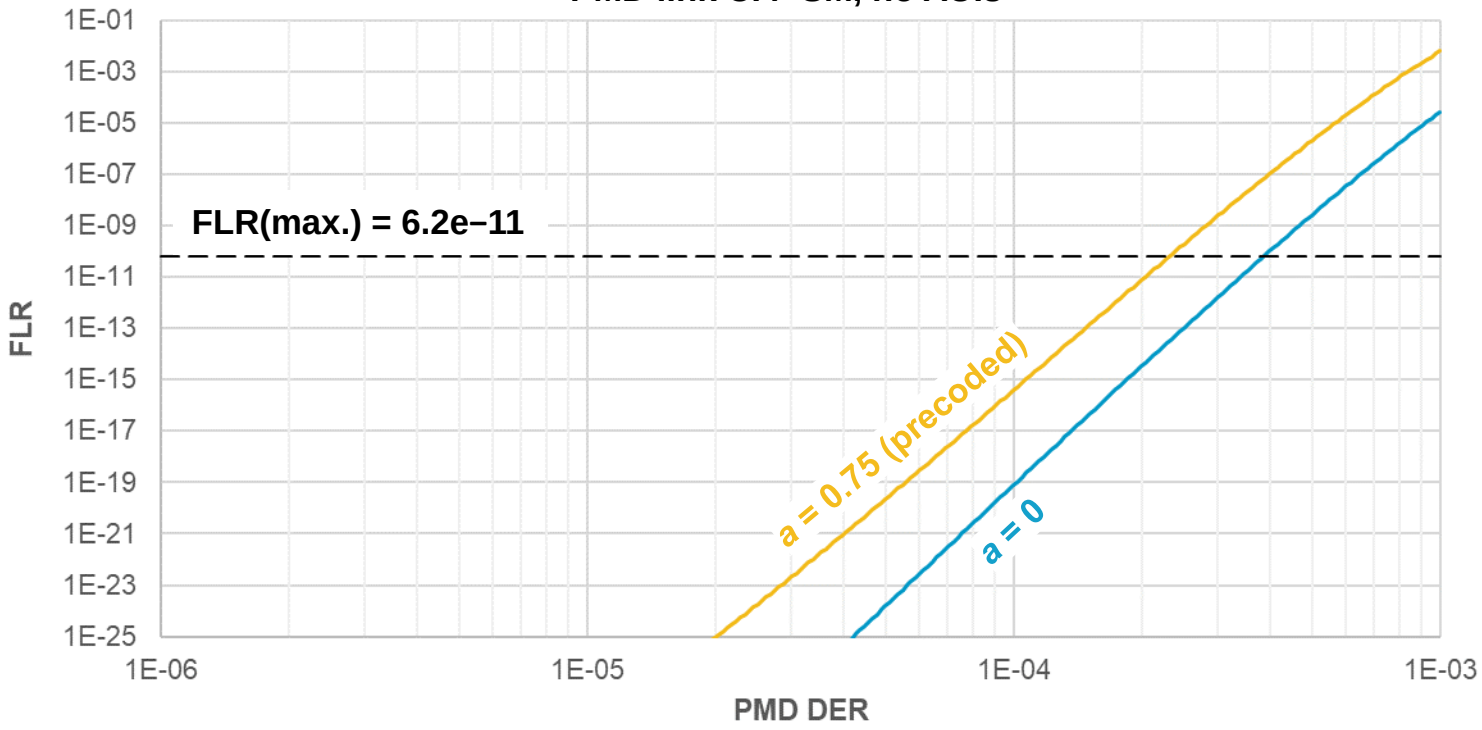
PMD link DER_0 when there are no AUIs



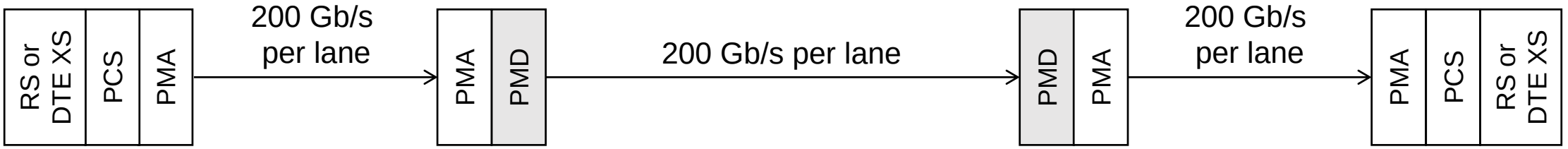
PMD link CI4+SM, no AUIs

a	0	0.75 (precoded)
DER_0	3.8e−4	2.3e−4
BER_1	2.8e−4	1.7e−4
SNR, dB	17.5	17.8

PMD link CI4+SM, no AUIs

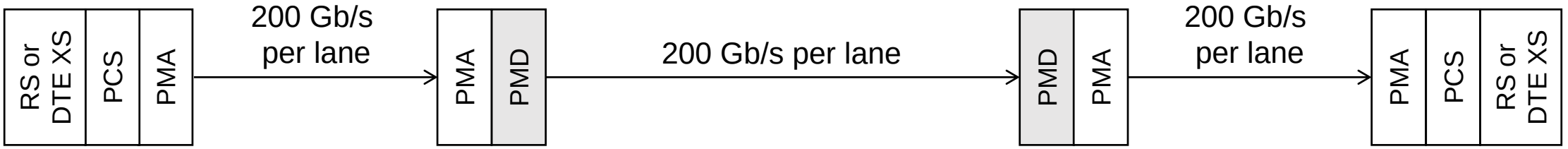


Add 200 Gb/s per lane AUI chip-to-chip (C2C)



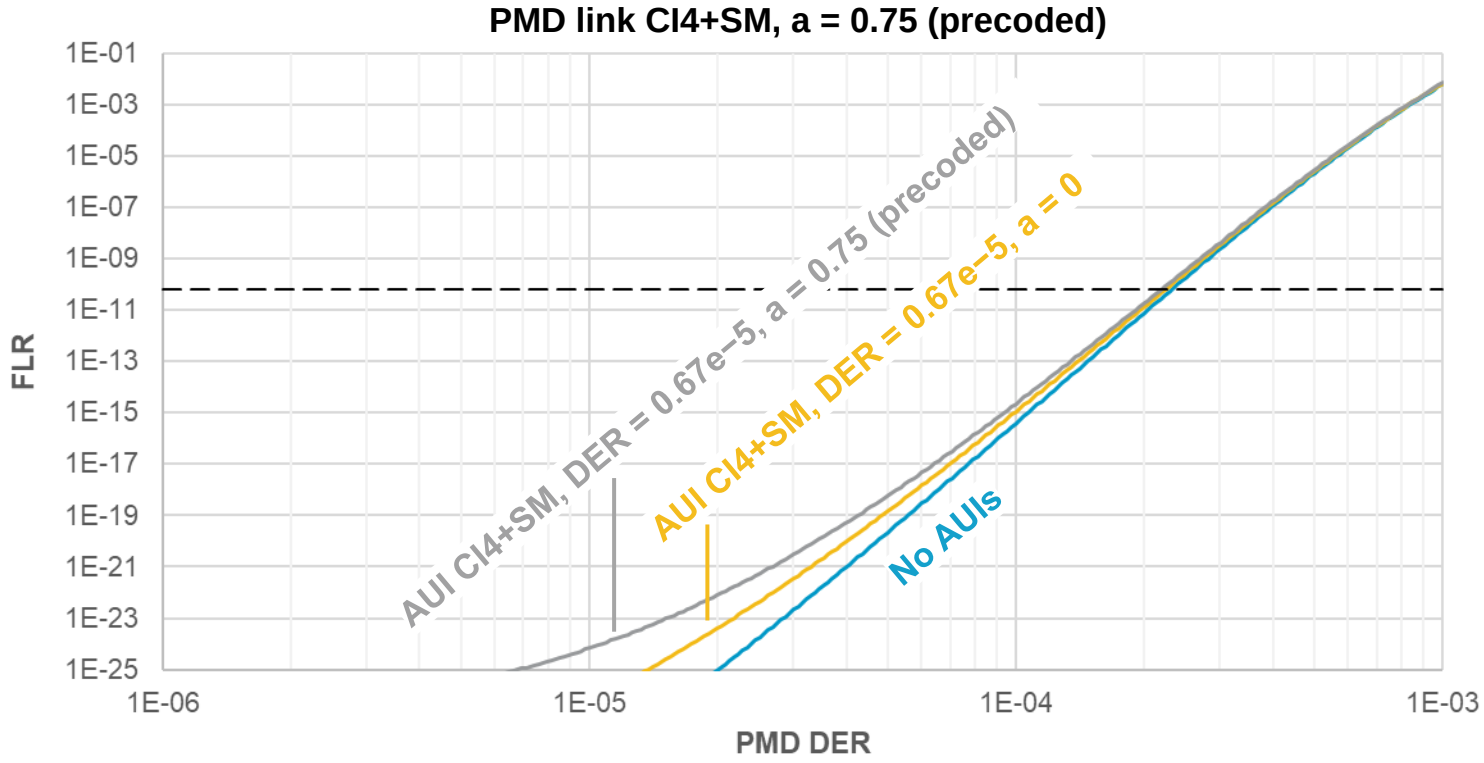
- Assume each PHY may optionally include one AUI C2C
- DER_0 for 200 Gb/s per lane AUI C2C was set to 0.67e−5 when the PHY also includes an AUI C2M (chip-to-module) (21 September 2023 motion #1)
- In this application, AUI C2M is not applicable but it is assumed that DER_0 for AUI C2C is unchanged

PMD link DER_0 with 200 Gb/s per lane AUIs

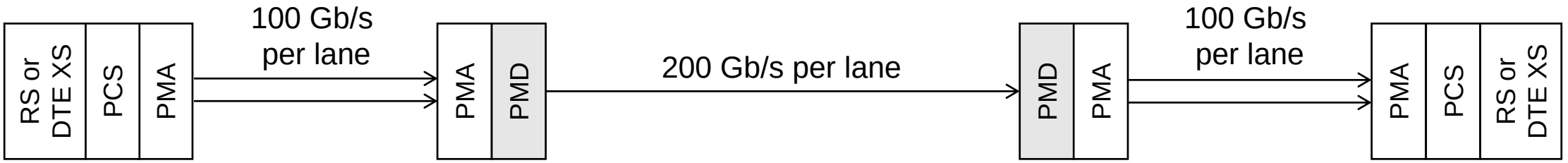


PMD link CI4+SM, a = 0.75 (precoded)
AUI CI4+SM, DER = 0.67e−5

AUI a	0	0.75 (precoded)
DER_0	2.2e−4	2.1e−4
BER_1	1.6e−4	1.5e−4
SNR, dB	17.9	17.9



What about 100 Gb/s per lane AUI C2C?

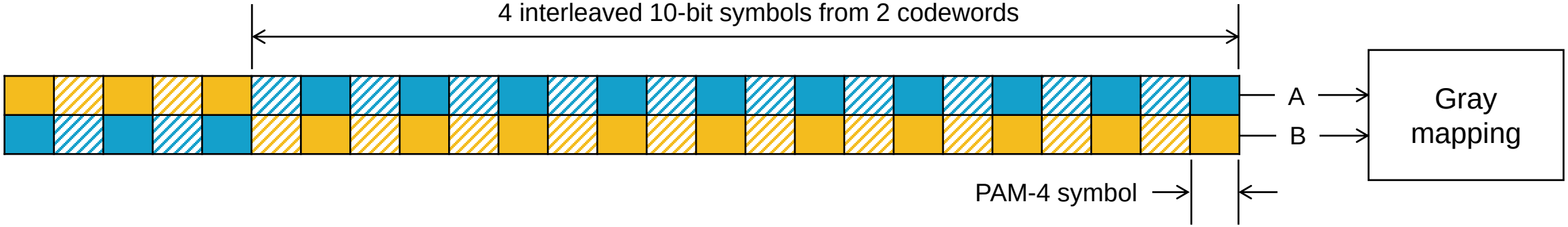


- Refer to IEEE Std 802.3ck-2022 Annex 120F
- Per Table 120F−8, DER_0 is 1e−5 (corresponding to BER_1 = 0.75e−5)
- Per Table 120F−5, a receiver lane is required to achieve a FEC symbol error ratio no greater than 1e−4
- However, the FEC symbol error ratio definition appears to be incorrect (see back-up)
- 120F.3.2.4 i) suggests BER = 1e−5 is acceptable

  [...] it is permissible to use the PRBS31Q pattern as described in 120.5.11.2.2 and bit error ratio testing. In this case the required bit error ratio is equal to the required FEC symbol error ratio divided by 10.

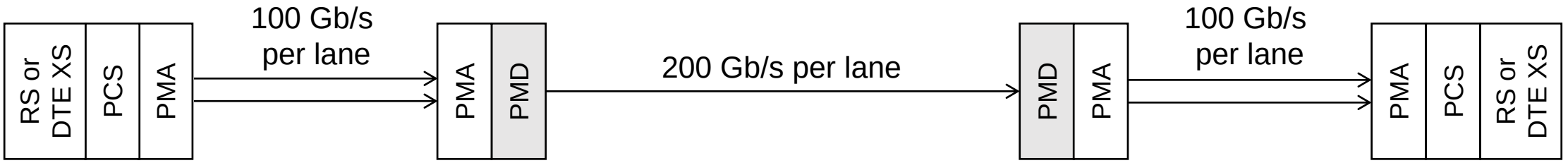
Assessing the impact of 100 Gb/s per lane AUIs

- The following multiplexing pattern would appear on the AUI for 200 and 400 Gb/s Ethernet

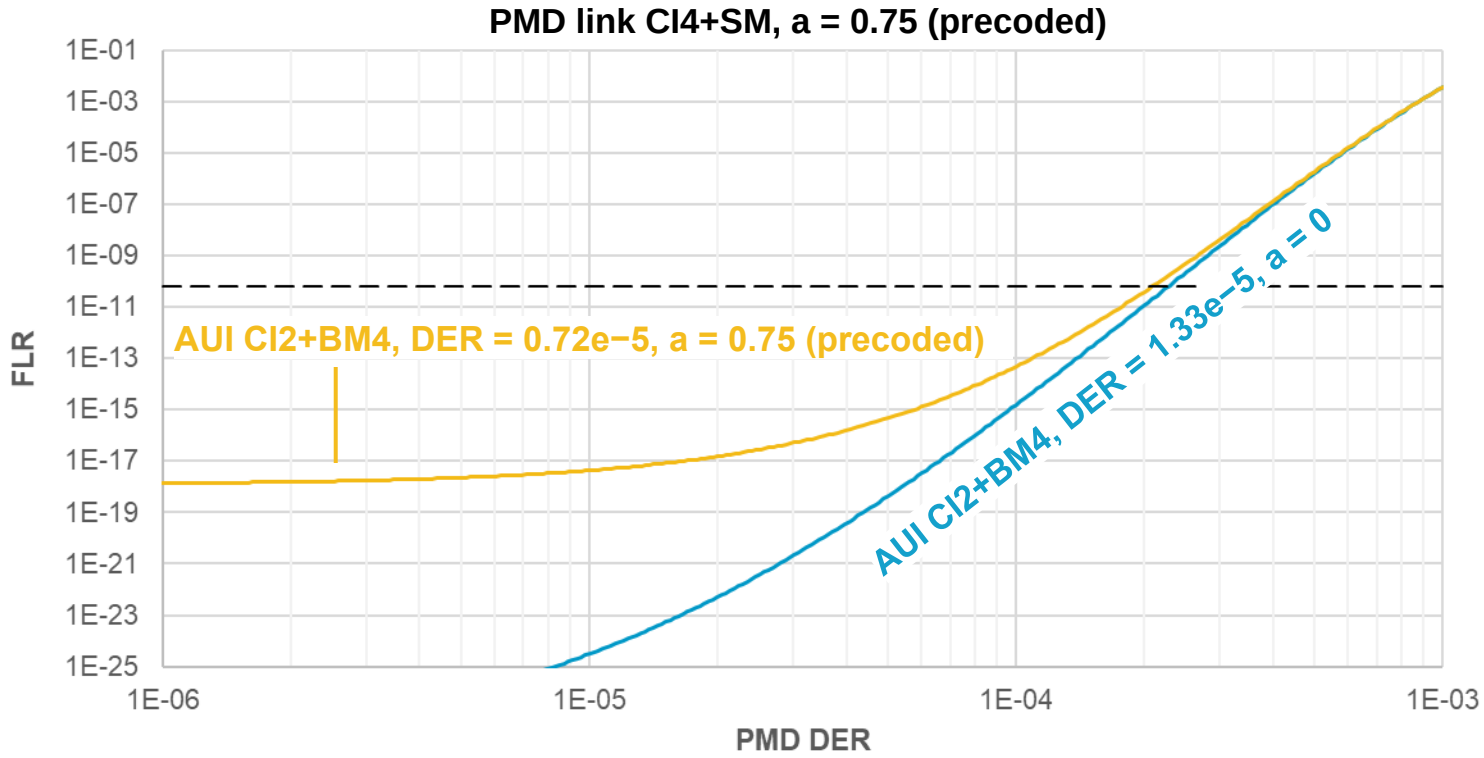


- This is referred to as “CI2+BM4” on the following slide
- PMA adjacent to the PMD converts the multiplexing pattern to “CI4+SM” for the PMD link
- The AUI receiver requirement can be met with DER = 1.33e−5 and a = 0 or with DER = 0.67e−5, a = 0.75, and precoding

PMD link DER_0 with 100 Gb/s per lane AUIs

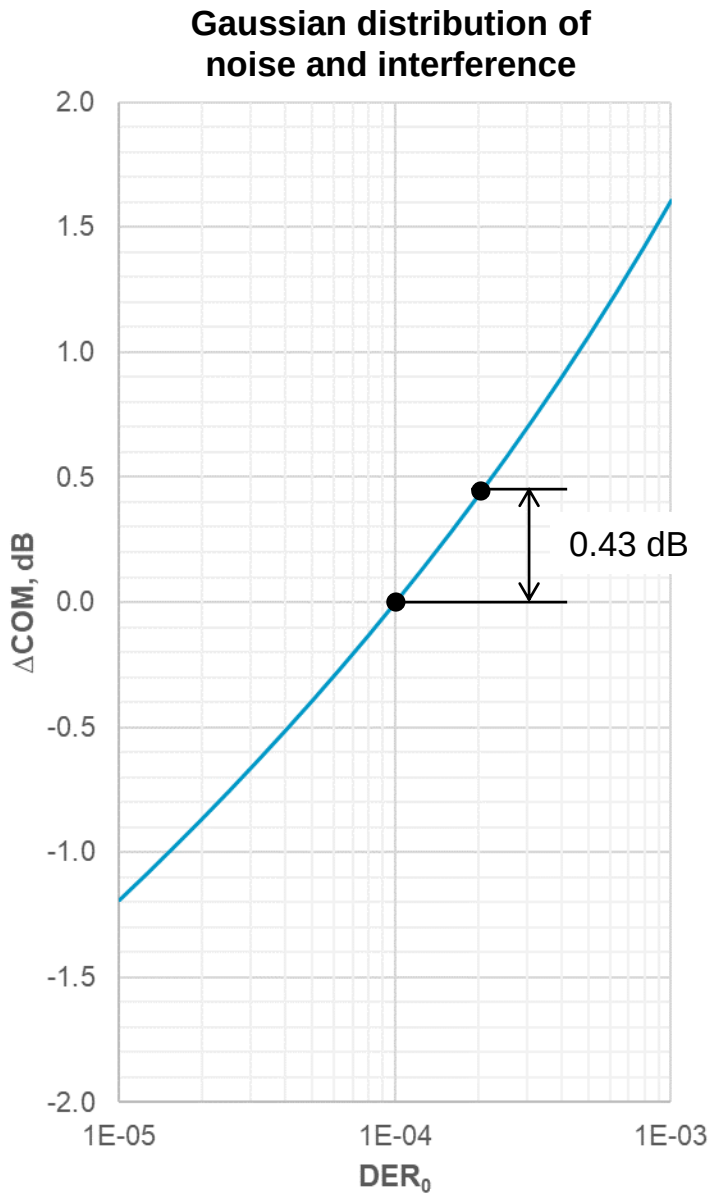


AUI DER	1.33e−5	0.67e−5
AUI a	0	0.75 (precoded)
DER_0	2.2e−4	2e−4
BER_1	1.6e−4	1.5e−4
SNR, dB	17.9	17.9



Summary and conclusions

- DER_0 = 2e−4 can be used for 200 Gb/s per lane backplane and copper cable PHYs
- About 0.4 dB improvement in COM compared to DER_0 = 1e−4
- 200 Gb/s per lane backplane and copper cable PHYs can be classified as Type 1 PHYs
- One instance of AUI C2C can be included while still meeting the FLR requirement

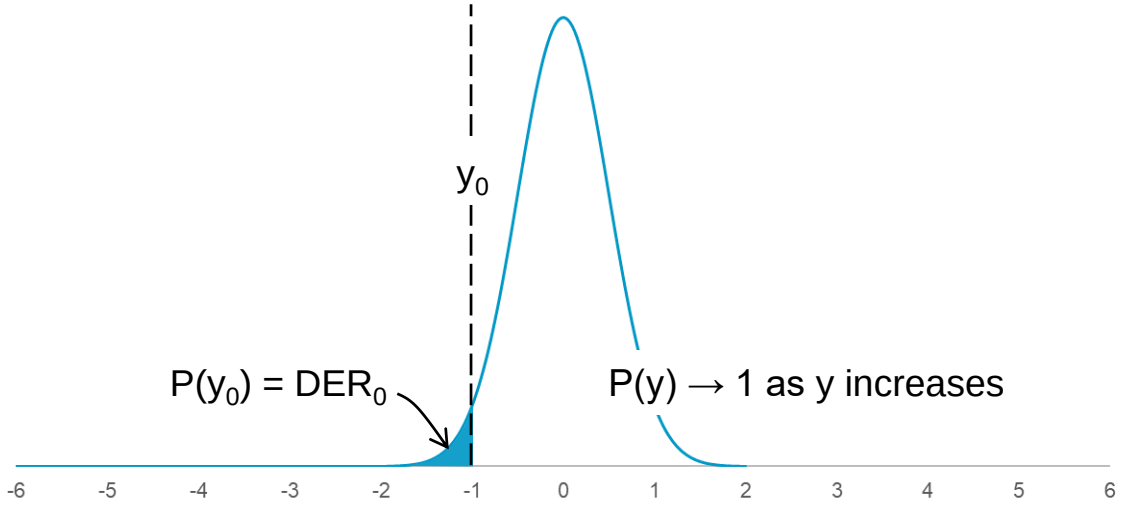


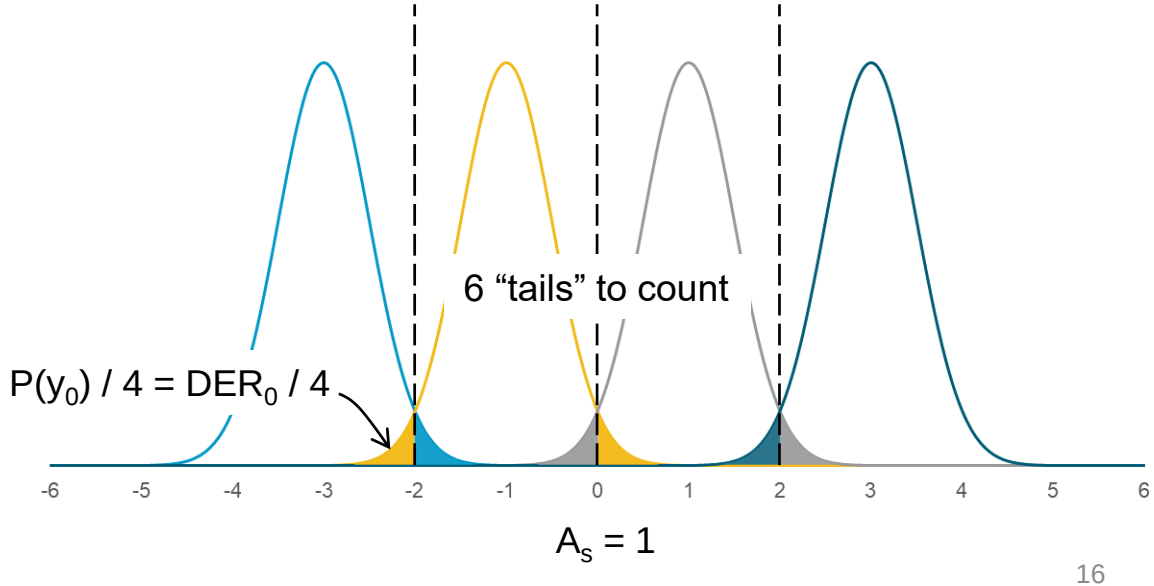
Back-up slides

Relationship between DER_0 and SER_1

- DER is the cumulative distribution of noise and interference as a function of amplitude
- y_0 is the amplitude for which DER is equal to DER_0
- A_{ni} is the magnitude of y_0
- $COM = 20 \log_{10}(A_s / A_{ni})$

- L is the number of signal levels i.e., PAM-L
- For L > 2, two threshold crossings must be considered for the inner signal levels
- There are 2(L − 1) ways to make an error over L signal levels
- $SER_1 = 2(1 - 1/L)\ DER$
- For L = 2, SER_1 = DER but <u>not</u> for L > 2





100 Gb/s per lane AUI C2C receiver requirements

- Table 120F−5 note a)

  The FEC symbol error ratio is measured in step 10) of the receiver interference tolerance method defined in 93C.2

- 93C.2 step 10)

  Measure the FEC symbol error ratio on the receiver under test using the errored symbol counter, FEC_symbol_error_counter_i, where i is the lane number of the receiver under test.

- 119.3.4

  FEC_symbol_error_counter_i (where i=0 to 7 for the 200GBASE-R PCS and i=0 to 15 for the 400GBASE-R PCS) are 32-bit counters that count once for each 10-bit symbol corrected on PCS lane I when align_status is true.

- 172.3.4 (IEEE P802.3df/D3.1)

  FEC_symbol_error_counter_i (where i=0 to 31 for the 800GBASE-R PCS) are 32-bit counters that count once for each 10-bit symbol corrected on PCS lane i when align_status is true.

Interpretation of requirements

- FEC_symbol_error_counter_i corresponds to PCS lane i
- However, the receiver test is performed on physical lane j which includes 4 PCS lanes
- 93C.2 step 10) instructs the user to measure FEC symbol error ratio using FEC_symbol_error_counter_i where i is set to the physical lane number j
- Physical lane j may not even include PCS lane i
- The FEC symbol error ratio measurement will miss errors on 3 or 4 of the 4 PCS lanes included in physical lane j
- The Annex 120F FEC symbol error ratio requirement appears incorrect so the equivalent BER requirement is considered instead
- Note that Clause 162 was modified in a manner that appears to recognize this issue while Clause 163 and Annex 120F were not

Clause 162 receiver requirements

- Table 162–16 note a)

  See 162.9.5.3.5 for definition of FEC symbol error ratio.

- 162.9.5.3.5

  Symbol error ratio is measured using the per-lane FEC symbol error counters (see 91.6 or 161.6) in the adjacent FEC sublayer, or the per-lane PCS symbol error counters (see 119.3.1) in the adjacent PCS, as appropriate.

  The FEC symbol error ratio is defined as the sum of the symbol error counters on all lanes divided by the number of symbols transmitted on all lanes, which may be estimated from the test time.

  [...]

  NOTE—If noise is applied to each of the n lanes one at a time, results of the n measurements are summed to yield the FEC symbol error ratio. The result may need to be corrected based on the FEC symbol error ratio with no noise added on any lane.