

# COM Simulation for 200G/L CR and KR with Floating FFE Taps

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**IEEE P802.3dj Task Force** 

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#### **Contributors**

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#### **Overview**

- **□** Background and Objective
- COM Analysis with Post Tap Dimension
- Benefits from Floating Taps
- Discussion and Summary

#### **Background and Objective**

- Discussion on floating FFE since August 2023
  - Floating-tap DFE and FFE have been compared in <a href="lit\_3dj\_elec\_01a\_230817"><u>lit\_3dj\_elec\_01a\_230817</u></a>, which shows impact on channel pass/fail
  - <u>lit\_3dj\_01a\_2309</u> and <u>lim\_3dj\_05\_2309</u> addressed the floating FFE methodology for COM
- mellitz\_3dj\_elec\_02\_231026 investigated the effect on RX FFE length
  - Without MLSE, 120+ post taps required to meet 40dB loss target and 3dB COM
  - Floating taps are not used for this set of experiments
- This presentation provides results from COM 4.2beta2 with floating FFE implementation to help progress CR & KR baseline equalizer
  - Key feature of COM 4.2beta2: floating DFE → floating FFE
  - Change from COM 4.2beta (This presentation): floating bank searched based on pulse response (ISI), instead of FFE coefficients

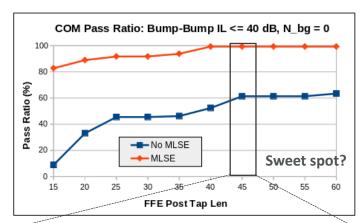
### **COM Configuration for KR & CR**

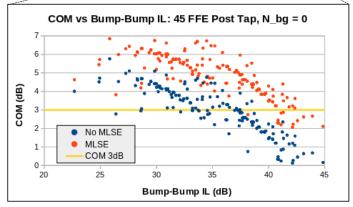
Table 93A-1 parameters			i	I/O control			Table 93A-3 parameters	i	
Parameter	Setting	Units	Information	DIAGNOSTICS	• 0	logical	Parameter	Setting	Units
f b	106.25	GBd	information	DISPLAY WINDOW	0	logical	package tl gamma0 a1 a2	[0 8.455e-4 3.40225e-4]	Onits
f min	0.05	GHz		CSV REPORT	• 0	logical	package_tl_gaiiiia0_a1_a2 package tl tau	0.00644805	ns/mm
Delta f	0.03	GHz		RESULT DIR	.\results\CAKR {date}\	logical	package_u_tau package Z c	[92 92; 70 70; 80 80; 100 100]	Ohm
C d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4 ]	nF	[TX RX]	SAVE_FIGURES	O .viesuits\cAkk_(uate)\	logical	package_z_c	[92 92, 70 70, 80 80, 100 100]	Offill
L s	[0.13 0.15 0.14; 0.13 0.15 0.14 ]	nH	[TX RX]	Port Order	[1324]	logical	Parameter	Setting	
C b	[0.3e-4 0.3e-4]	nF	[TX RX]	RUNTAG	CAKR RCos eval		board tl gamma0 a1 a2	[0 6.44084e-4 3.6036e-05]	1.5 db/in @ 56G
z_p select	[0.36-4 0.36-4]	HF	[test cases to run]	COM CONTRIBUTION	CARR_RCOS_EVAI_	logical	board tl tau	5.790E-03	ns/mm
z_p (TX)	[12 31; 1 1 : 1 1 : 0.5 0.5 ]	mm	[test cases to run]	Operational	0	logical	board Z c	100	Ohm
z p (NEXT)	[12 29; 11 ; 11; 0.5 0.5]	mm	[test cases]	ERL Pass threshold	9.7	dB	z bp (TX)	125	mm
z p (FEXT)	[12 31: 1 1 : 1 1 : 0.5 0.5 ]	mm	[test cases]	COM Pass threshold	3	db	z bp (NEXT)	0	mm
z p (RX)	[12 29; 1 1 ; 1 1 ; 0.5 0.5 ]	mm	[test cases]	DER 0	1.00E-04	ub	z_bp (REXT)	125	mm
PKG Tx FFE preset	[12 27; 11 ; 11; 0.5 0.5]	111111	[test cases]	T r	4.00E-03	ns	z bp (RX)	0	mm
C p	[0.5e-4 0.5e-4]	nF	[TX RX]	FORCE TR	4.000-03	logical	C 0	[0,2e-4 0]	nF
R O	50	Ohm	[IARA]	PMD type	C2C	logical	C_0	[0.2e-4 0]	nF
R d	[45 45]	Ohm	[TX RX]	EW	1		Include PCB	0.26-4 0]	logical
A v	0.39235	V	vp/vf=	TDR and ERL options	+ '	logical	Include PCB		logical
A_V A fe	0.39235	V	vp/vf=	TDR and ERL options	1	logical			
A_re A ne	0.37233	V	vp/ vi-	ERL	1	logical	Seletions (rectangle, gaussian,dual rayleigh,triangle		
A_lie	4	v		ERL ONLY	0	ns	Histogram Window Weight	gaussian	selection
M .	32			TR TDR	0.01	IIS	Or	0.02	UI
filter and Eq	32			IR_IDR N	3500	logical	Qr	0.02	OI .
f r	0.6	*fb		TDR Butterworth	1	logical			
c(0)	0.54	10	min	beta x	0		ICN parameters		
c(-1)	[-0.4:0.02:0]		[min:step:max]	rho_x	0.618		f v	0.594	Fb
c(-1)	[0:.02:0.12]		[min:step:max]	TDR W TXPKG	0.010	UI	f f	0.594	Fb
	[0:.02:0.12]		[min:step:max]	N bx	0	01	f n	0.594	Fb
c(-3) c(-4)	0		[min:step:max]	fixture delay time	[00]		f_n f 2	79,688	GHz
c(-4)	0		[min:step:max]	Tukev Window	1		A ft	0.450	V V
N b	0	UI	[min:step:max]	Noise, jitter	1		A nt	0.450	V
b max(1)	0.75	UI	As/dffe1	sigma RJ	0.01	UI	A_nt	0.450	v
b_max(1)	[0.3 0.2*ones(1.22)]	_	As/dfe2N b	sigma_k; A_DD	0.01	UI	Floating Tap Control		
b_max(2N_b)	[0.3 0.2 ones(1,22)]		As/dfe1	eta 0	6.00E-09	V^2/GHz			0.1.2 2
b_min(1)	[-0.2 -0.2*ones(1,22)]		As/dfe2N b	SNR TX	6.00E-09	dB	N_bg N bf	xx 5	0 1 2 or 3 groups
	[-0.2 -0.2 ones(1,22)]	-Jn	[min:step:max]	R LM	0.95	UD .	N_DI N f	60	taps per group UI span for floating taps
g_DC f z	[-12:1:0] 42.5	dB GHz	[min:step:max]	K_LM	0.95		N_T bmaxg	0.2	max DFE value for floating taps
	42.5 42.5	GHz			-	_	N tail start		(UI) start of tail taps limit
f_p1 f p2	42.5 106.25	GHz		Enforce Causality	0 trend to DC		N_tall_start	XX	(OI) Start OI tail taps limit
	[-6:1:0]	GHZ	[minustanum nu²	S-parameter magnitude extrapolation policy	trenu_to_DC				
g_DC_HP f HP PZ	1.328125	CII	[min:step:max]	51h P555				0	IiI
		GHz logical	include in fe	Filter: RxFFE		UI	MLSE		logical
Butterworth	0		include in fr	ffe_pre_tap_len	6		Deserve testine		
Raised_Cosine	6.70E+10	logical	include in fr	ffe_post_tap_len	xx	UI	Receiver testing		leeleel.
RC_Start	6.70E+10 7.97E+10	Hz	start freq for RCos	ffe_tap_step_size	0		RX_CALIBRATION	0	logical V
RC_end	/.y/E+10	Hz	end freq for RCos	ffe_main_cursor_min	1		Sigma BBN step	5.00E-03	V
CDR	[4/0]			ffe_pre_tap1_max	1	$\vdash$	II adf na annad		
sample_adjustment	[-16 8]	phase		ffe_post_tap1_max	1	$\vdash$	mli_3df_02_220316		
ts_anchor	1			ffe_tapn_max ffe_backoff	1 0		benartsi_3df_01a_2211		
				пе_раскоп	1 0				

#### First look at the CR/KR Channels: Fixed FFE Tap Only

- Total of 145 test cases varies with
  - All CR & KR channels posted in 802.3dj <u>Tools & Channels</u>
  - 2 package test cases: short/long
  - Bump-bump IL <= 40dB</p>

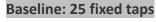
- With MLSE, 40 taps are good enough?
  - COM gets consistent 2 dB gain as IL > 35dB
  - In practical, MLSE gain is a little over 1 dB at most
  - More work required here
- Power efficiency: 60+ taps vs MLSE?
  - > 45-tap seems less helpful?

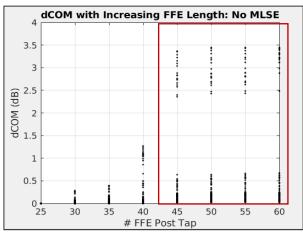


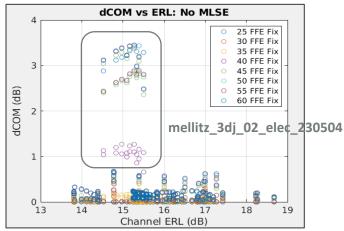


#### **Benefits from Increasing Taps: Fixed FFE Tap Only**

- FFE taps span within some ranges, e.g., 45<sup>th</sup>-60<sup>th</sup> UIs, contribute negligible COM gain
  - Benefits from floating taps?
- mellitz\_3dj\_02\_elec\_230504 channel seems to benefit more with increasing FFE taps
  - Reflections majorly located at increasing tap range?
  - Relative low ERL?
  - Need more study





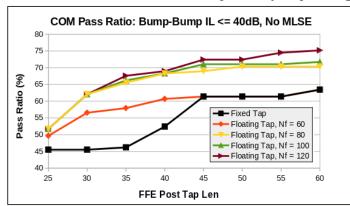


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#### **Benefits from Floating Tap**

- Floating tap enjoys higher flexibility under the identical FFE length
  - Short fixed taps + floating taps
- Sweet spots of post tap dimension
  - Floating taps with total of >= 45 taps
  - Nf = 80

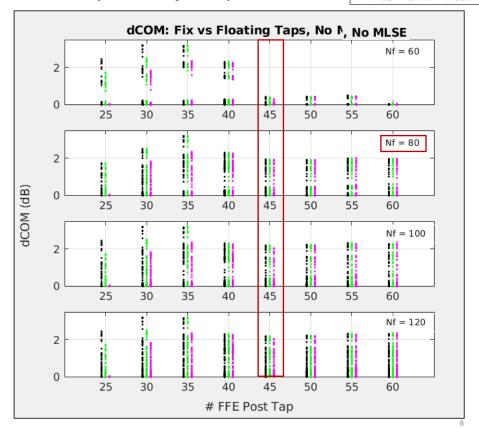
\* 20 FFE fixed taps + floating taps



#### dCOM = COM (Floating Tap)-COM (Fixed Tap Only)

\* Set total taps identical for comparison

15 FFE Fix + Floating
20 FFE Fix + Floating
25 FFE Fix + Floating



#### **Discussion and Summary**

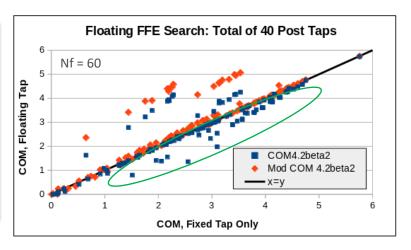
- Suggested to revise floating FFE functionality with proposed methodology for COM
- Provided CR and KR channel analysis suggesting reference parameters path forward
  - <= 45 FFE taps in total</p>
  - Floating FFE with Nf <= 80</p>
- Recommended baseline equalizer for 802.3dj CR and KR: MLSE with floating FFE taps
  - Floating taps yield benefit of less taps
  - Need more study on MLSE behavior in COM

# Appendix





- COM 4.2beta2: Floating bank search methodology
  - Step 1: Compute FFE coefficients for all taps within floating tap range Nf
  - Step 2: Search floating bank location based on resulting FFE coefficient in Step 1
- [This Presentation] Modified COM 4.2beta2
  - Step 1: Search floating bank location based on FFE input SBR (ISI), see lit\_3dj\_01a\_2309



- With the same tap number, fixed tap outperforms floating tap frequently
  - [Major] Current methodology of floating bank search cannot guarantee the optimal bank location
    - FFE coefficients are hard to determine ISI strength directly due to inherent behavior of convolution
    - Suggestion: Search bank location based on ISI, instead of FFE coefficients
  - [Minor] Even we allocate floating taps to the identical location that fixed taps used, the resulting FFE coefficients are different
    - COM 4.2beta2 simply set all resulting FFE coefficients at non-selected floating taps to 0
    - Suggestion: Calculate FFE coefficients with selected taps only (and their corresponding delay)

## Thank you

**Questions and Discussions**