A Baseline Proposal To Enable More Flexible Architectures and Longer Reach 200Gb/Lane Passive Copper Cables

Matt Brown, AlphaWave
Sam Kocsis, Amphenol
Jason Chan, Arista
Jim Weaver, Arista
Adam Healey, Broadcom
Karlheinz Muth, Broadcom
Howard Heck, Intel
Mike Li, Intel
Kent Lusted, Intel
Rick Rabinovich, Keysight
Mike Dudek, Marvell
Piers Dawe, Nvidia
Chris Diminico, PHY-SI/SenTekse
Richard Mellitz, Samtec
Megha Shanbhag, TE Connectivity
Nathan Tracy, TE Connectivity

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Supporters

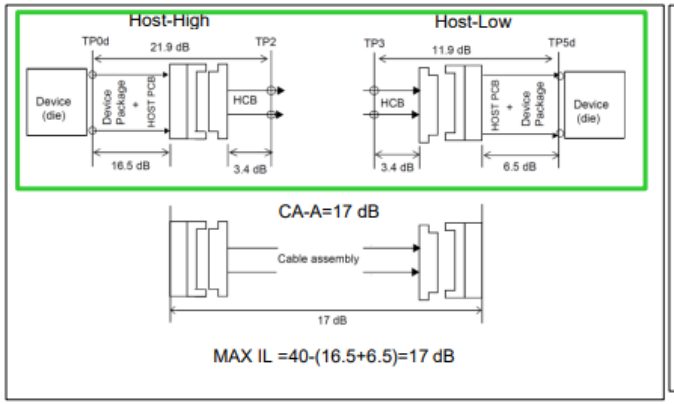
- Leesa Noujeim, Google
- Cedric Lam, Google
- Alex Levin, Microsoft
- Karl Bois, Nvidia
- Scott Sommers, Molex
- Vivek Shah, Molex
- Lenin Patra, Marvell
- Femi Akinwale, Intel
- Terry Little, FIT
- Jeffery Maki, Juniper Networks
- Ali Ghiasi, Ghiasi Quantum
- Mike Klempa, AlphaWave
- David Cassan, AlphaWave
- Upen Reddy Kareti, Cisco
- Pirooz Tooyserkani, Cisco

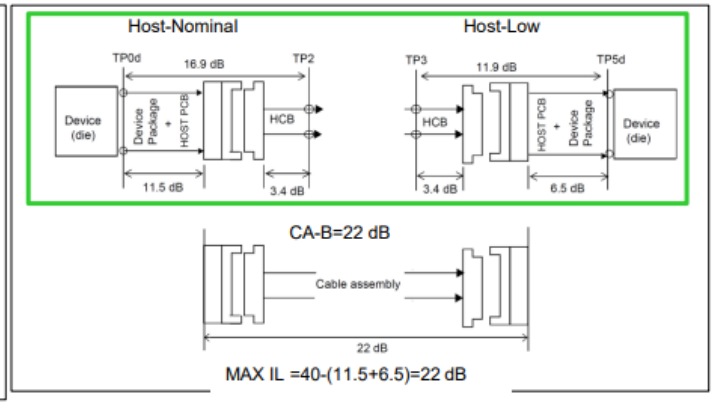
Background

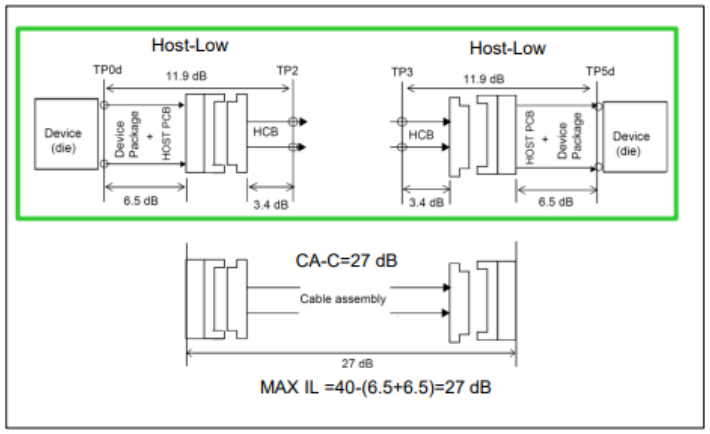
- As CR signalling rates increase, the loss per length increases as f(GHz) increases, and the cable reach, decreases. To address this, this presentation proposes careful management of the budgeted losses for 200G/lane passive copper cables
- July 2023: “A Possible Path to More Flexible Architectures and Longer Reach Passive Copper Cables” presentation (tracy_3dj_01a_2307.pdf) presented the concept of reallocating loss budget where it is not being utilized to enable more flexible architectures and longer cables.
- September 2023: “Considerations for Insertion Loss Budget Baseline” presentation (diminico_3dj_01a_2309.pdf) proposed insertion loss budgets for symmetrical link cases as well as these new flexible architectures and longer cables
- Further detail was requested in September to support the proposal

Proposal from Sept: diminico_3dj_01a_2309

Asymmetrical Links - Informative Annex







Link Configurations IL (TX to RX)

	Host-Low	Host-Nominal	Host-High
Host -Low	CA-A,B,C	CA-A,B	CA-A
Host-Nominal	CA-A,B	CA-A	not supported
Host-High	CA-A	not Supported	not supported

Device Package + Host PCB		Cable + 2xconnectors	
Host-Low	6.5 dB	CA-A	17 dB
Host-Nominal	11.5 dB	CA-B	22 dB
Host-High	16.5 dB	CA-C	27 dB

802.3dj Task Force

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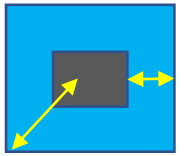
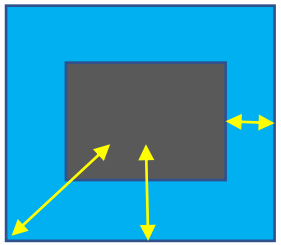
- Requested to bring further support for HL (Host-Low) and HH (Host-High) implementations
- Following slides show supporting examples

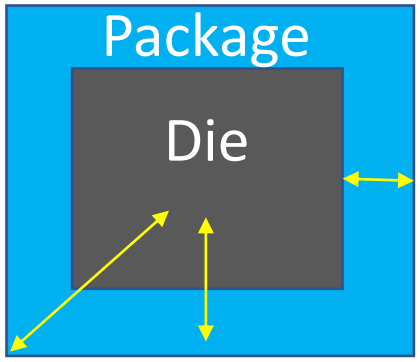
This is NOT a nomenclature proposal! It's about better utilization of our loss budgets

Package Losses

- Overall package size varies
  - NIC or FPGA may be small to medium package, short to medium traces
  - Switches or routers typically have larger packages
  - Loss optimized/Radix optimized may have short, medium and long package traces, all in the same device
- Differences between shortest package trace to longest package trace within a given package become more significant with large packages
- We want to be able use every dB of loss effectively

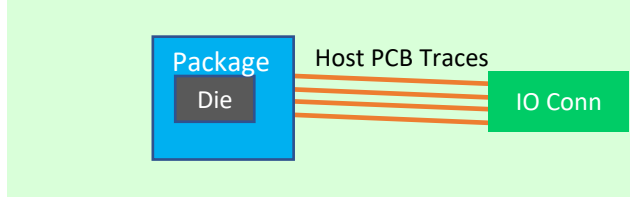


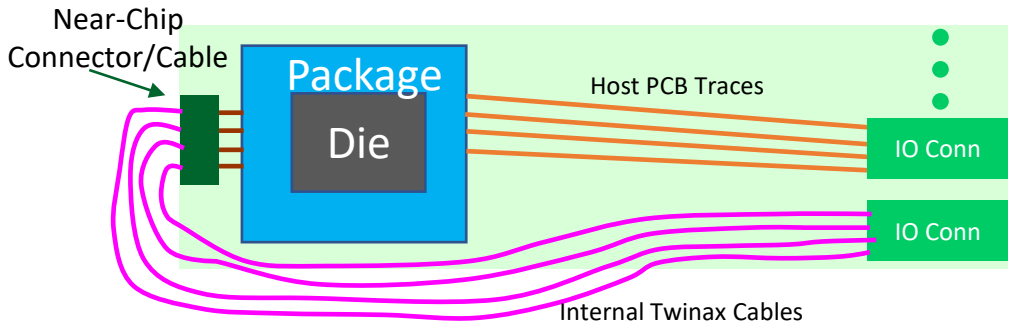


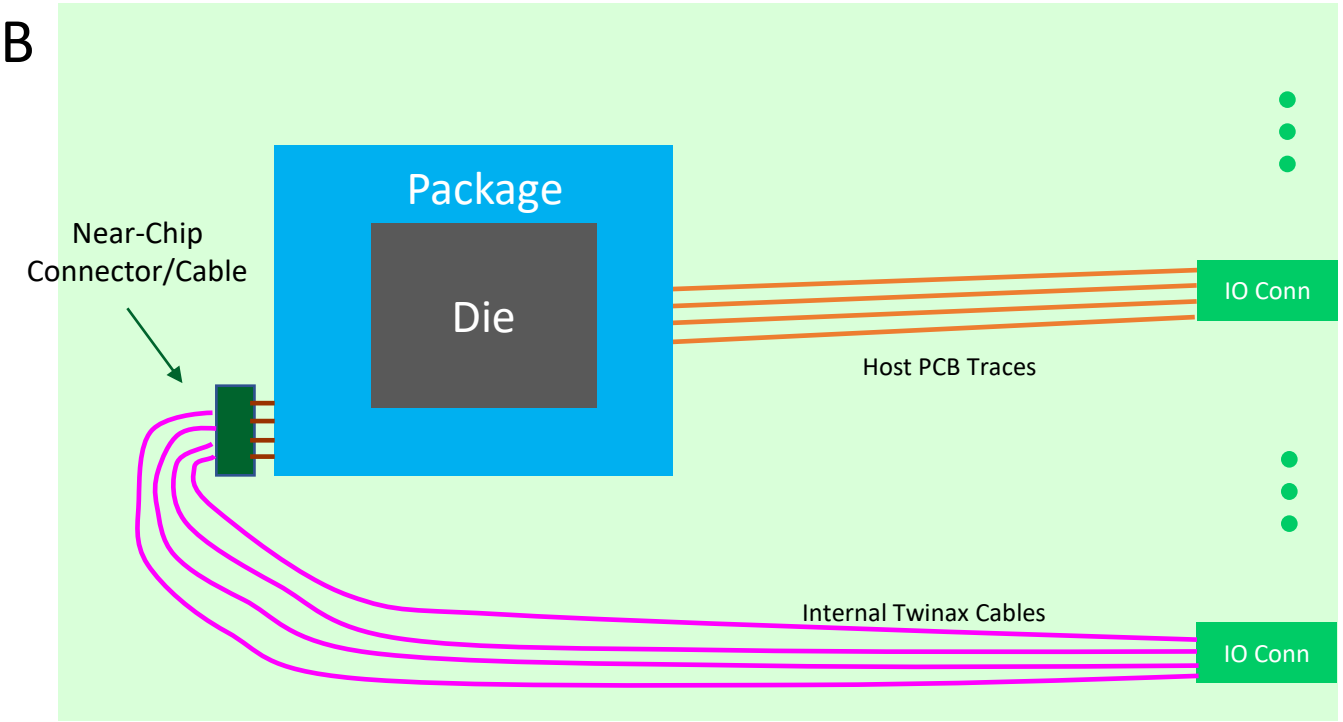


Host losses

- Host loss will vary:
  - NIC or FPGA may have short to medium traces
  - Nominal cases may have mix of PCB traces, and
  - Mix of internally cabled twinax w/near-chip connectors,
  - Or, 100% cabled twinax

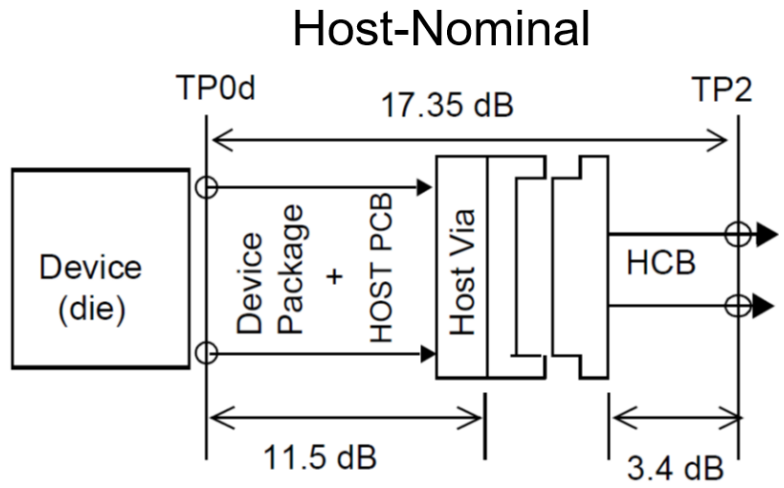


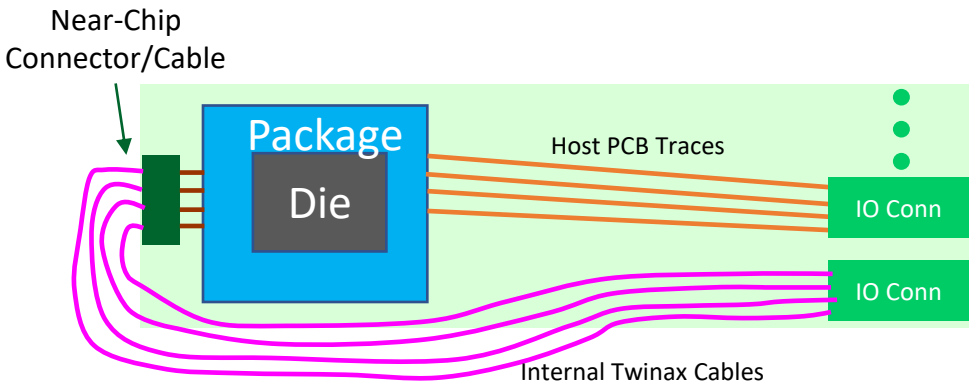




HN (Host-Nominal) Possible Implementation

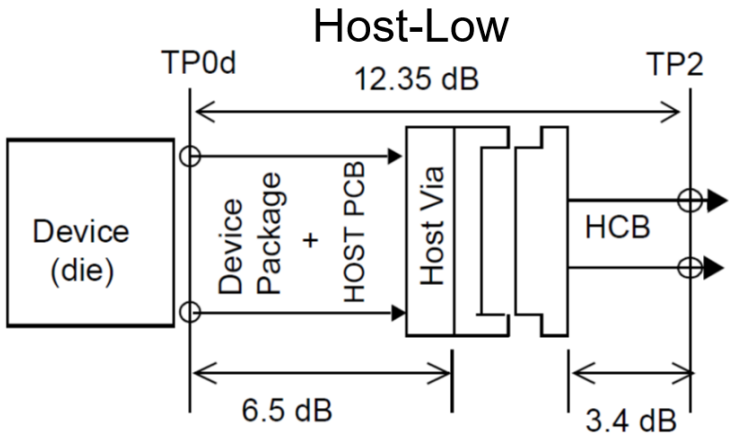
- This has been adopted as baseline at Sept ’23:
  - “Move to adopt the the CR host and cable assembly insertion loss budget proposed in diminico_3dj_01a_2309, slide 7 for the symmetrical CR use case.”
  - See: (motion 5, page 22 of https://www.ieee802.org/3/dj/public/23_09/motions_3cwdfdj_2309.pdf)
  - Host (pkg+PCB trace) loss of 11.5dB and cable assembly loss of 17dB were adopted
- HN traditionally is for an implementation using a large package on a high radix port count. Some ports will fall into HN, but the extreme ports will be HH
- 11.5dB overall host loss –
  - Example allocation, PCB host based:
    - 5dB package
    - 0.5dB BGA transition
    - 6dB for PCB trace, ~4.28” reach, based on assumptions in *weaver_3dj_elec_01_230831.pdf*
  - Example allocation, cabled host based:
    - 5dB for package
    - 0.5dB for BGA transition
    - 2.8dB for PCB trace, ~2” reach, based on assumptions in *weaver_3dj_elec_01_230831.pdf*
    - 1dB for the Near package connector
    - 2.2dB for 30AWG-6.8in cable

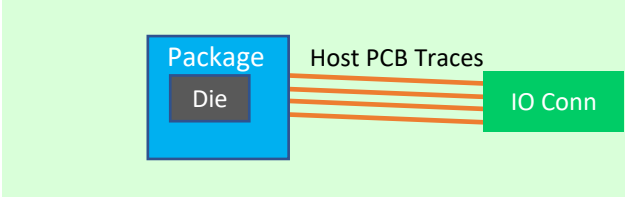




HL (Host-Low) Possible Implementation

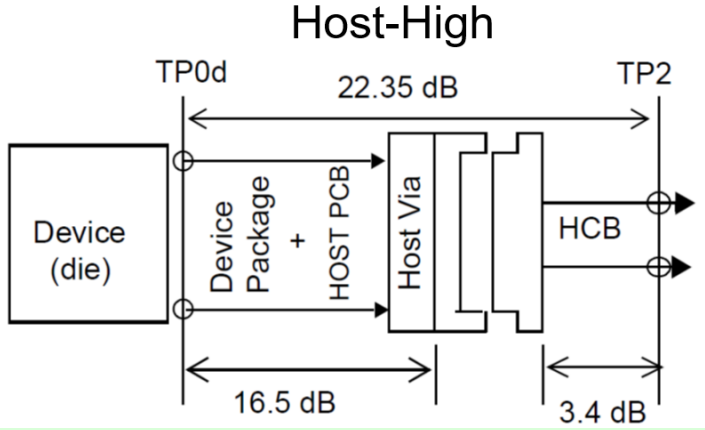
- The classic thought of HL is a NIC, but could also be a retimer
- 6.5dB overall HL loss –
  - Example allocation:
    - 3.9dB for package loss
    - 0.5dB for BGA transition
    - 2.1dB for PCB trace, ~1.5” reach, based on assumptions in *weaver_3dj_elec_01_230831.pdf*

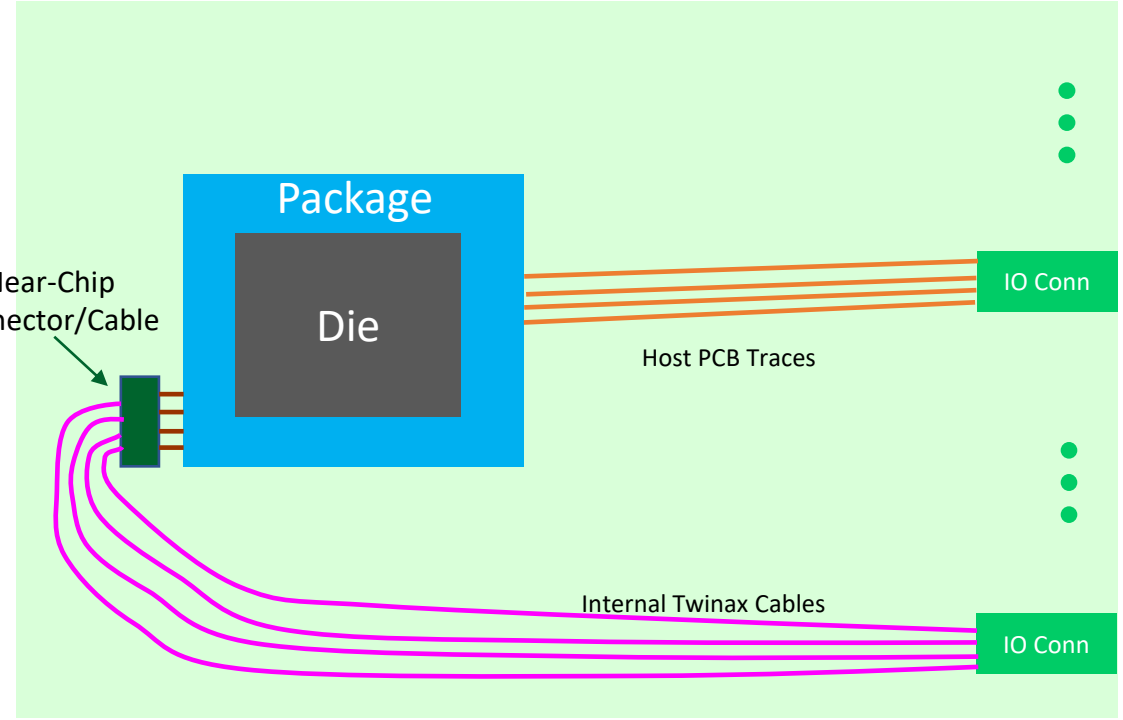




HH (Host-High) Possible Implementation

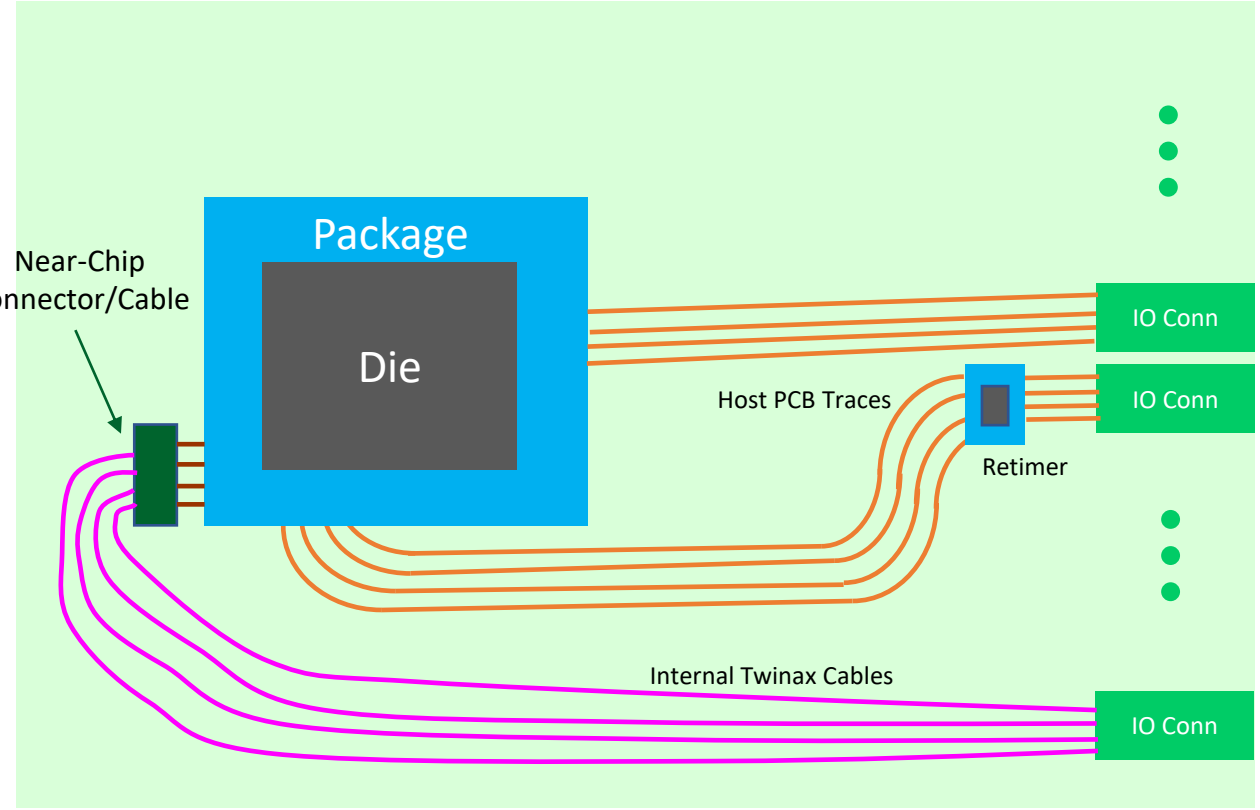
- HH is for an implementation using a large package on a higher radix port count. Some ports will fall into HN, but the extreme ports will be HH
- 16.5dB overall host loss –
  - Example allocation, PCB host based:
    - 9dB package
    - 0.5dB BGA transition
    - 7dB for PCB trace, ~5” reach, based on assumptions in *weaver_3dj_elec_01_230831.pdf*
  - Example allocation, cabled host based:
    - 9dB for package
    - 0.5dB for BGA transition
    - 2.8dB for PCB trace, ~2” reach, based on assumptions in *weaver_3dj_elec_01_230831.pdf*
    - 1dB for the Near package connector
    - 3.2dB for 32AWG-8in cable



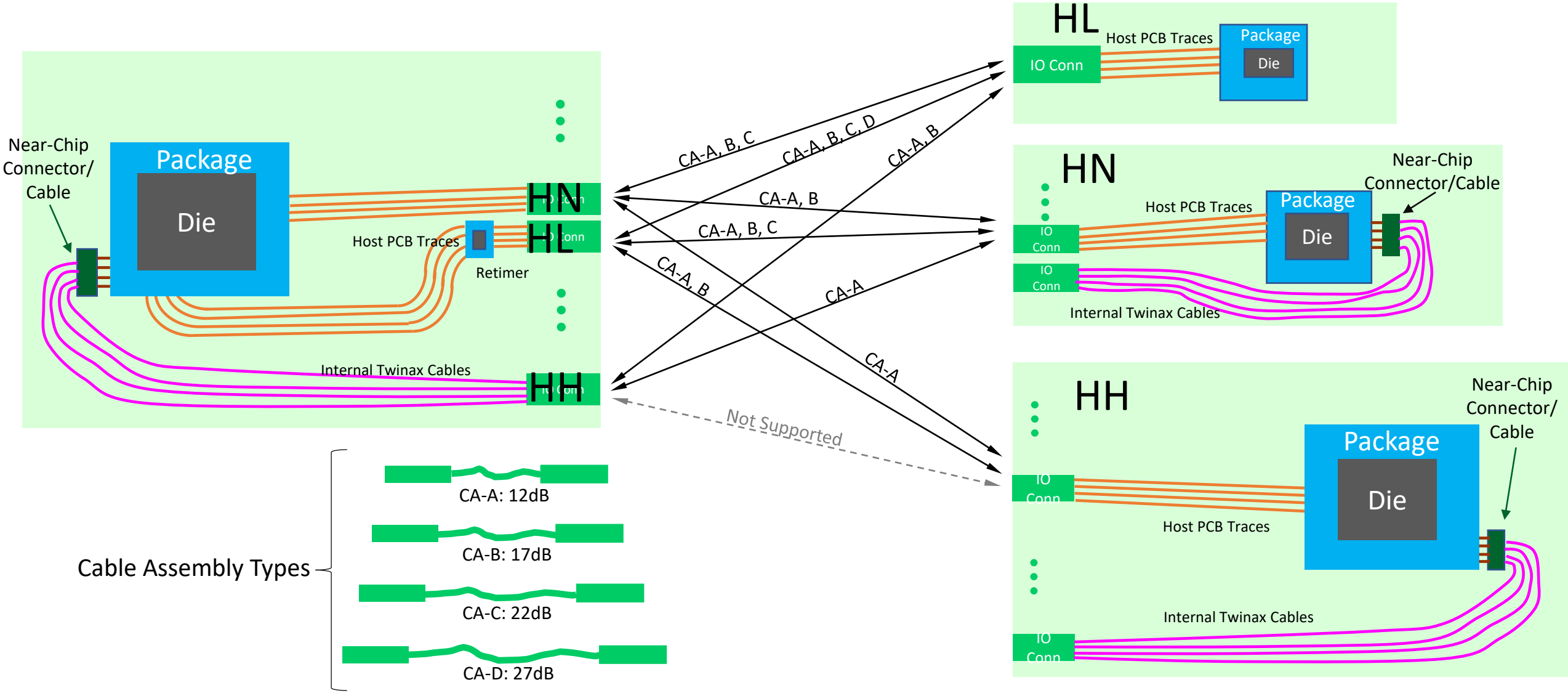


HL, HN, and HH Can All Exist In A Single Implementation

- Best case pkg loss, worst case pkg loss all on the same device
- Low host loss, nominal host loss and high host loss all on the PCB
- It is reasonable that product implementations can have a combination of HL, HN, HH
- End users can leverage these combinations for longer external cables



Flexible Host Architecture



Proposed CR die-to-die Informative Annex - Insertion Loss @53.125 GHz, page 1

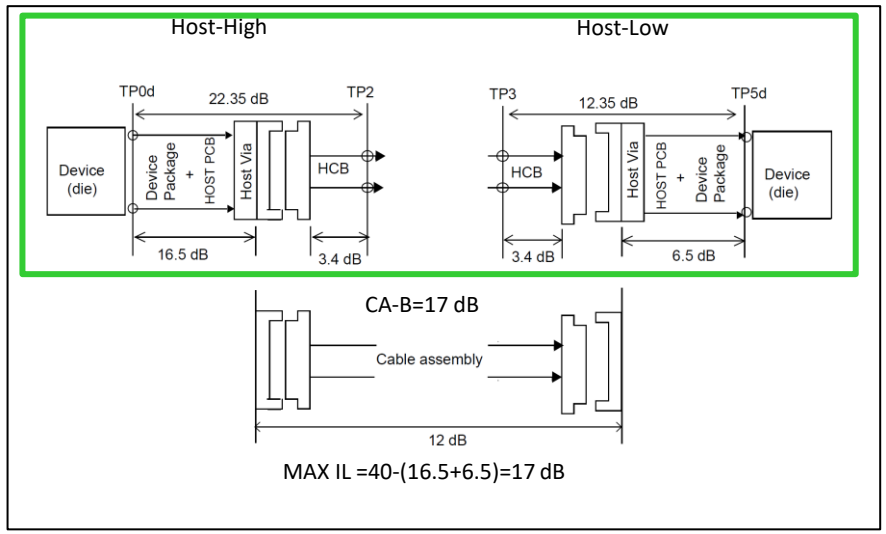
- Flexible host architectures and cable assemblies

Link Configurations IL (TX to RX)

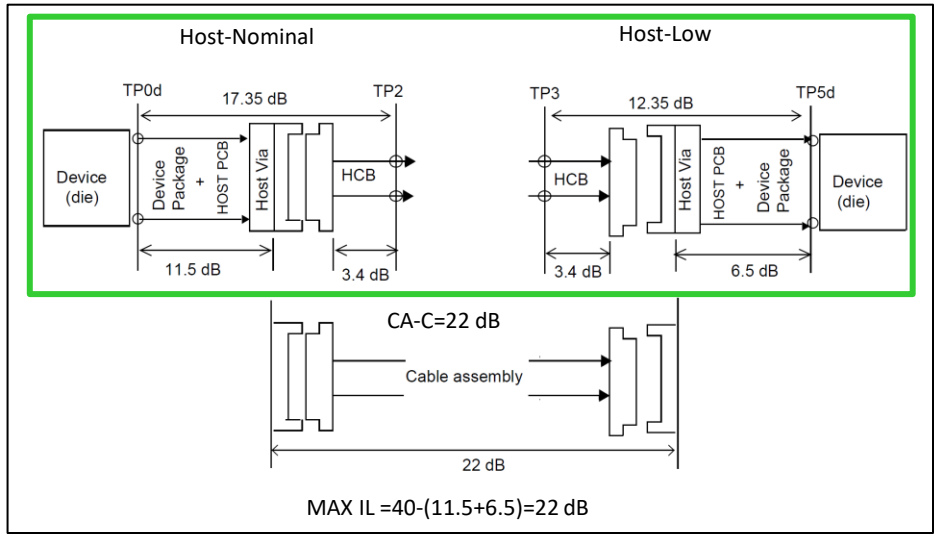
Device Package + Host PCB	Host-Low 6.5 dB	Host-Nominal 11.5 dB	Host-High 16.5 dB
Host -Low 6.5 dB	CA-A,B,C,D	CA-A,B,C	CA-A,B
Host-Nominal 11.5 dB	CA-A,B,C	CA-A,B	CA-A
Host-High 16.5 dB	CA-A,B	CA-A	not supported

Cable Assembly	Insertion Loss Cable + 2*Connectors
CA-A	12 dB
CA-B	17 dB
CA-C	22 dB
CA-D	27 dB

Proposed baseline content



NOTE—The 16.5 dB and 6.5 dB ILdd includes allowance for BGA and connector footprint vias.



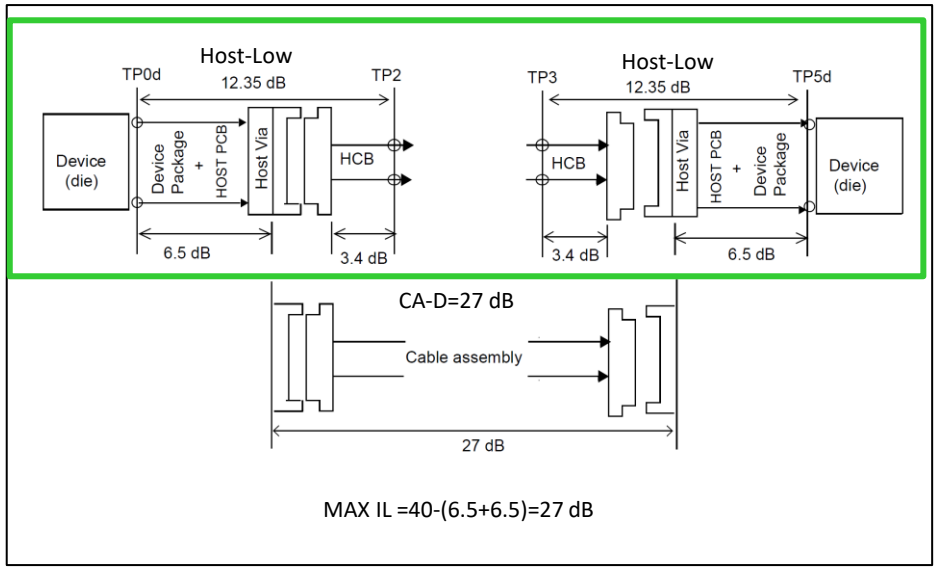
NOTE—The 11.5 dB and 6.5 dB ILdd includes allowance for BGA and connector footprint vias.

*Host Losses predicated on MTF IL assumptions https://www.ieee802.org/3/df/public/adhoc/electrical/22_0502/diminico_3df_01_220502.pdf slide 7

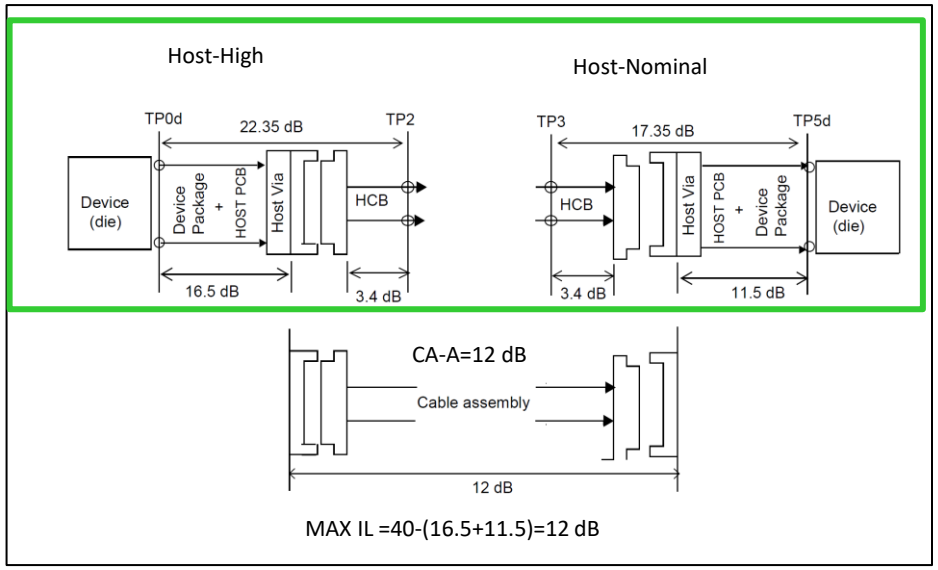
Note: Module compliance board (MCB) is not shown and is the subject of a separate proposal

Proposed CR die-to-die Informative Annex - Insertion Loss @53.125 GHz, page 2

- Flexible host architectures and cable assemblies



NOTE— 6.5 dB ILdd includes allowance for BGA and connector footprint vias.



NOTE—The 16.5 dB and 11.5 dB ILdd includes allowance for BGA and connector footprint vias.

Note: Module compliance board (MCB) is not shown and is the subject of a separate proposal

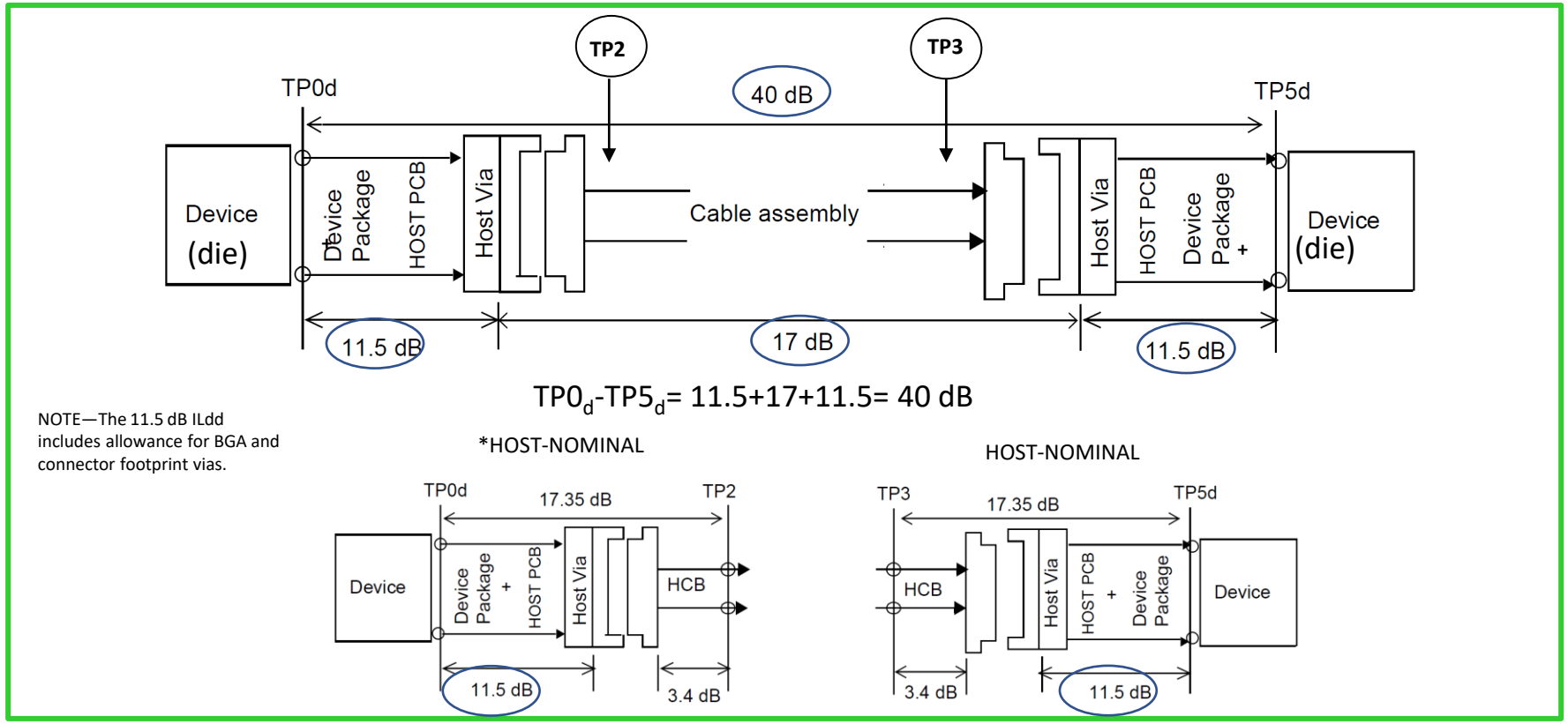
*Host Losses predicated on MTF IL assumptions https://www.ieee802.org/3/df/public/adhoc/electrical/22_0502/diminico_3df_01_220502.pdf slide 7

Summary

- The concept of insertion loss ‘harvesting’ and reallocation has been introduced with strong support
- Baseline content has been proposed with supporting ‘example’ implementations
- Consistent with actual use cases and deployments (at prior rates)
- Complementary to the symmetrical CR baseline (HN) that has already been adopted:
  - Move to adopt the the CR host and cable assembly insertion loss budget proposed in diminico_3dj_01a_2309, slide 7 for the symmetrical CR use case.
  - See: (motion 5, page 22 of https://www.ieee802.org/3/dj/public/23_09/motions_3cwdfdj_2309.pdf)
- Enhances broad market potential

Q & A

Adopted baseline CR die-to-die Informative Annex - Insertion Loss @53.125 GHz



MAX IL =40-(11.5+11.5)=17 dB

*Host Losses predicated on MTF IL assumptions
https://www.ieee802.org/3/df/public/adhoc/electrical/22_0502/diminico_3df_01_220502.pdf slide 7

: Values adopted at Sept interim or prior

COM and Compliance Validation

Cable Assembly	Mated-Cable IL
CA-A	Up to 12 dB
CA-B	Up to 17 dB
CA-C	Up to 22 dB
CA-D	Up to 27 dB

- COM analysis similar to 802.3ck with addition of Host Loss options in COM setup file (Host-Low, Host-Nominal, Host-High)
- COM setup file would define a *single* reference allocation of package + PCB for each of the Host options (H-L, H-N, H-H)
- COM analysis would be done for a subset of cases depending on the cable assembly
  - Further work to be completed to verify that additional validation steps are not necessary

Link Configurations IL (TX to RX)			
Device Package + Host PCB	Host-Low (6.5 dB)	Host-Nominal (11.5 dB)	Host-High (16.5 dB)
Host-Low (6.5 dB)	CA-A,B,C,**D**	CA-A,B,**C**	CA-A,**B**
Host-Nominal (11.5 dB)	CA-A,B,**C**	CA-A,**B**	CA-**A**
Host-High (16.5 dB)	CA-A,**B**	CA-**A**	

Link Configuration IL = 40dB (TP0d-TP5d)