212Gb/s Per Lane PAM4 CR Channels with Flexible Host Architectures and Longer Reach Cables - Switch Perspective

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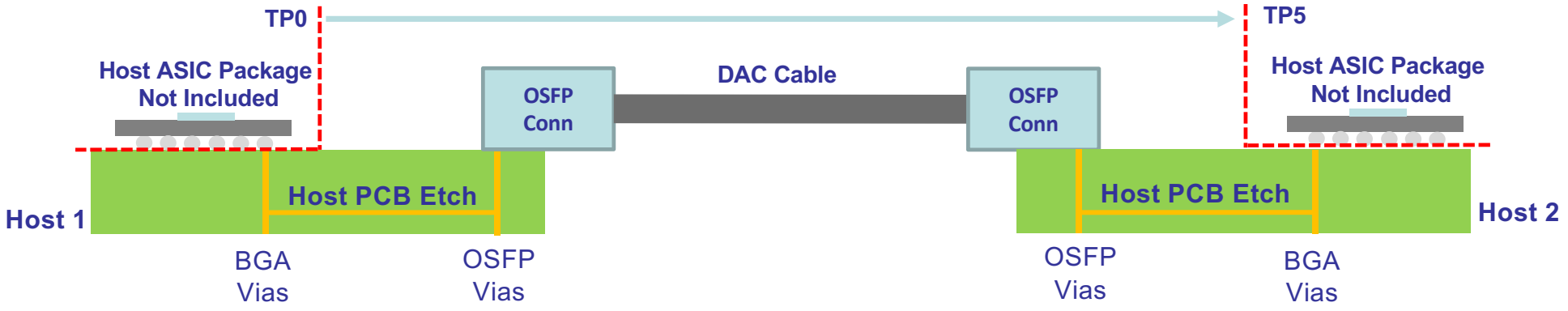
Overview

- This is a preliminary investigation into a typical CR implementation
- The intent is to facilitate early discussion among participants using *realizable channels*
  - PCB trace s-parameter data measurement procedure similar to Delta-L but using AFR
  - All PCB footprints designed using HFSS and conform to the DFM rules of major fabricators
- These models are ball-to-ball to allow use with different package models
  - Bump-to-bump channel specification is still critical, owing to large package losses
- Development is continuing, so all models are subject to continuous refinement.
  - New channels will be contributed as refinements are made

Description

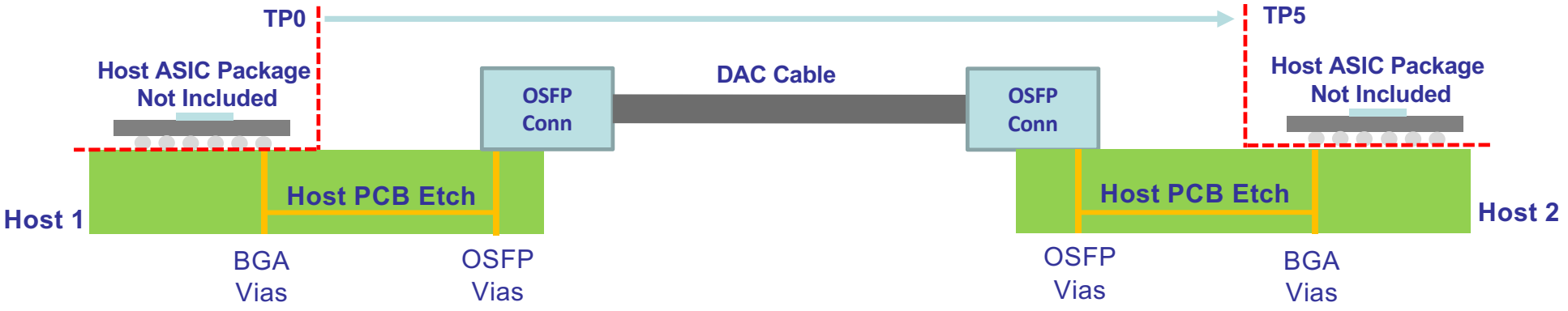
- Simulation of a typical host-to-host CR architecture over various trace lengths where one of the hosts is representative of a large switch
  - For NIC perspective, please reference akinwale_3dj_01_2311
- Composition:
  - BGA / PCB trace / OSFP via escapes simulated with HFSS
  - OSFP DAC cable assembly models with mated connectors provided by 3 vendors
- Ball-to-Ball topology: does not include package effects
- This presentation does NOT propose the following:
  - Specific aggregate losses
  - Specific host architecture implementations



Host-to-Module Composition

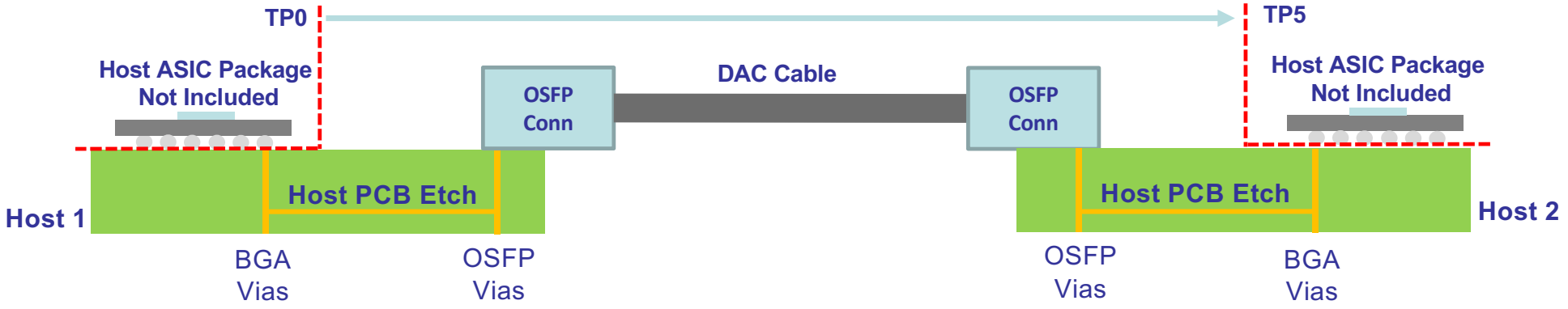
- PCB Composition
  - BGA & OSFP Breakout Footprints
    - ~ 3mm worst-case PTH breakout depth
    - 8 mil vias with 5 mil stubs
    - Conforms to current PCB fab design rules
    - Nothing exotic: no skip layers, no microvias
  - Host Breakout Trace
    - Fanout lengths to OSFP vias: 2, 3, 5 inches
    - Losses @Hi Temp: ~ 1.40 dB/in @ 53.125 GHz
    - 90 ohm @ 6 mil line width

- DAC cable Composition
  - OSFP 1x1 SMT Connector with DAC 26AWG cable
    - Vendors “X”, “Y”, “Z”
    - Room Temperature only models
    - Cable Lengths: 0.5m, 1.0m, 1.5m @ 26AWG
    - Integrated DAC cable assembly models includes
      - OSFP 1x1 connectors with mated module PCB’s
      - Cable attachment assemblies
      - 26AWG twinax cables
        - Vendor ‘X’: 100 ohms
        - Vendor ‘Y’: 95 ohms
        - Vendor ‘Z’: 92 ohms



Asymmetric Host / Cable Combos

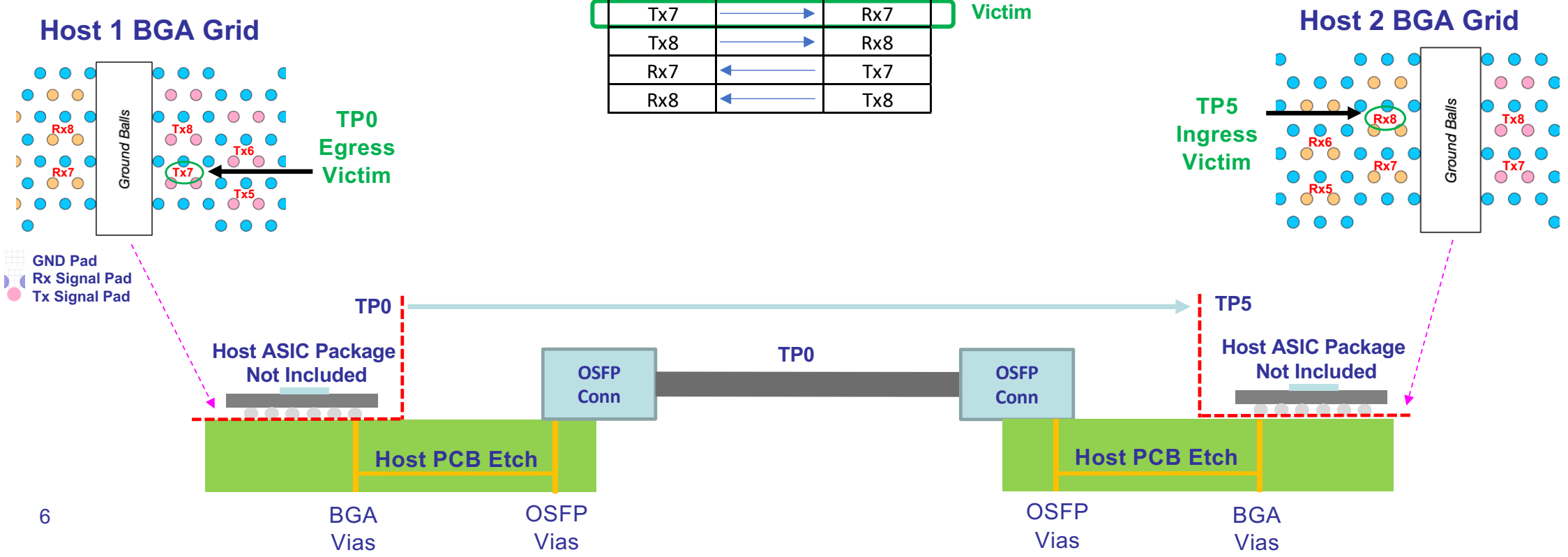
Host #1 PCB Trace	Cable	Host #2 PCB Trace
HH (5 inch)	0.5m	HN (3 inch)
HH (5 inch)	1.0m	HL (2 inch)
HN (3 inch)	1.0m	HN (3 inch)
HN (3 inch)	1.5m	HL (2 inch)



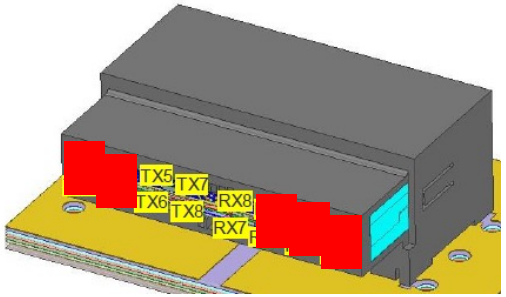
Signaling Topology

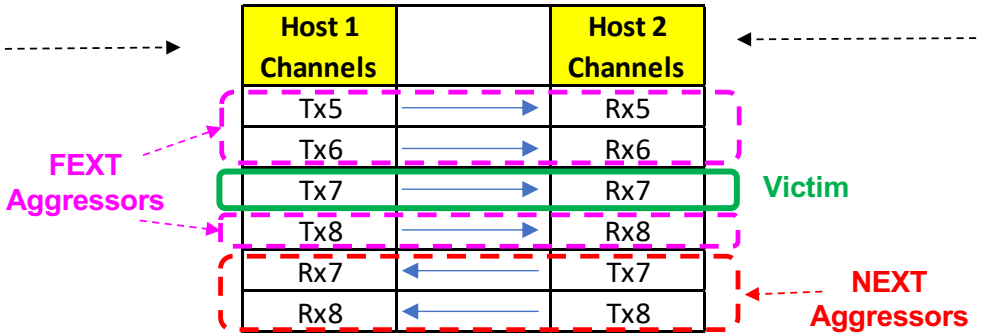
Host 1 Channels		Host 2 Channels
Tx5	→	Rx5
Tx6	→	Rx6
Tx7	→	Rx7
Tx8	→	Rx8
Rx7	←	Tx7
Rx8	←	Tx8

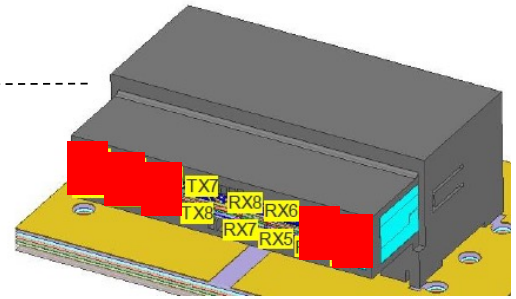
Victim



Signaling Topology

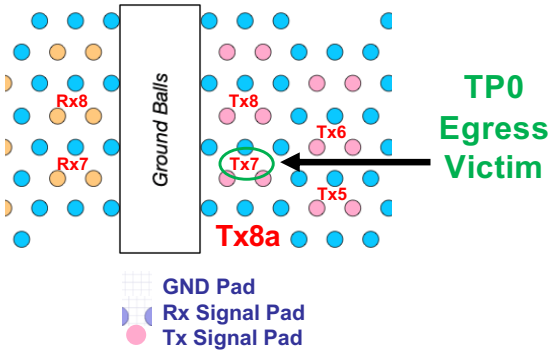






Vendor-provided DAC cable assembly models limited to the above available ports

Host 1 BGA Grid



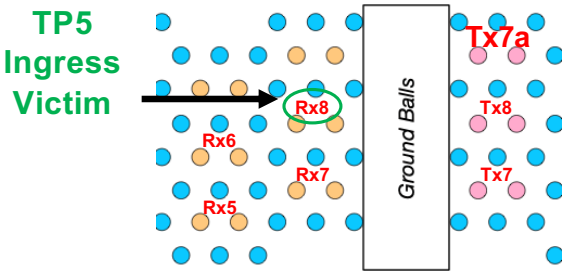
To include the "virtual" FEXT/NEXT from BGA signal balls Tx8a and Tx7a instantiate two copies of the following:

Tx8a: "…FEXT_TP0_Tx8_to_TP5_Rx7.s4p"

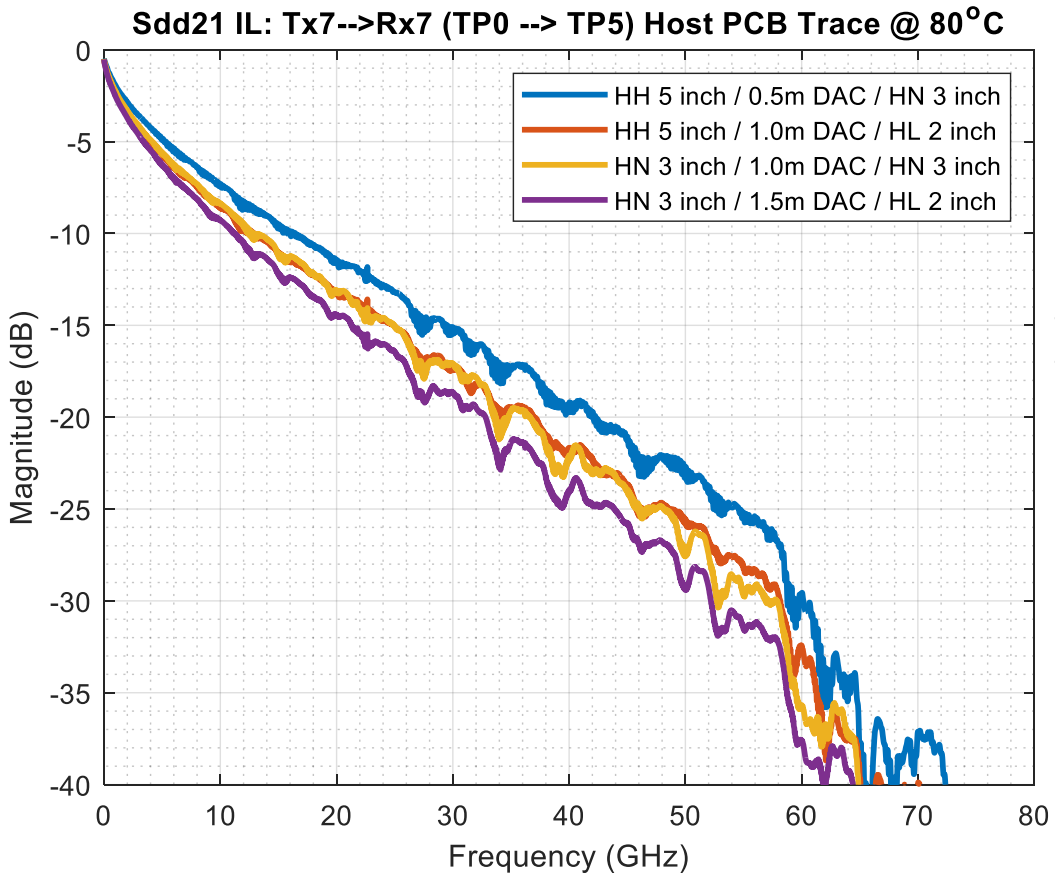
Tx7a: "…NEXT_TP0_Tx7_to_TP5_Rx7.s4p"

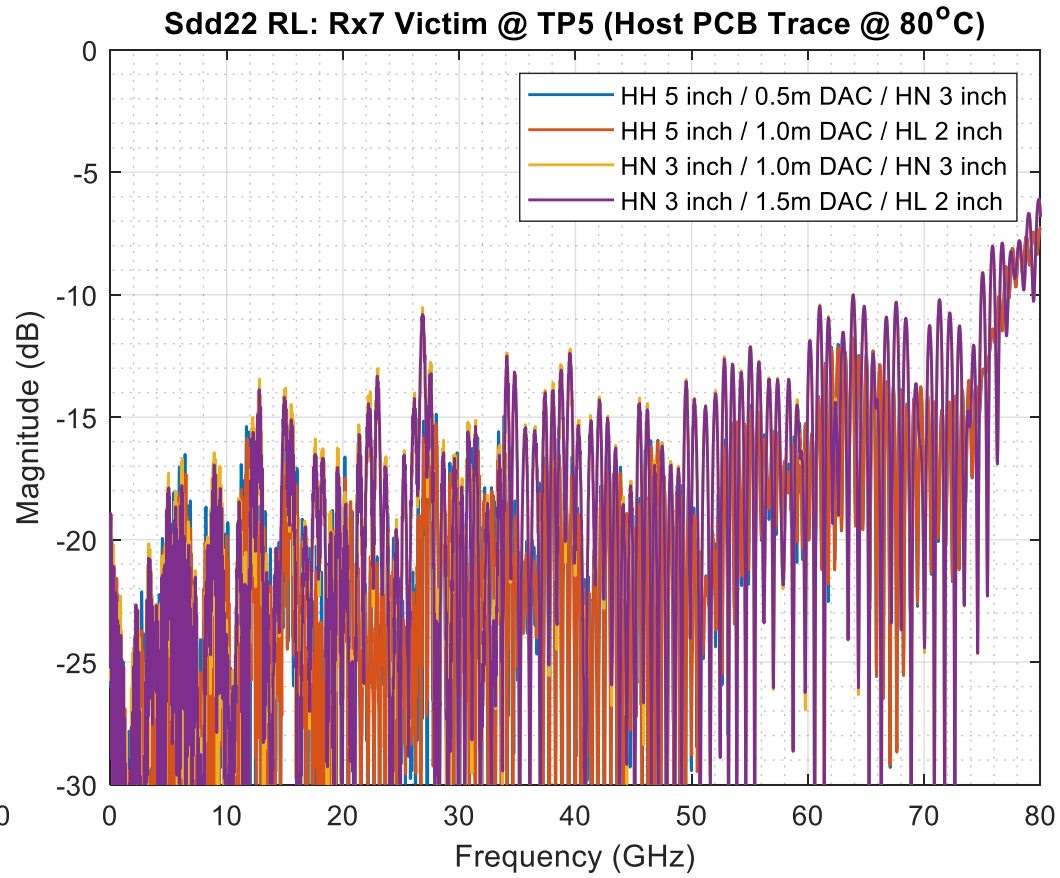
See slides 17-19 for full file names

Host 2 BGA Grid

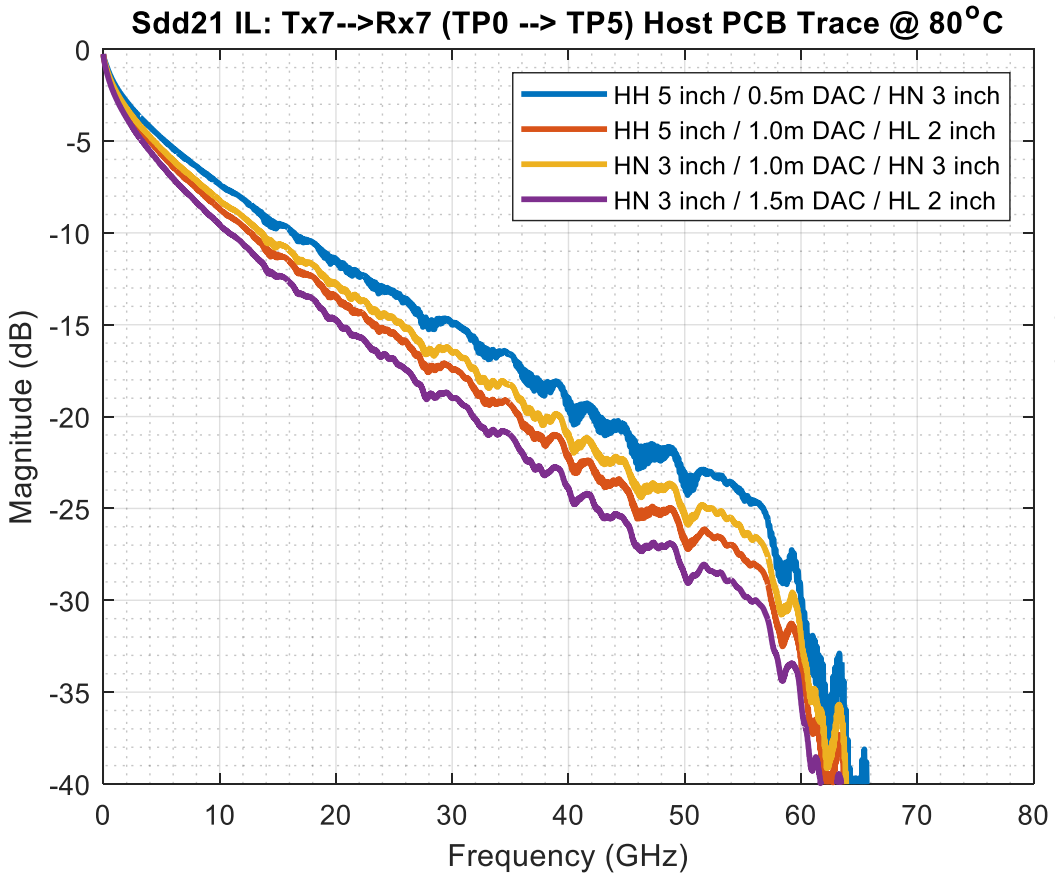


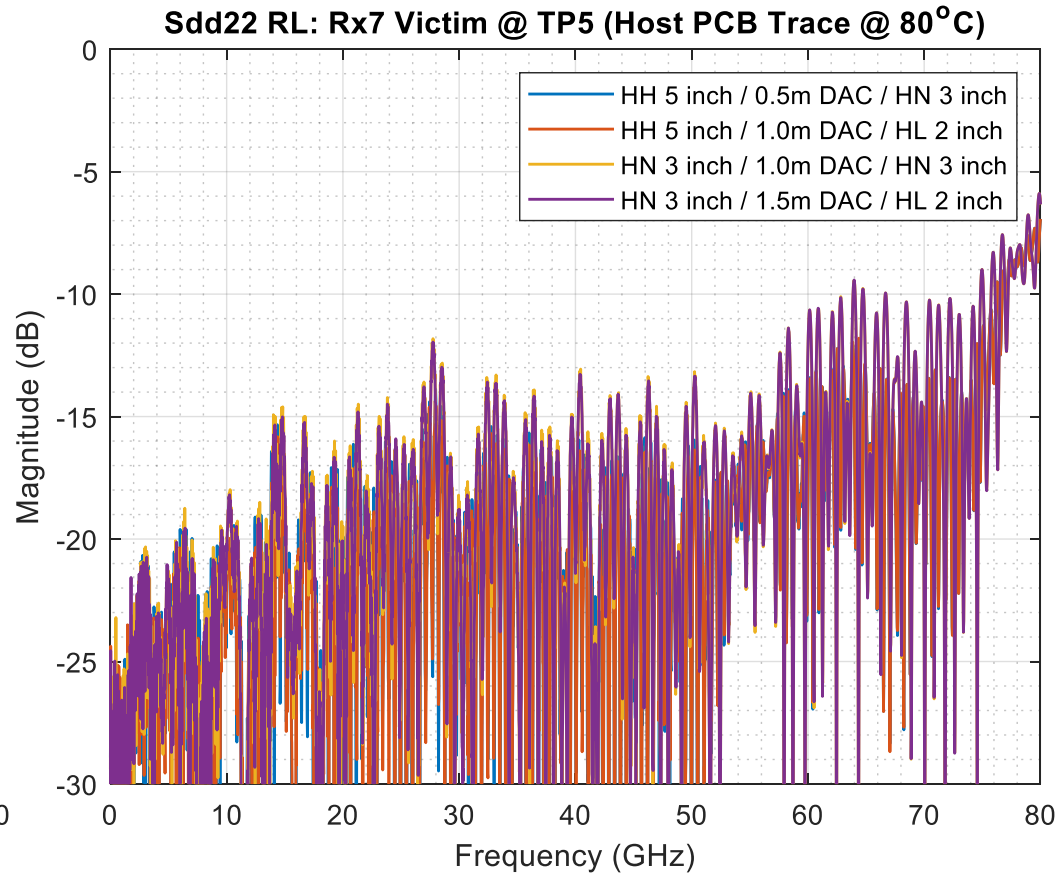
CR Channel Model with Vendor “X” OSFP DAC Cable Insertion/Return Loss vs. Host PCB Lengths



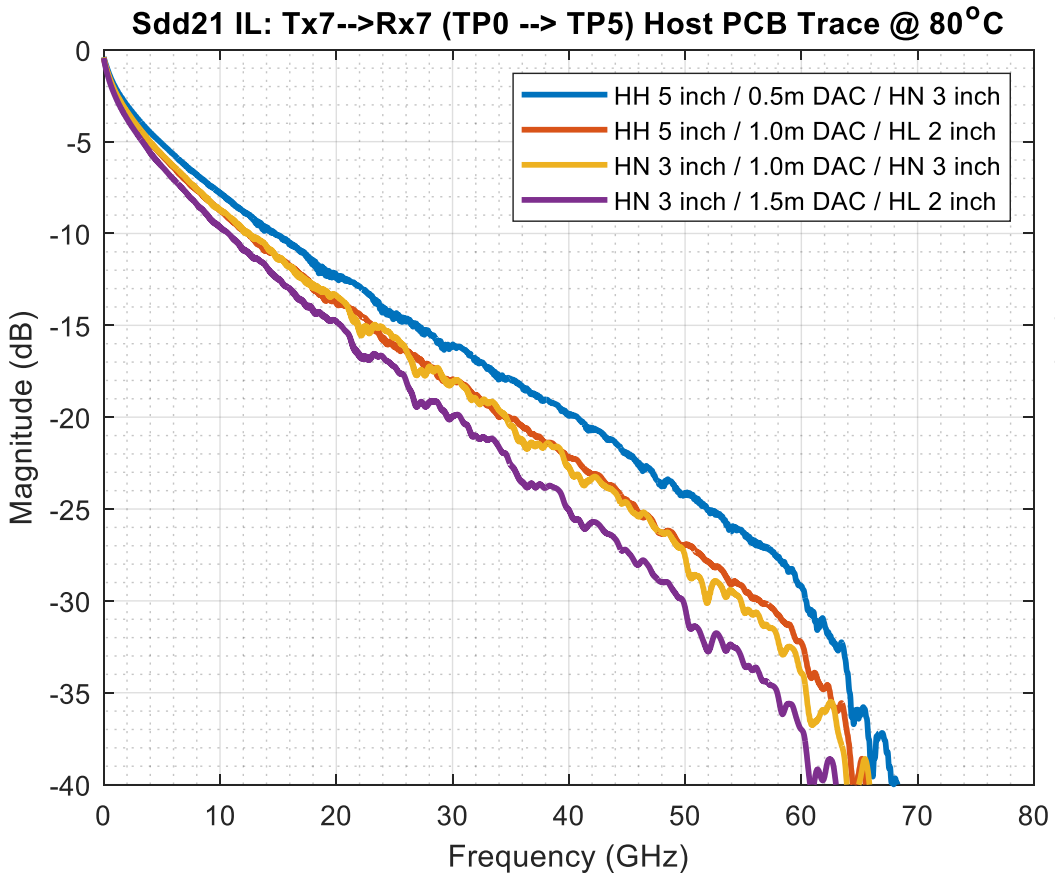


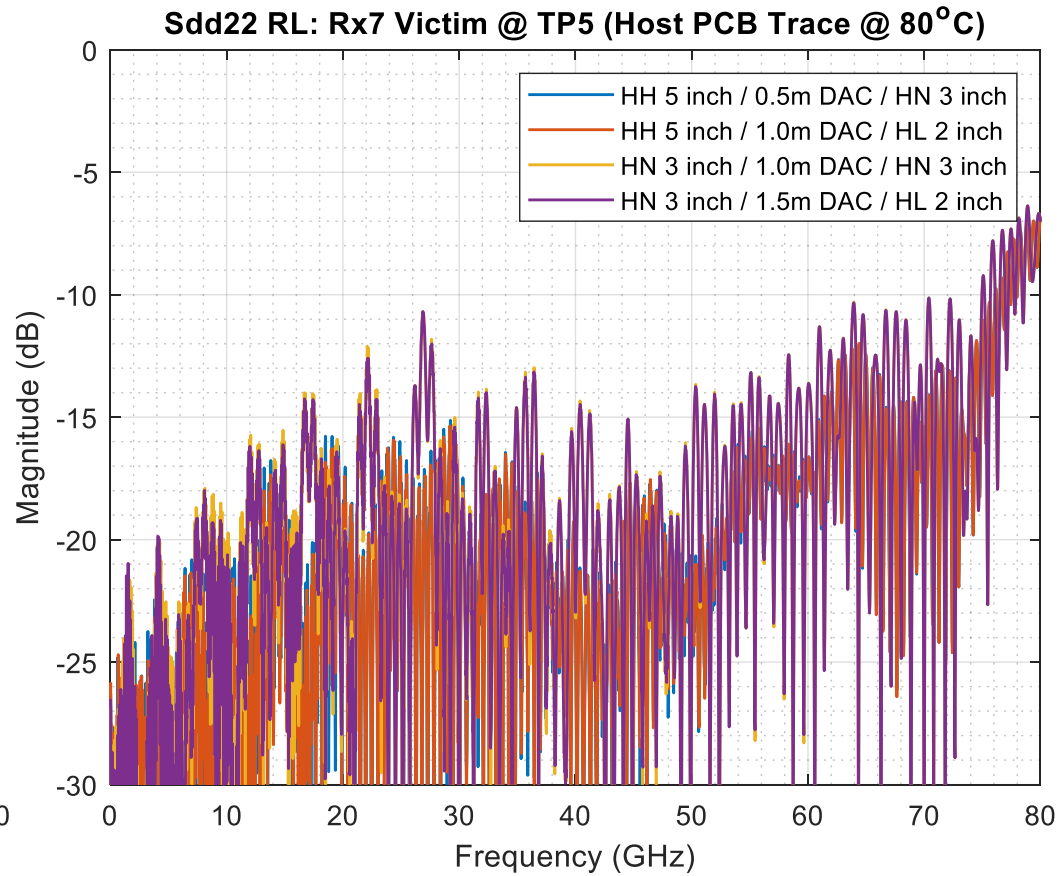
CR Channel Model with Vendor “Y” OSFP DAC Cable Insertion/Return Loss vs. Host PCB Lengths



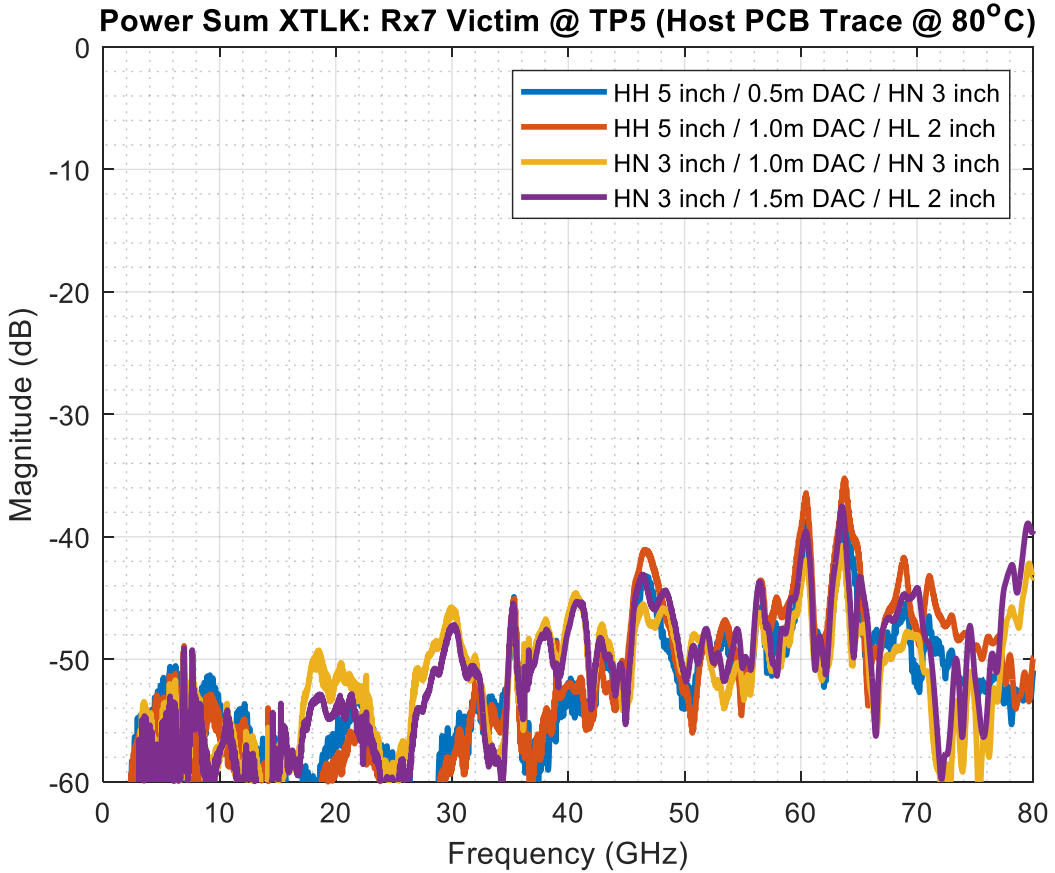


CR Channel Model with Vendor "Z" OSFP DAC Cable Insertion/Return Loss vs. Host PCB Lengths

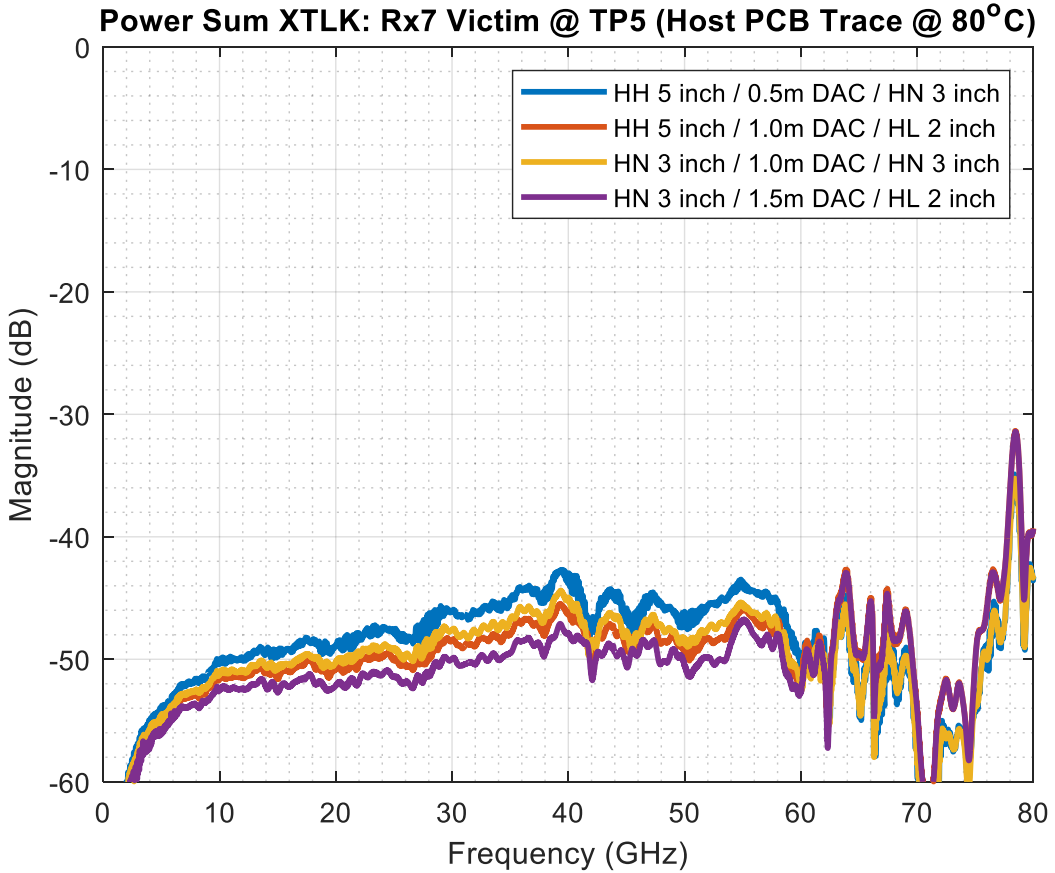




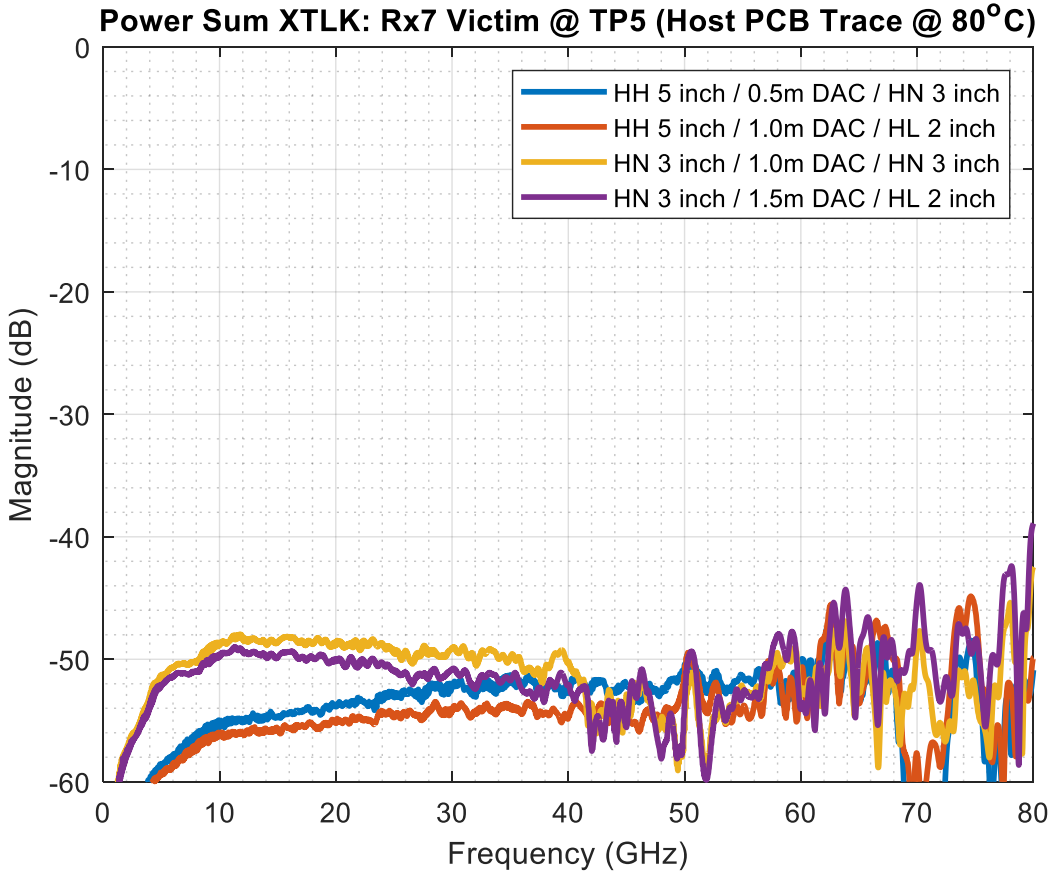
CR Channel Model with Vendor “X” OSFP DAC Cable
Power Sum XTLK vs. Host PCB Lengths



CR Channel Model with Vendor “Y” OSFP DAC Cable Insertion/Return Loss vs. Host PCB Lengths



CR Channel Model with Vendor “Z” OSFP DAC Cable Insertion/Return Loss vs. Host PCB Lengths



Summary

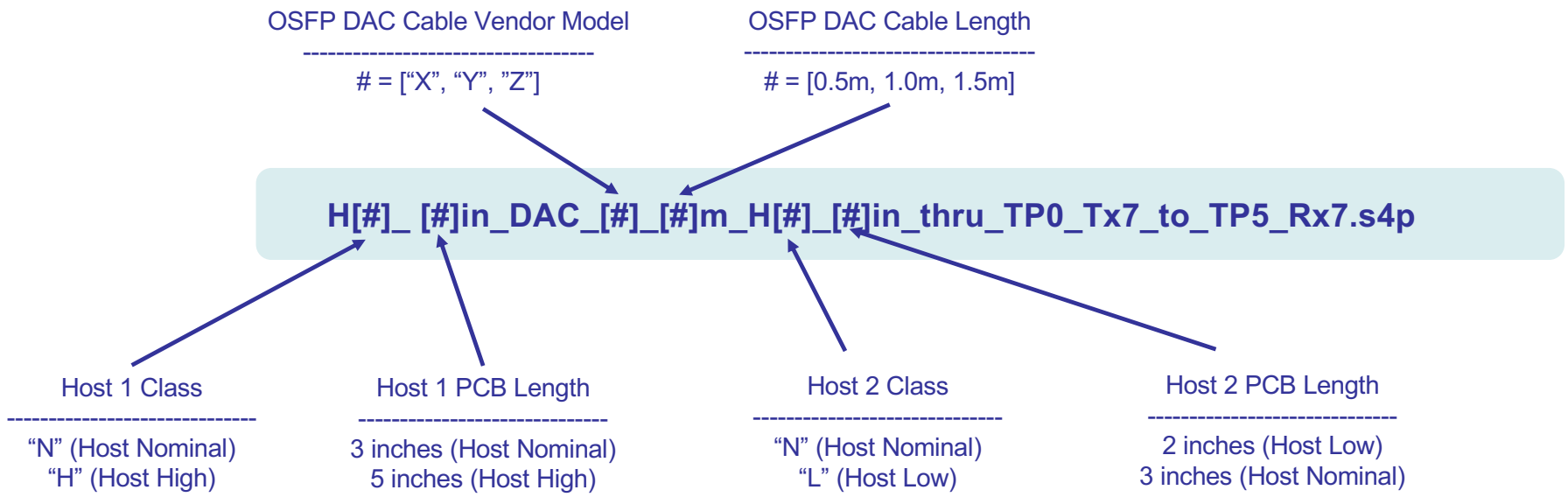
- Contributed CR channel models with OSFP DAC Cables

			TP0-TP5 Insertion Loss (dB) @53GHz		
Host #1	**Cable**	**Host #2**	**DAC 'X'**	**DAC 'Y'**	**DAC 'Z'**
HH (5" trace)	CA-A (0.5m)	HN (3" trace)	-25.35	-23.36	-25.45
HH (5" trace)	CA-B (1.0m)	HL (2" trace)	-27.73	-26.58	-28.33
HN (3" trace)	CA-B (1.0m)	HN (3" trace)	-29.54	-25.14	-29.23
HN (3" trace)	CA-C (1.5m)	HL (2" trace)	-31.66	-28.49	-32.16

- Each victim channel contains 6 signal lanes: 1 victim and 5 aggressors
- Return losses less than –10dB to ~60GHz
- Power summed XTLK is generally less than –40dB to ~60GHz

CR Channels

File Naming Convention: TP0→TP5 Thru Channels



CR Channels

Thru Channel Files: OSFP DAC Cable Vendor: ### = [X, Y, Z]

HH_5in_DAC_###_0p5m_HN_3in_thru_TP0_Tx7_to_TP5_Rx7.s4p
HH_5in_DAC_###_1p0m_HL_2in_thru_TP0_Tx7_to_TP5_Rx7.s4p
HN_3in_DAC_###_1p0m_HN_3in_thru_TP0_Tx7_to_TP5_Rx7.s4p
HN_3in_DAC_###_1p5m_HL_2in_thru_TP0_Tx7_to_TP5_Rx7.s4p

CR Channels

File Naming Convention: TP0→TP5 FEXT Channels

OSFP DAC Cable Vendor Model

= [“X”, “Y”, ”Z”]

OSFP DAC Cable Length

= [0.5m, 1.0m, 1.5m]

Far-End Aggressor Source on Host 1

= [5, 6, 8]

H[#]_ [#]in_DAC_[#]_[#]m_H[#]_[#]in_FEXT_TP0_Tx[#]_to_TP5_Rx7.s4p

Host 1 Class

“N” (Host Nominal)
“H” (Host High)

Host 1 PCB Length
---
3 inches (Host Nominal)
5 inches (Host High)

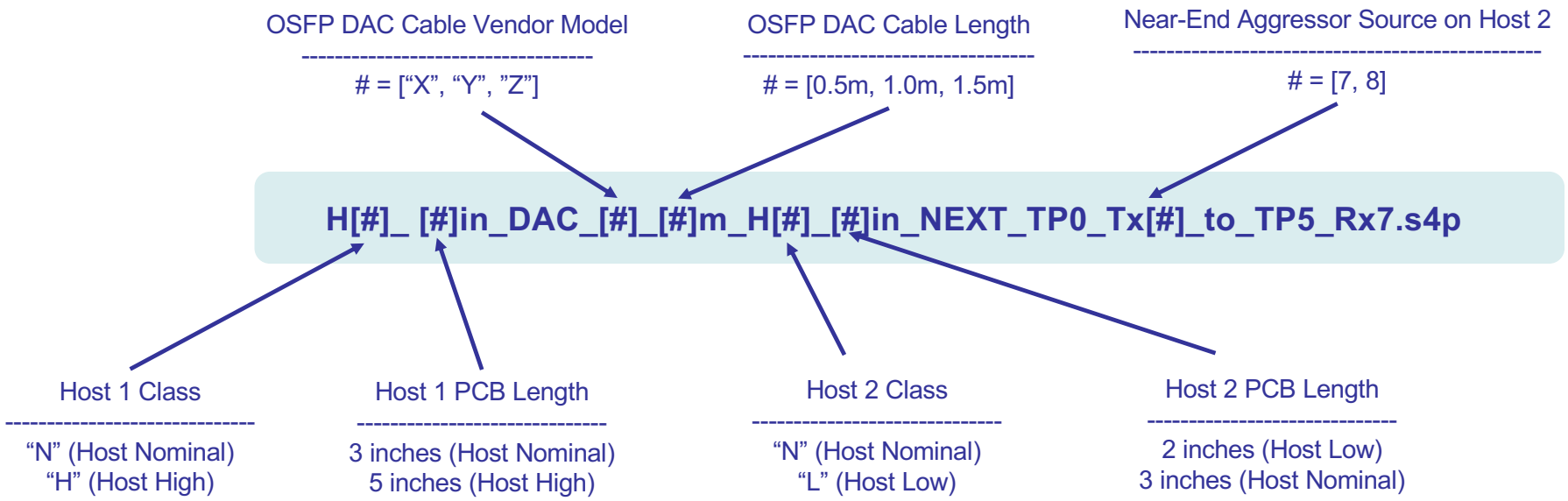
Host 2 Class

“N” (Host Nominal)
“L” (Host Low)

Host 2 PCB Length
---
2 inches (Host Low)
3 inches (Host Nominal)

CR Channels

File Naming Convention: TP0→TP5 NEXT Channels



CR Channels

XTLK Channel Files:

OSFP DAC Cable Vendor: ### = [X, Y, Z]

HH - 0.5m DAC - HN

HH_5in_DAC_###_0p5m_HN_3in_FEXT_TP0_Tx5_to_TP5_Rx7.s4p
HH_5in_DAC_###_0p5m_HN_3in_FEXT_TP0_Tx6_to_TP5_Rx7.s4p
HH_5in_DAC_###_0p5m_HN_3in_FEXT_TP0_Tx8_to_TP5_Rx7.s4p
HH_5in_DAC_###_0p5m_HN_3in_NEXT_TP0_Tx7_to_TP5_Rx7.s4p
HH_5in_DAC_###_0p5m_HN_3in_NEXT_TP0_Tx8_to_TP5_Tx7.s4p

HN - 1.0m DAC - HN

HN_3in_DAC_###_1p0m_HN_3in_FEXT_TP0_Tx5_to_TP5_Rx7.s4p
HN_3in_DAC_###_1p0m_HN_3in_FEXT_TP0_Tx6_to_TP5_Rx7.s4p
HN_3in_DAC_###_1p0m_HN_3in_FEXT_TP0_Tx8_to_TP5_Rx7.s4p
HN_3in_DAC_###_1p0m_HN_3in_NEXT_TP0_Tx7_to_TP5_Rx7.s4p
HN_3in_DAC_###_1p0m_HN_3in_NEXT_TP0_Tx8_to_TP5_Rx7.s4p

HH - 1.0m DAC - HL

HH_5in_DAC_###_1p0m_HL_2in_FEXT_TP0_Tx5_to_TP5_Rx7.s4p
HH_5in_DAC_###_1p0m_HL_2in_FEXT_TP0_Tx6_to_TP5_Rx7.s4p
HH_5in_DAC_###_1p0m_HL_2in_FEXT_TP0_Tx8_to_TP5_Rx7.s4p
HH_5in_DAC_###_1p0m_HL_2in_NEXT_TP0_Tx7_to_TP5_Rx7.s4p
HH_5in_DAC_###_1p0m_HL_2in_NEXT_TP0_Tx8_to_TP5_Tx7.s4p

HN - 1.5m DAC - HL

HN_3in_DAC_###_1p5m_HL_2in_FEXT_TP0_Tx5_to_TP5_Rx7.s4p
HN_3in_DAC_###_1p5m_HL_2in_FEXT_TP0_Tx6_to_TP5_Rx7.s4p
HN_3in_DAC_###_1p5m_HL_2in_FEXT_TP0_Tx8_to_TP5_Rx7.s4p
HN_3in_DAC_###_1p5m_HL_2in_NEXT_TP0_Tx7_to_TP5_Rx7.s4p
HN_3in_DAC_###_1p5m_HL_2in_NEXT_TP0_Tx8_to_TP5_Tx7.s4p