212Gb/s Per Lane PAM4 CR Channels with Flexible Host Architectures and Longer Reach Cables - Switch Perspective

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Overview

- This is a preliminary investigation into a typical CR implementation
- The intent is to facilitate early discussion among participants using realizable channels
  - PCB trace s-parameter data measurement procedure similar to Delta-L but using AFR
  - All PCB footprints designed using HFSS and conform to the DFM rules of major fabricators
- These models are ball-to-ball to allow use with different package models
  - Bump-to-bump channel specification is still critical, owing to large package losses
- Development is continuing, so all models are subject to continuous refinement.
  - New channels will be contributed as refinements are made
Description

- Simulation of a typical host-to-host CR architecture over various trace lengths where one of the hosts is representative of a large switch
  - For NIC perspective, please reference akinwale_3dj_01_2311

- **Composition:**
  - BGA / PCB trace / OSFP via escapes simulated with HFSS
  - OSFP DAC cable assembly models with mated connectors provided by 3 vendors

- **Ball-to-Ball topology:** does not include package effects

- This presentation does NOT propose the following:
  - Specific aggregate losses
  - Specific host architecture implementations
### PCB Composition

- **BGA & OSFP Breakout Footprints**
  - ~3mm worst-case PTH breakout depth
  - 8 mil vias with 5 mil stubs
  - Conforms to current PCB fab design rules
  - Nothing exotic: no skip layers, no microvias

- **Host Breakout Trace**
  - Fanout lengths to OSFP vias: 2, 3, 5 inches
  - Losses @Hi Temp: ~1.40 dB/in @ 53.125 GHz
  - 90 ohm @ 6 mil line width

### DAC cable Composition

- **OSFP 1x1 SMT Connector with DAC 26AWG cable**
  - Vendors “X”, “Y”, “Z”
  - Room Temperature only models
  - Cable Lengths: 0.5m, 1.0m, 1.5m @ 26AWG
  - Integrated DAC cable assembly models includes
    - OSFP 1x1 connectors with mated module PCB’s
    - Cable attachment assemblies
    - 26AWG twinax cables
      - Vendor ‘X’: 100 ohms
      - Vendor ‘Y’: 95 ohms
      - Vendor ‘Z’: 92 ohms
Asymmetric Host / Cable Combos

<table>
<thead>
<tr>
<th>Host #1 PCB Trace</th>
<th>Cable</th>
<th>Host #2 PCB Trace</th>
</tr>
</thead>
<tbody>
<tr>
<td>HH (5 inch)</td>
<td>0.5m</td>
<td>HN (3 inch)</td>
</tr>
<tr>
<td>HH (5 inch)</td>
<td>1.0m</td>
<td>HL (2 inch)</td>
</tr>
<tr>
<td>HN (3 inch)</td>
<td>1.0m</td>
<td>HN (3 inch)</td>
</tr>
<tr>
<td>HN (3 inch)</td>
<td>1.5m</td>
<td>HL (2 inch)</td>
</tr>
</tbody>
</table>
Signaling Topology

Vendor-provided DAC cable assembly models limited to the above available ports

To include the “virtual” FEXT/NEXT from BGA signal balls Tx8a and Tx7a instantiate two copies of the following:

- **Tx8a**: “...FEXT_TP0_Tx8_to_TP5_Rx7.s4p”
- **Tx7a**: “...NEXT_TP0_Tx7_to_TP5_Rx7.s4p”

*See slides 17-19 for full file names*
CR Channel Model with Vendor “X” OSFP DAC Cable
Insertion/Return Loss vs. Host PCB Lengths
CR Channel Model with Vendor “Y” OSFP DAC Cable Insertion/Return Loss vs. Host PCB Lengths
CR Channel Model with Vendor “Z” OSFP DAC Cable
Insertion/Return Loss vs. Host PCB Lengths

Sdd21 IL: Tx7→Rx7 (TP0 ↔ TP5) Host PCB Trace @ 80°C

Sdd22 RL: Rx7 Victim @ TP5 (Host PCB Trace @ 80°C)
CR Channel Model with Vendor “X” OSFP DAC Cable
Power Sum XTLK vs. Host PCB Lengths
CR Channel Model with Vendor “Y” OSFP DAC Cable
Insertion/Return Loss vs. Host PCB Lengths
CR Channel Model with Vendor “Z” OSFP DAC Cable Insertion/Return Loss vs. Host PCB Lengths
Summary

- Contributed CR channel models with OSFP DAC Cables

<table>
<thead>
<tr>
<th>Host #1</th>
<th>Cable</th>
<th>Host #2</th>
<th>DAC 'X'</th>
<th>DAC 'Y'</th>
<th>DAC 'Z'</th>
</tr>
</thead>
<tbody>
<tr>
<td>HH (5&quot; trace)</td>
<td>CA-A (0.5m)</td>
<td>HN (3&quot; trace)</td>
<td>-25.35</td>
<td>-23.36</td>
<td>-25.45</td>
</tr>
<tr>
<td>HH (5&quot; trace)</td>
<td>CA-B (1.0m)</td>
<td>HL (2&quot; trace)</td>
<td>-27.73</td>
<td>-26.58</td>
<td>-28.33</td>
</tr>
<tr>
<td>HN (3&quot; trace)</td>
<td>CA-B (1.0m)</td>
<td>HN (3&quot; trace)</td>
<td>-29.54</td>
<td>-25.14</td>
<td>-29.23</td>
</tr>
<tr>
<td>HN (3&quot; trace)</td>
<td>CA-C (1.5m)</td>
<td>HL (2&quot; trace)</td>
<td>-31.66</td>
<td>-28.49</td>
<td>-32.16</td>
</tr>
</tbody>
</table>

- Each victim channel contains 6 signal lanes: 1 victim and 5 aggressors
- Return losses less than –10dB to ~60GHz
- Power summed XTLK is generally less than –40dB to ~60GHz
CR Channels

File Naming Convention: TP0→TP5 Thru Channels

```
H[#]_ [#]in_DAC_[#]_[#]m_H[#]_[#]m_thru_TP0_Tx7_to_TP5_Rx7.s4p
```

- **OSFP DAC Cable Vendor Model**
  - # = ["X", "Y", "Z"]
- **OSFP DAC Cable Length**
  - # = [0.5m, 1.0m, 1.5m]

- **Host 1 Class**
  - "N" (Host Nominal)
  - "H" (Host High)
- **Host 1 PCB Length**
  - 3 inches (Host Nominal)
  - 5 inches (Host High)

- **Host 2 Class**
  - "N" (Host Nominal)
  - "L" (Host Low)
- **Host 2 PCB Length**
  - 2 inches (Host Low)
  - 3 inches (Host Nominal)
CR Channels

**Thru Channel Files:** OSFP DAC Cable Vendor: ### = [X, Y, Z]

HH_5in_DAC_###_0p5m_HN_3in_thru_TP0_Tx7_to_TP5_Rx7.s4p
HH_5in_DAC_###_1p0m_HL_2in_thru_TP0_Tx7_to_TP5_Rx7.s4p
HN_3in_DAC_###_1p0m_HN_3in_thru_TP0_Tx7_to_TP5_Rx7.s4p
HN_3in_DAC_###_1p5m_HL_2in_thru_TP0_Tx7_to_TP5_Rx7.s4p
CR Channels

File Naming Convention: TP0→TP5 FEXT Channels

- **OSFP DAC Cable Vendor Model**
  - # = ["X", "Y", "Z"]

- **OSFP DAC Cable Length**
  - # = [0.5m, 1.0m, 1.5m]

- **Far-End Aggressor Source on Host 1**
  - # = [5, 6, 8]

- **Host 1 PCB Length**
  - 3 inches (Host Nominal)
  - 5 inches (Host High)

- **Host 1 Class**
  - "N" (Host Nominal)
  - "H" (Host High)

- **Host 2 PCB Length**
  - 2 inches (Host Low)
  - 3 inches (Host Nominal)

- **Host 2 Class**
  - "N" (Host Nominal)
  - "L" (Host Low)

- **Host 1**

- **Port 1**
  - TP0

- **Port 2**
  - FEXT Channel

- **Port 3**

- **Port 4**
  - TP5

**File Name Template**

```
H[#]_[#]in_DAC_[#]_[#]m_H[#]_[#]in_FEXT_TP0_Tx[#]_to_TP5_Rx7.s4p
```
CR Channels

File Naming Convention: TP0→TP5 NEXT Channels

OSFP DAC Cable Vendor Model
# = ["X", "Y", "Z"]

OSFP DAC Cable Length
# = [0.5m, 1.0m, 1.5m]

Near-End Aggressor Source on Host 2
# = [7, 8]

H[#]_ [#]in_DAC_[#]_[#]m_H[#]_[#]in_NEXT_TP0_Tx[#]_to_TP5_Rx7.s4p

Host 1 Class
“N” (Host Nominal)
“H” (Host High)

Host 1 PCB Length
3 inches (Host Nominal)
5 inches (Host High)

Host 2 Class
“N” (Host Nominal)
“L” (Host Low)

Host 2 PCB Length
2 inches (Host Low)
3 inches (Host Nominal)

Port 1
TP0

Port 2
NEXXT Channel

Port 3

Port 4
TP5
CR Channels

**XTLK Channel Files:** OSFP DAC Cable Vendor: ### = [X, Y, Z]

### HH - 0.5m DAC - HN
- HH_5in_DAC_###_0p5m_HN_3in_FEXT_TP0_Tx5_to_TP5_Rx7.s4p
- HH_5in_DAC_###_0p5m_HN_3in_FEXT_TP0_Tx6_to_TP5_Rx7.s4p
- HH_5in_DAC_###_0p5m_HN_3in_FEXT_TP0_Tx8_to_TP5_Rx7.s4p
- HH_5in_DAC_###_0p5m_HN_3in_NEXT_TP0_Tx7_to_TP5_Rx7.s4p
- HH_5in_DAC_###_0p5m_HN_3in_NEXT_TP0_Tx8_to_TP5_Tx7.s4p

### HH - 1.0m DAC - HL
- HH_5in_DAC_###_1p0m_HL_2in_FEXT_TP0_Tx5_to_TP5_Rx7.s4p
- HH_5in_DAC_###_1p0m_HL_2in_FEXT_TP0_Tx6_to_TP5_Rx7.s4p
- HH_5in_DAC_###_1p0m_HL_2in_FEXT_TP0_Tx8_to_TP5_Rx7.s4p
- HH_5in_DAC_###_1p0m_HL_2in_NEXT_TP0_Tx7_to_TP5_Rx7.s4p
- HH_5in_DAC_###_1p0m_HL_2in_NEXT_TP0_Tx8_to_TP5_Tx7.s4p

### HH - 1.0m DAC - HN
- HH_5in_DAC_###_1p0m_HN_3in_FEXT_TP0_Tx5_to_TP5_Rx7.s4p
- HH_5in_DAC_###_1p0m_HN_3in_FEXT_TP0_Tx6_to_TP5_Rx7.s4p
- HH_5in_DAC_###_1p0m_HN_3in_FEXT_TP0_Tx8_to_TP5_Rx7.s4p
- HH_5in_DAC_###_1p0m_HN_3in_NEXT_TP0_Tx7_to_TP5_Rx7.s4p
- HH_5in_DAC_###_1p0m_HN_3in_NEXT_TP0_Tx8_to_TP5_Tx7.s4p

### HH - 1.5m DAC - HL
- HH_5in_DAC_###_1p5m_HL_2in_FEXT_TP0_Tx5_to_TP5_Rx7.s4p
- HH_5in_DAC_###_1p5m_HL_2in_FEXT_TP0_Tx6_to_TP5_Rx7.s4p
- HH_5in_DAC_###_1p5m_HL_2in_FEXT_TP0_Tx8_to_TP5_Rx7.s4p
- HH_5in_DAC_###_1p5m_HL_2in_NEXT_TP0_Tx7_to_TP5_Rx7.s4p
- HH_5in_DAC_###_1p5m_HL_2in_NEXT_TP0_Tx8_to_TP5_Tx7.s4p

### HH - 1.5m DAC - HN
- HH_5in_DAC_###_1p5m_HN_3in_FEXT_TP0_Tx5_to_TP5_Rx7.s4p
- HH_5in_DAC_###_1p5m_HN_3in_FEXT_TP0_Tx6_to_TP5_Rx7.s4p
- HH_5in_DAC_###_1p5m_HN_3in_FEXT_TP0_Tx8_to_TP5_Rx7.s4p
- HH_5in_DAC_###_1p5m_HN_3in_NEXT_TP0_Tx7_to_TP5_Rx7.s4p
- HH_5in_DAC_###_1p5m_HN_3in_NEXT_TP0_Tx8_to_TP5_Tx7.s4p