200G/L Technical Feasibility

Brian Welch (Cisco)

Vasu Parthasarathy (Broadcom)

Contributors and Supporters

- Dirk Lutz (Eoptolink)
- Mark Gustlin (Cisco)
- Jim Theodoras (HG Genuine)
- Piers Dawe (Nvidia)
- John Johnson (Broadcom)
- Vishnu Balan (Nvidia)
- Zvi Rechtman (Nvidia)
- Craig Thompson (Nvidia)
- Sridhar Ramesh (Maxlinear)

Intentions

- Intent of this presentation is to explore (and hopefully establish) technical feasibility for 200G/L IMDD at 500m and 2km.
  - Exploration includes technical feasibility of both FECo and FECi.

- 10km is not considered except as a point of comparison for 500m and 2km.
  - Although it is likely that much of the work here would indirectly bolster confidence in 10km performance.

Overview

- Chapter I: Comparisons between 200G/L proposals
  - How do the proposed requirements compare across different 200G/L IMDD proposals?
- Chapter II: History of 100G/L
  - What were expectations of 100G/L when we adopted baselines?
  - How did 100G/L mature as products came to market?
- Chapter III: 200G/L measurements and analyses
  - What do 200G/L measurements say today?
  - How does this compare to 100G/L at the same point in task force?

Chapter I

Comparisons between 200G/L proposals

Comparisons between 200G/L proposals

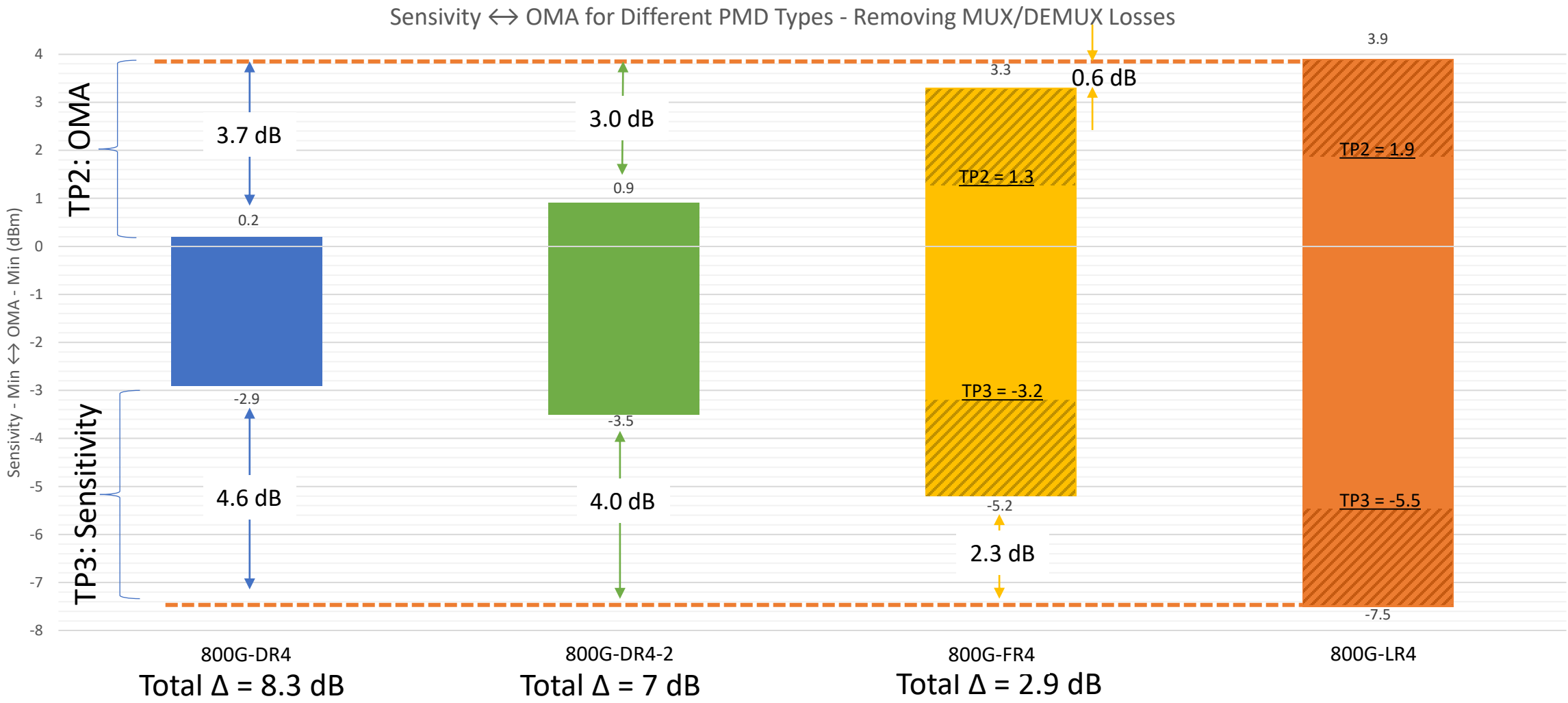
- Optical performance requirements, for transmitter and receiver, generally get more stringent for longer reach standards. This is a function of:
  - Increased fiber plant loss and penalties
  - Mux/Demux loss for multi-wavelength solutions

- Taken together, the difference in optical requirements for 10km, 2km, and 500m proposal is considerable.
  - Up to 4.6 dB difference in receiver sensitivity specifications
  - Up to 3.7 dB difference in transmitter OMA specifications

FR4/LR4 assumes 2dB loss for CWDM/LWDM Mux and Demux

Compares baseline proposals from September Task Force Meeting

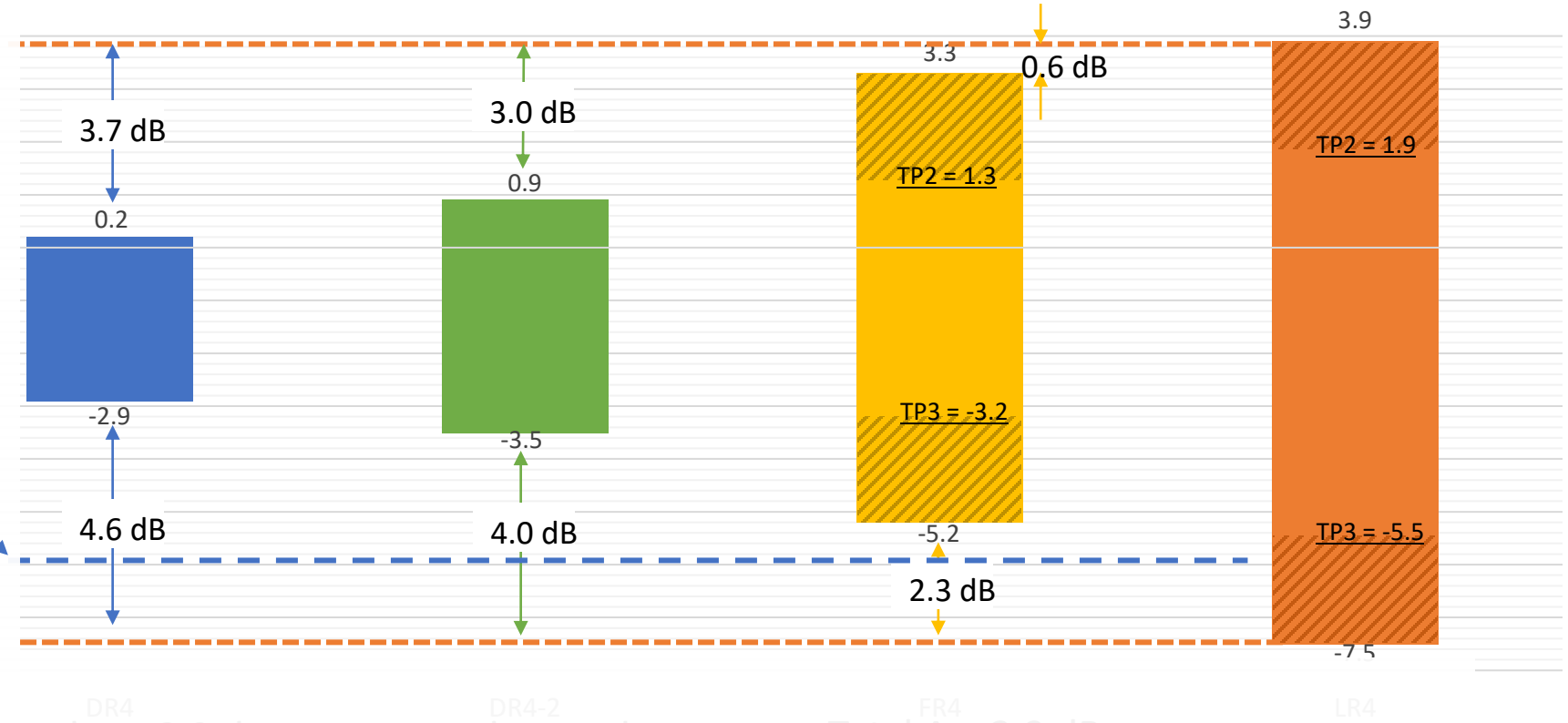
Comparisons between 200G/L proposals



What does this show?

Approx FECo sensitivity assuming ~1.5dB reduction in net coding gain

FECi sensitivity for LR4



1st order assessment: If LR4 links are feasible using FECi, then shorter distances with relaxed link budgets should be feasible with FECo.

Comparisons between 200G/L proposals

- Presently, the same FECi is proposed for all 200G/L PMD types.
  - The FECi SD net coding gain has been indicated to be around 1.5 dB (parthasarathy_3dj_01_2303.pdf)

- For reaches less than 10km, the relative relaxation in the receiver sensitivity (Rx Sens.) and link budget exceeds the additional 1.5 dB coding gain of the FECi.

800G-LR4 vs	Rx Sens difference (dB)	Overall Link budget difference (TP2-TP3) [dB]
800G-FR4	~2.3	2.9
800G-DR4-2	~4.0	7
800G-DR4	~4.6	8.3

- Technical feasibility for 800G-LR4 with FECi indicates technical feasibility probable for all other 200G/L PMD types likely with FECo

Chapter II

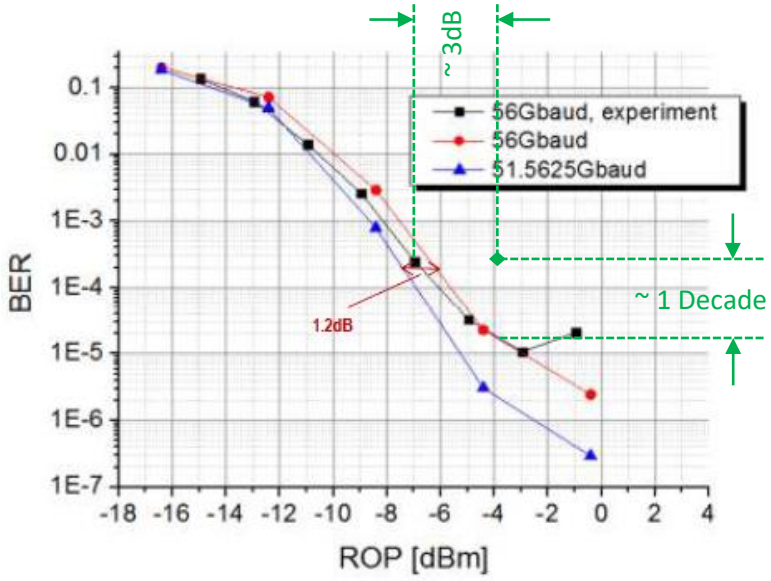
History of 100G/L

History of 100G/L

- Baseline for 400GBASE-DR4 (first 100G/L standard) was adopted in July 2015
- Prior to adoption measurement results had been shared in way_3bs_01a_0115.pdf and conroy_3bs_01b_0515.pdf
- Measurements showed ~ 2-3 dB of sensitivity margin, ~1 decade of BER margin (see next slide)
  - Margin measured to unstressed sensitivity value; stressed margin would be higher.
- **Considerable improvements in sensitivity and BER were achieved with production modules (following slides).**

Evolution of 100G/L: Pre-Standard (2015)

56 → 51.5625Gbaud: Receiver Sensitivity Improvement



Baud rate = 56Gbaud or 51.5625Gbaud

DAC 3dB BW=16.5GHz, 2nd order Bessel for DAC

TX linear AMP BW=30GHz

EML BW=32GHz

SNR before E/O =22.5dB, ER=6dB

RIN=-145dB/Hz

RX input noise density=30pA/Hz^(1/2)

PD+TIA BW=32GHz, PD responsivity=0.75, 400Ohm transimpedance

5th-order Bessel approximation of Tx amp, E/O, PD+TIA

5 bits A/D ENOB, 5th order Bessel A/D, 20GHz BW A/D

19 taps pre-correction T-spaced, 21-taps FFE Rx T/2-spaced

Receiver sensitivity improved by 1.2dB @ BER=2.1e-4 when the baud rate is lowered from 56 to 51.5625Gbaud

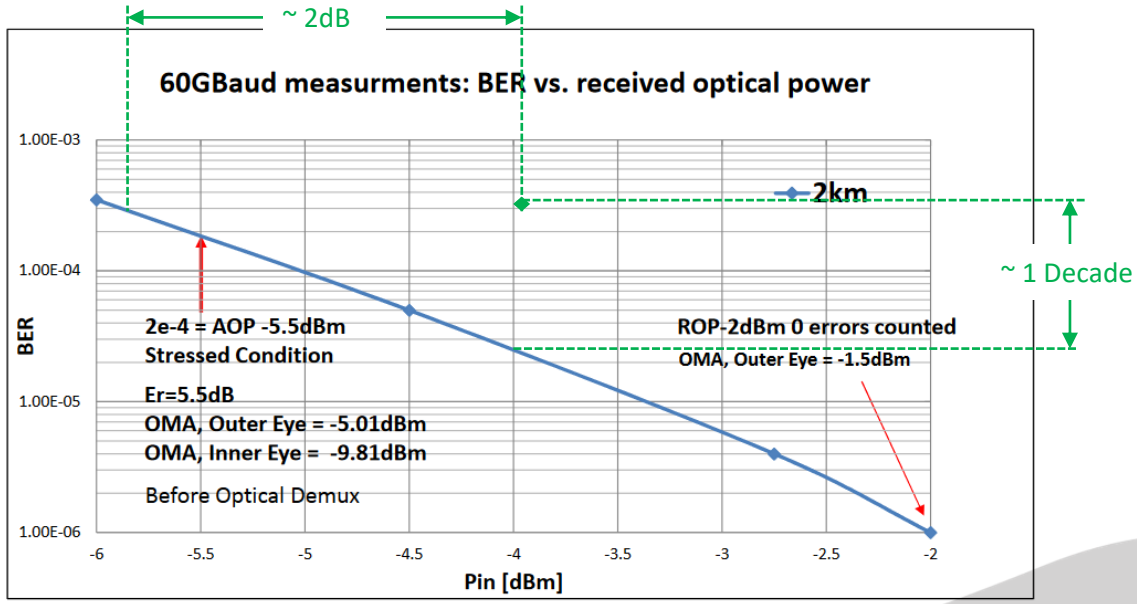
9

NeoPhotonics

Measured BER vs. RX AOP – MZM 1550nm

RX AOP Range (-2dBm to -6dBm)

Er = 5.5dB
Measure @1/4BR



Noise Density = 30pA, CD =34ps/nm and Baud Rate =60GB

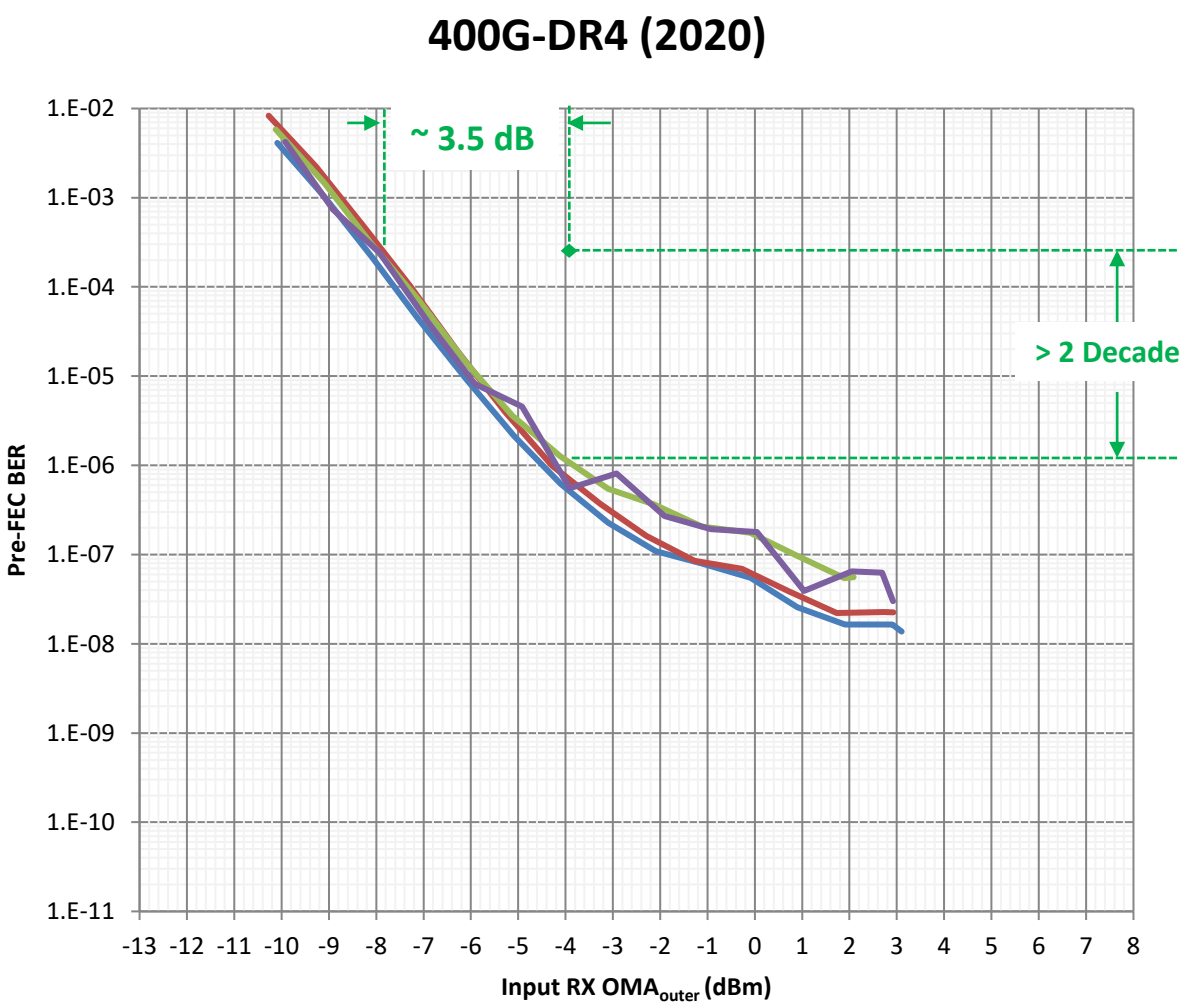
6

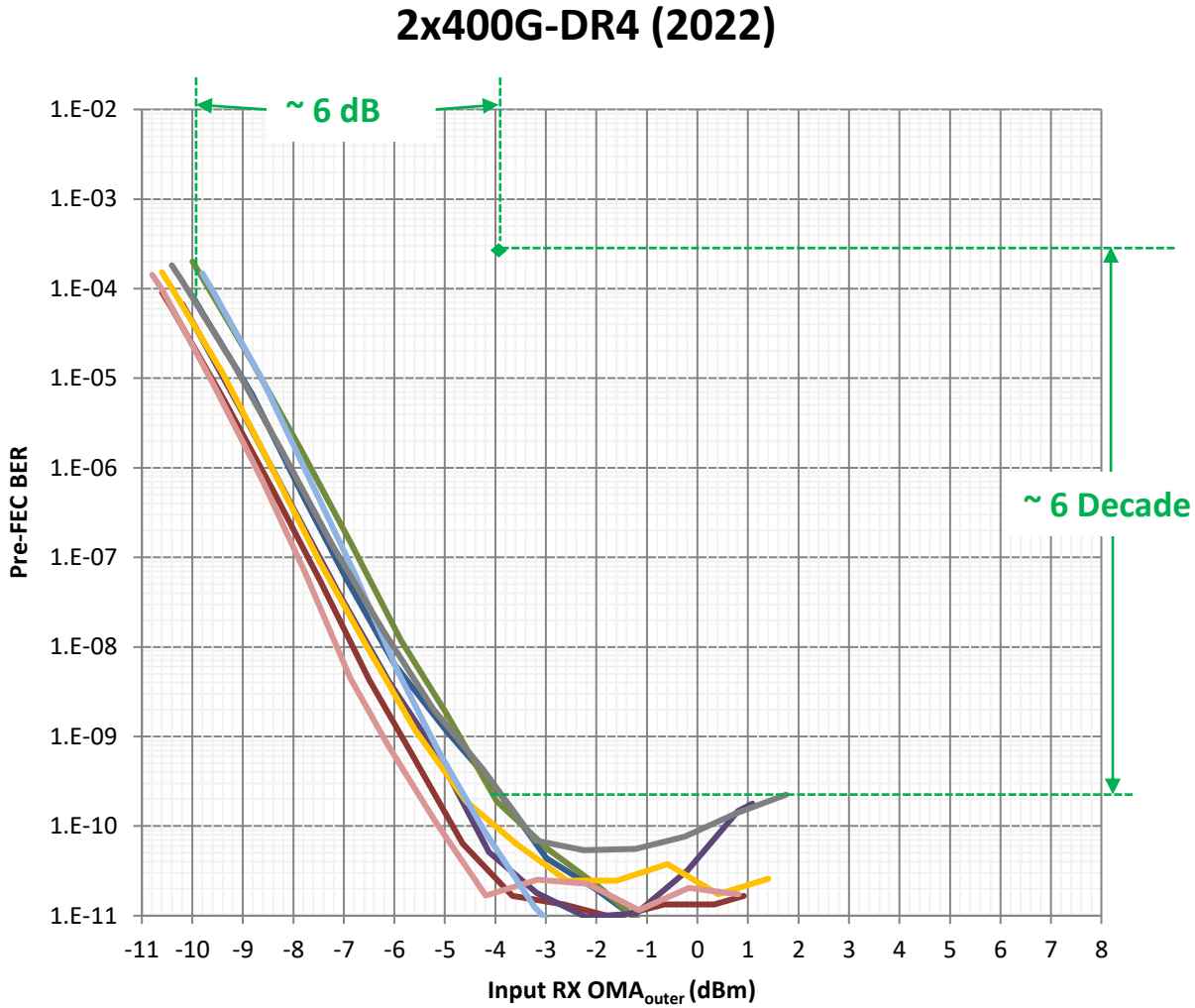
IEEE 802.3bs Task Force May 2015

way_3bs_01a_0115.pdf

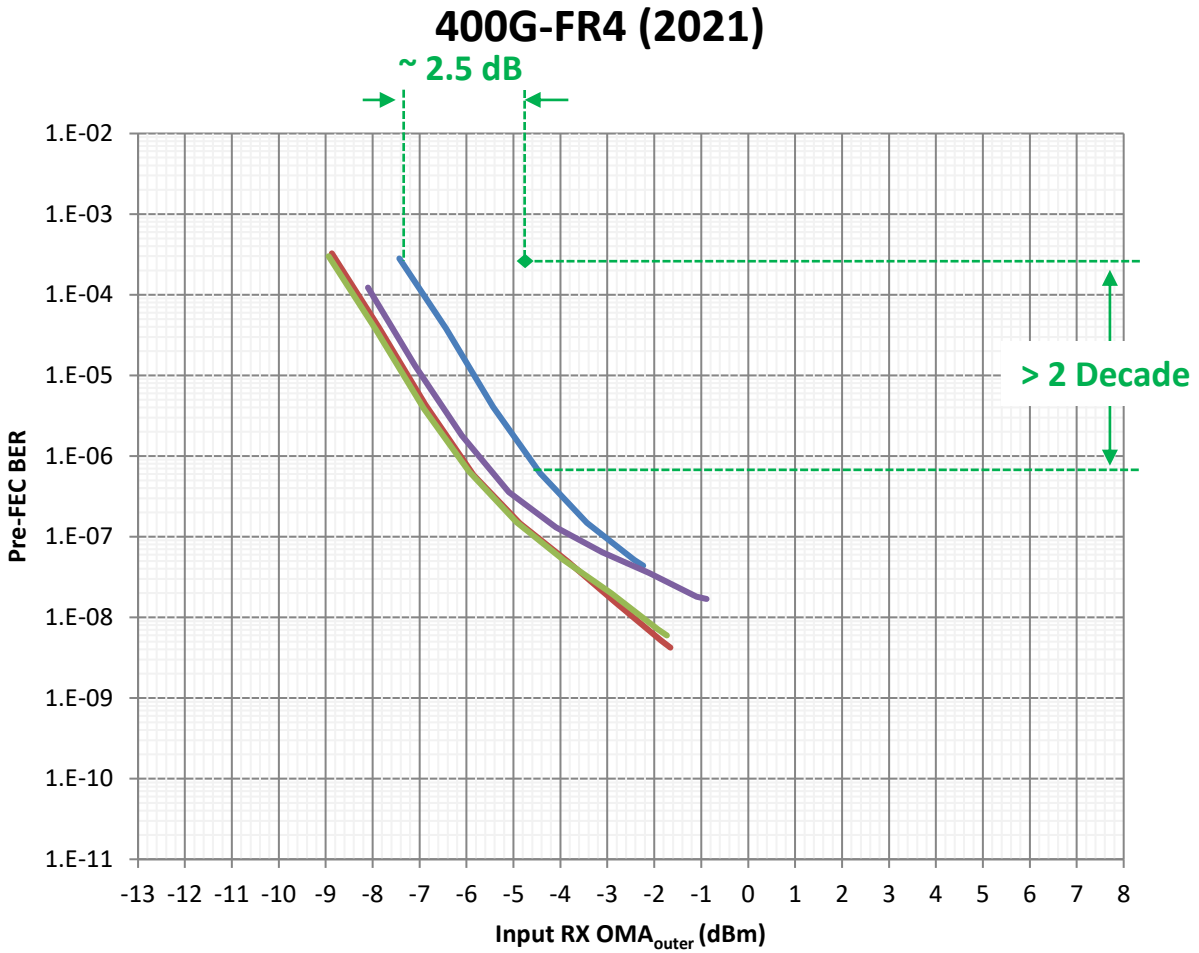
conroy_3bs_01b_0515.pdf

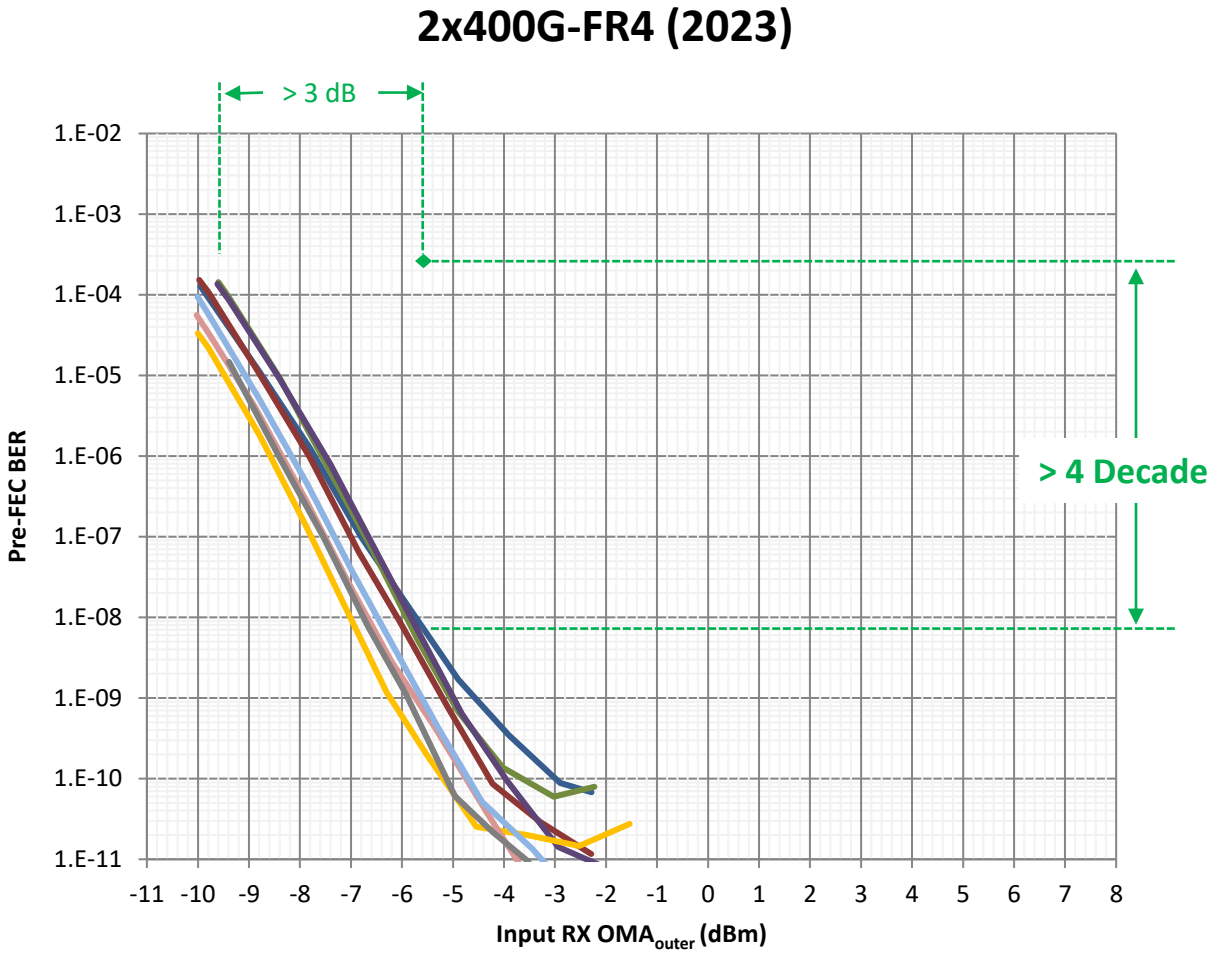
Evolution of 100G/L: Early 400G-DR4 Production





Evolution of 100G/L: Early 400G-FR4 Production

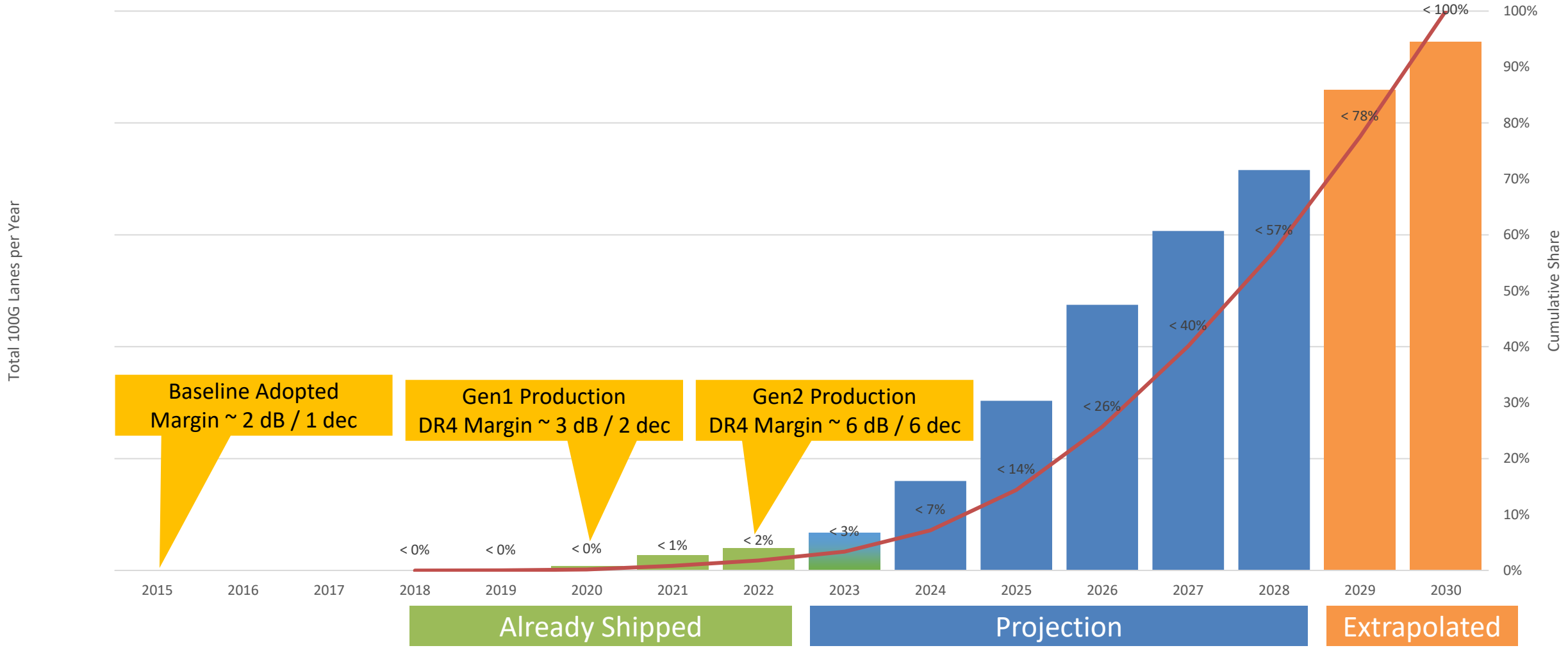




Data from LightCounting Sept 2023 Report

Note: LightCounting reports do not break out 800G-DR8 and 800G-DR4 volumes separately. Here all 800G module volume is assumed 800G-DR8.

100G/L Technology & Market Evolution



Learnings from 100G/L

- At the time of first baseline adoption at 100G/L, there were few experimental results, and those that did exist showed little margin.
- Since that time margin has expanded rapidly, with over 6 dB & 6 decades of margin in more recent 100G/L optical modules
- Majority of the 100G/L market yet to come

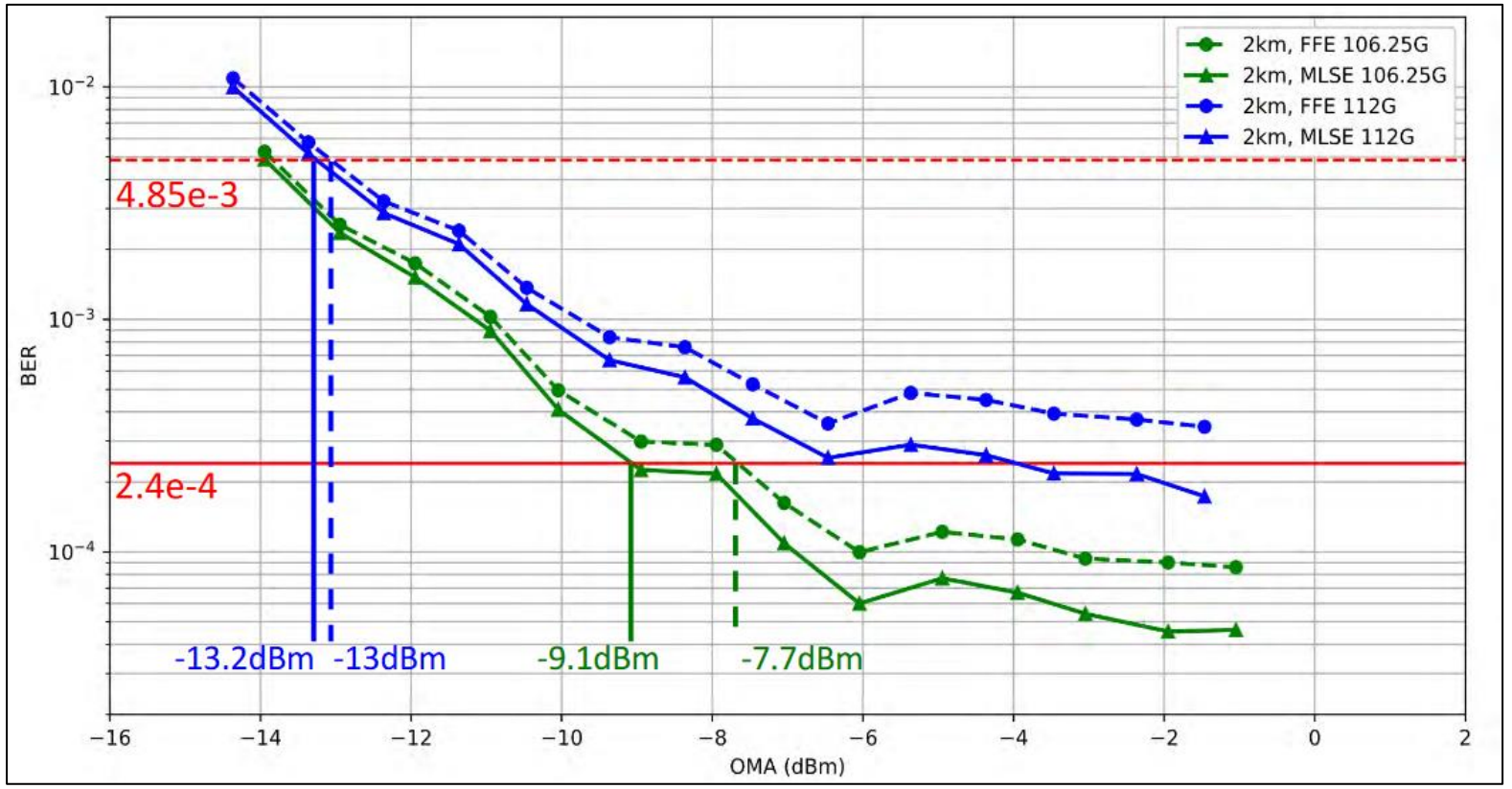
Chapter III

200G/L measurements and analyses

From li_3dj_01a_230206.pdf

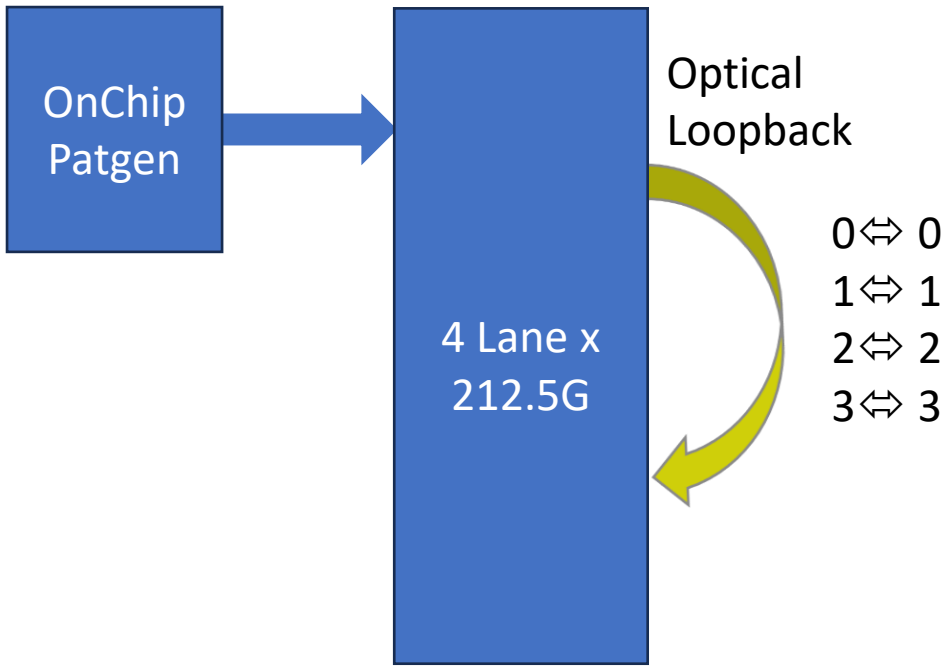
Evolution of 200G/L: Pre-Standard (Feb 2023)

- Earliest results showed feasibility
- Lab bench results consistent with pre-standard 100G/L experiments
- Narrow margins to error floors

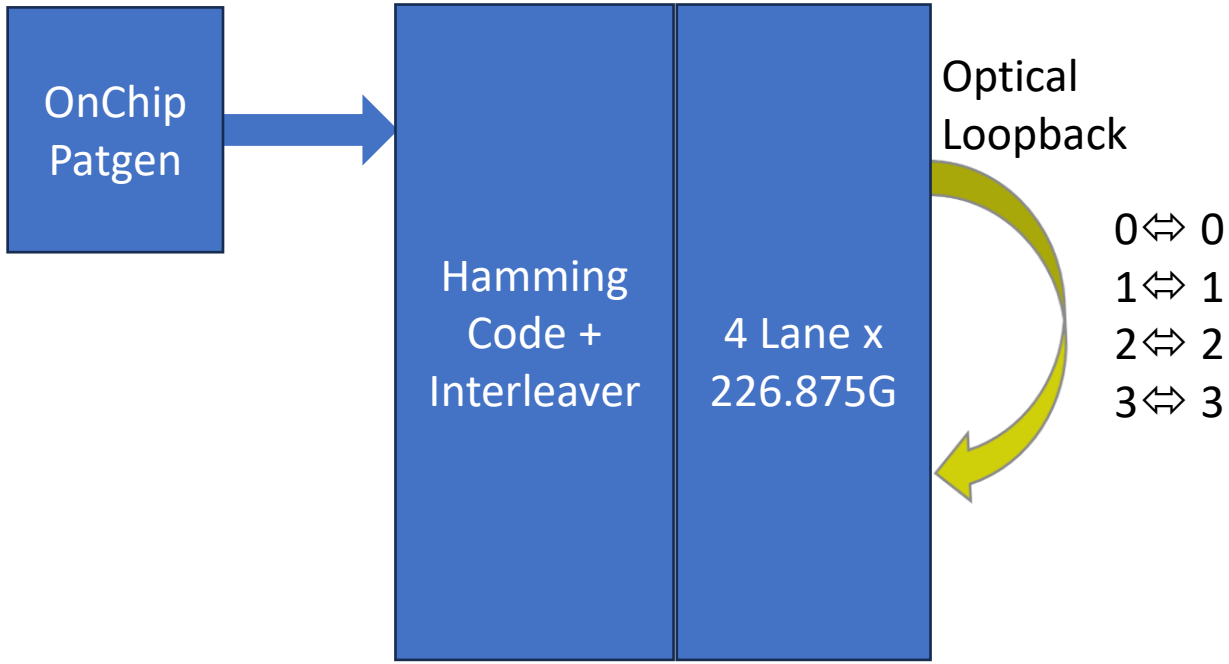


Evolution of 200G/L: Updated Pre-Standard (Nov 2023)

Early results from production-grade module with 8x100G to 4x200G DSP. Based on Monolithic 5nm CMOS (BCM85821* and BCM85822*)



Test Setup: FECo

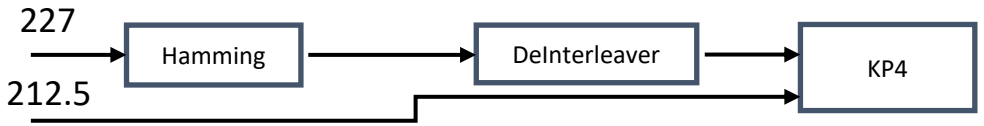


Test Setup: FECi

*https://www.broadcom.com/company/news/product-releases/61436

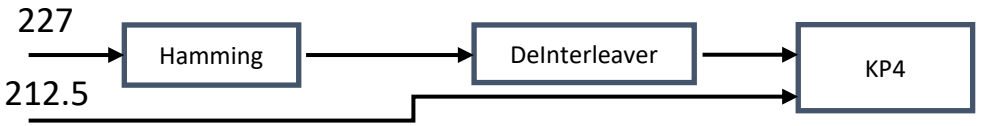
Evolution of 200G/L: Updated Pre-Standard (Nov 2023)

- https://www.broadcom.com/company/news/product-releases/61436
- Two separate module designs: Integrated Laser Driver (ILD) and External Laser Driver (ELD)
  - EML based module
  - Code/rate compliant to the IEEE standard
- Ten-minute evaluation in loopback condition at both 212.5 and 226.875Gbps
  - To arrive at performance limits: a) No crosstalk (single lane traffic) b) Room temperature c) Default OMA d) 11 tap TXFIR optimized for BER (while still getting acceptable TDECQ) e) Optical side only (no electrical interface) f) Single module result (randomly picked)



Module Type	Rate	PreHamming BER	preKP4 BER	Max KP4 correction
ELD	212.5	n/a	8e-9	3
ELD	226.875	< 3e-6	1.5e-11	2
ILD	212.5	n/a	2e-9	2
ILD	226.875	<3e-6	7e-12	2

Evolution of 200G/L: Updated Pre-Standard (Nov 2023)



Power evaluation

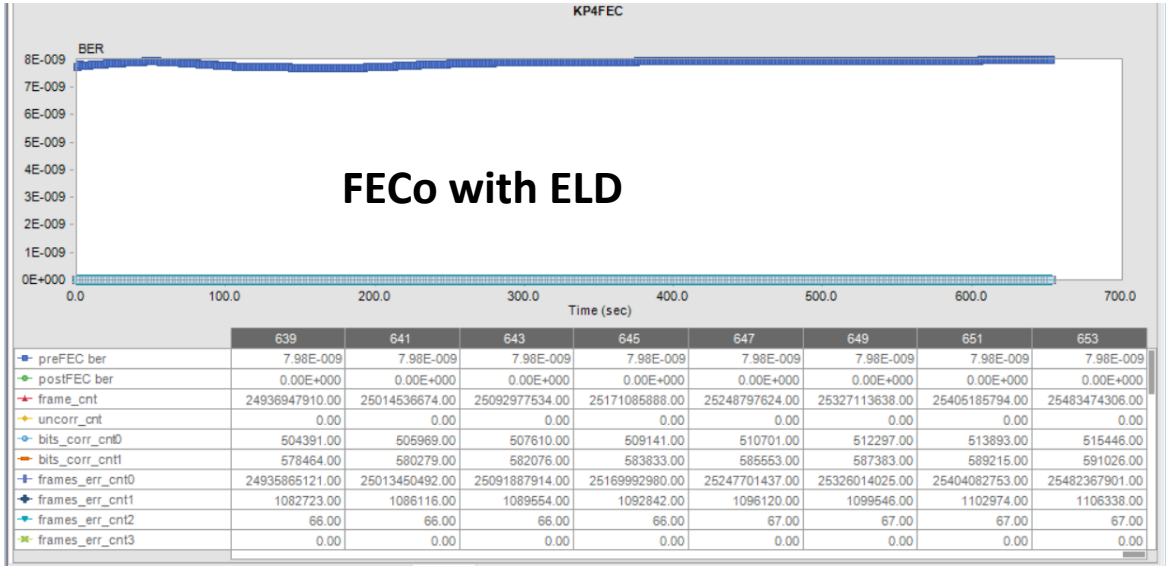
- pj/bit results were in line with design targets
- Per optical lane power comparison: $P_{212.5G}$ approximately 20% lower than $P_{226.875G}$

Investigated possible low latency modes with ELD

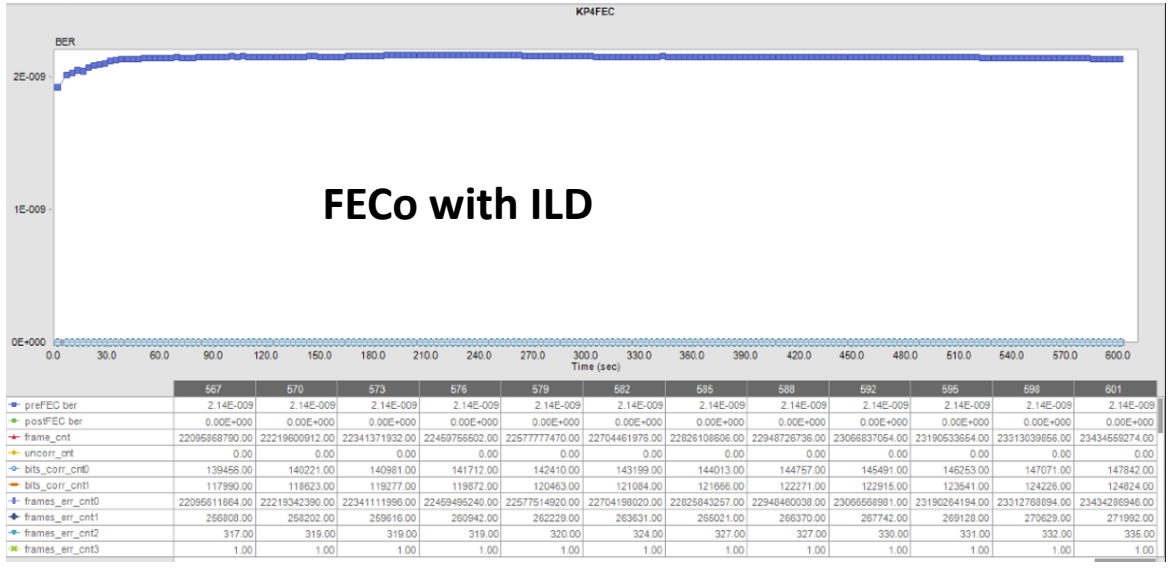
Rate	preKP4 BER	Max KP4 correction	Max KP4 correction (CI bypass)
212.5	7.98e-9	3	NA
226.875	1.46e-11	2	4*

*Note – About 2.5-3x increase in KP4 corrected bins was observed at higher preKP4 BER's (~e-6/e-7) when CI is bypassed

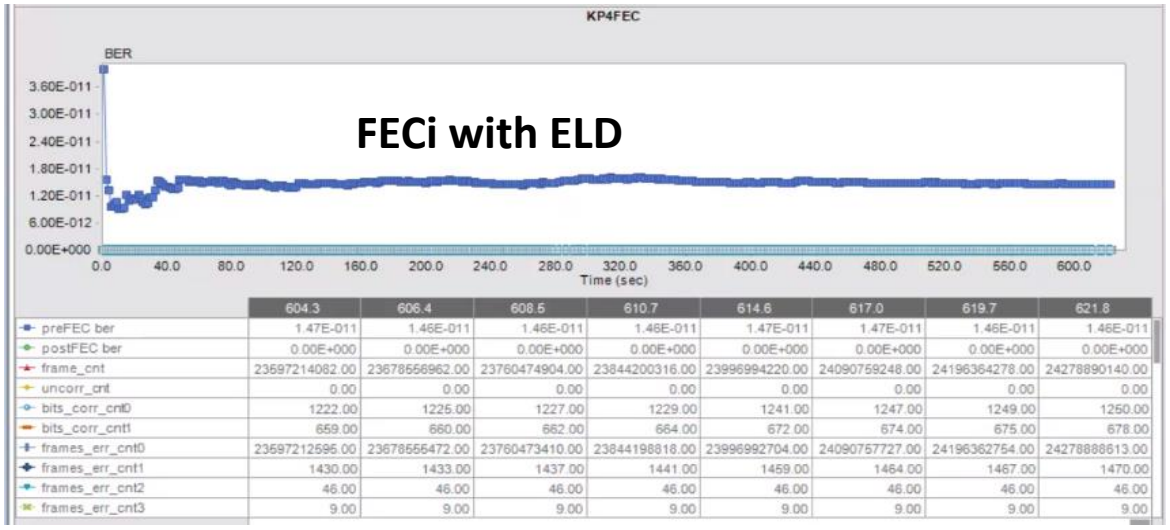
Detailed Test Results



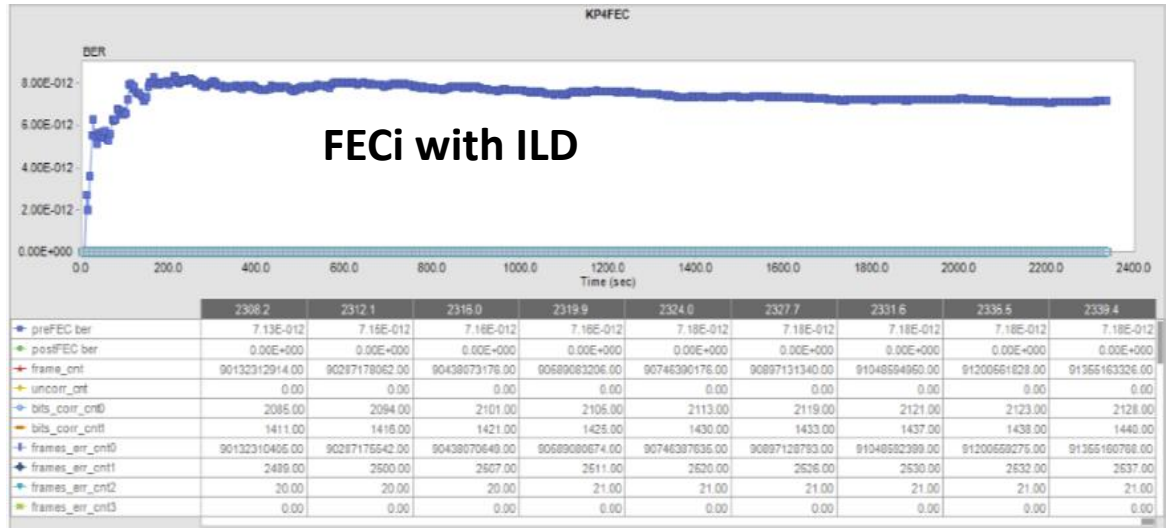
	639	641	643	645	647	649	651	653
preFEC ber	7.98E-009	7.98E-009	7.98E-009	7.98E-009	7.98E-009	7.98E-009	7.98E-009	7.98E-009
postFEC ber	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000
frame_cnt	24936947910.00	25014536674.00	25092977534.00	25171085888.00	25248797624.00	25327113638.00	25405185794.00	25483474306.00
uncorr_cnt	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
bits_corr_cnt0	504391.00	505969.00	507610.00	509141.00	510701.00	512297.00	513893.00	515446.00
bits_corr_cnt1	578464.00	580279.00	582076.00	583833.00	585553.00	587383.00	589215.00	591026.00
frames_err_cnt0	24935865121.00	25013450492.00	25091887914.00	25169992980.00	25247701437.00	25326014025.00	25404082753.00	25482367901.00
frames_err_cnt1	1082723.00	1086116.00	1089554.00	1092842.00	1096120.00	1099546.00	1102974.00	1106338.00
frames_err_cnt2	66.00	66.00	66.00	66.00	67.00	67.00	67.00	67.00
frames_err_cnt3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00



	567	570	573	576	579	582	585	588	592	595	598	601
preFEC ber	2.14E-009	2.14E-009	2.14E-009	2.14E-009	2.14E-009	2.14E-009	2.14E-009	2.14E-009	2.14E-009	2.14E-009	2.14E-009	2.14E-009
postFEC ber	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000
frame_cnt	22095868790.00	22219609912.00	22341371932.00	22459756602.00	22577777470.00	22704461976.00	22826108606.00	22948726736.00	23066837054.00	23190533664.00	23313039656.00	23434659274.00
uncorr_cnt	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
bits_corr_cnt0	139456.00	140221.00	140981.00	141712.00	142410.00	143199.00	144013.00	144757.00	145491.00	146253.00	147071.00	147842.00
bits_corr_cnt1	117990.00	118623.00	119277.00	119872.00	120463.00	121084.00	121666.00	122271.00	122915.00	123541.00	124226.00	124824.00
frames_err_cnt0	22095611664.00	22219342390.00	22341111996.00	22459495240.00	22577514920.00	22704198020.00	22826843257.00	22948460038.00	23066568981.00	23190264194.00	23312768894.00	23434286946.00
frames_err_cnt1	256808.00	258202.00	259616.00	260942.00	262229.00	263631.00	265021.00	266370.00	267742.00	269128.00	270629.00	271992.00
frames_err_cnt2	317.00	319.00	319.00	319.00	320.00	324.00	327.00	327.00	330.00	331.00	332.00	335.00
frames_err_cnt3	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00



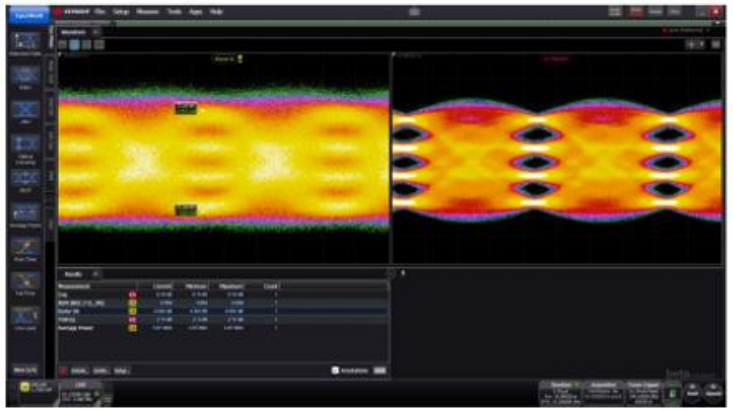
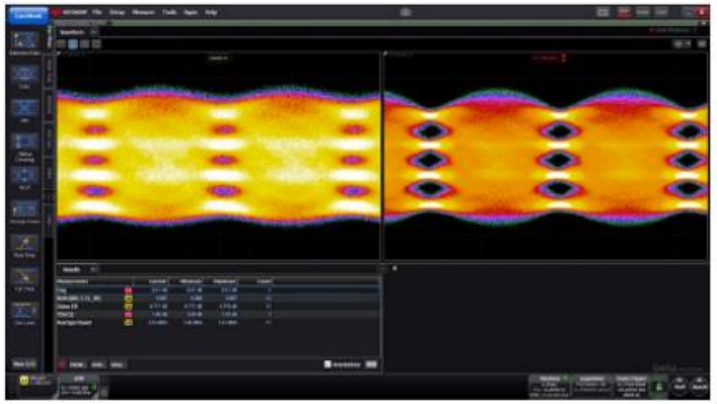
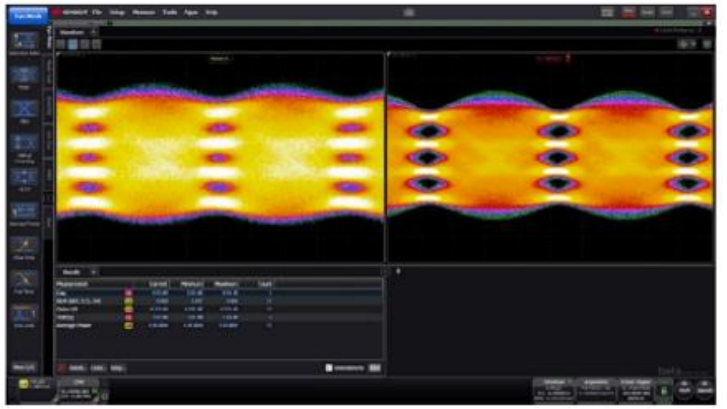
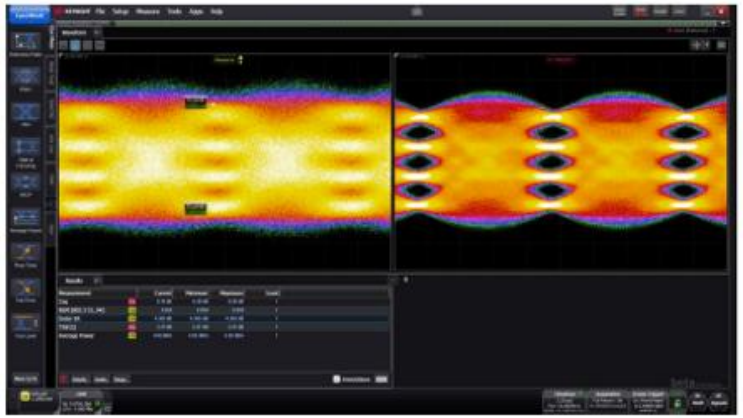
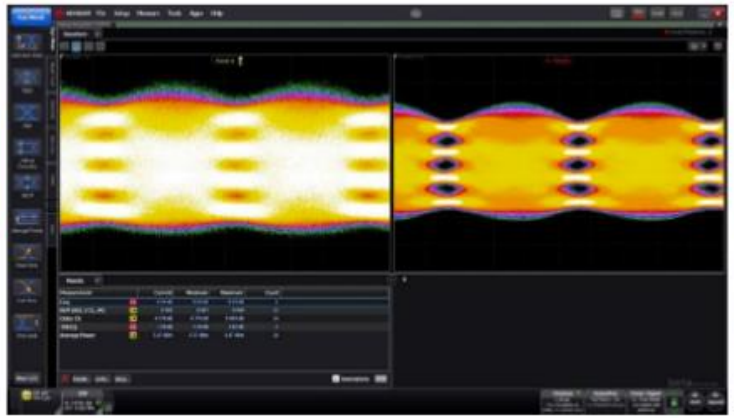
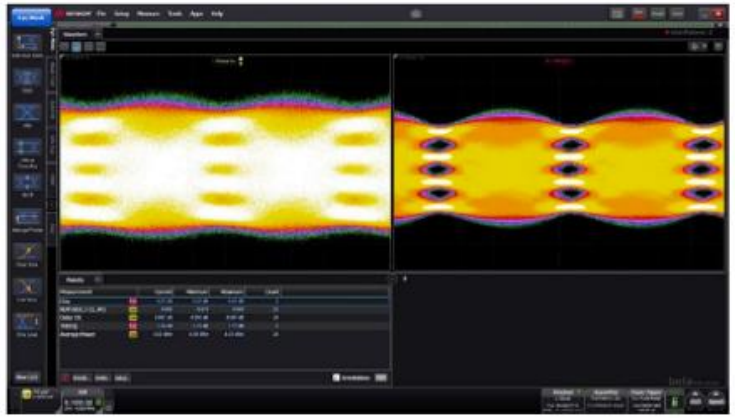
	604.3	606.4	608.5	610.7	614.6	617.0	619.7	621.8
preFEC ber	1.47E-011	1.46E-011	1.46E-011	1.46E-011	1.47E-011	1.47E-011	1.46E-011	1.46E-011
postFEC ber	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000
frame_cnt	23597214082.00	23678556962.00	23760474904.00	23844200316.00	23996994220.00	24090759248.00	24196364278.00	24278890140.00
uncorr_cnt	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
bits_corr_cnt0	1222.00	1225.00	1227.00	1229.00	1241.00	1247.00	1249.00	1250.00
bits_corr_cnt1	659.00	660.00	662.00	664.00	672.00	674.00	675.00	678.00
frames_err_cnt0	23597212595.00	23678555472.00	23760473410.00	23844198816.00	23996992704.00	24090757727.00	24196362754.00	24278888613.00
frames_err_cnt1	1430.00	1433.00	1437.00	1441.00	1459.00	1464.00	1467.00	1470.00
frames_err_cnt2	46.00	46.00	46.00	46.00	46.00	46.00	46.00	46.00
frames_err_cnt3	9.00	9.00	9.00	9.00	9.00	9.00	9.00	9.00



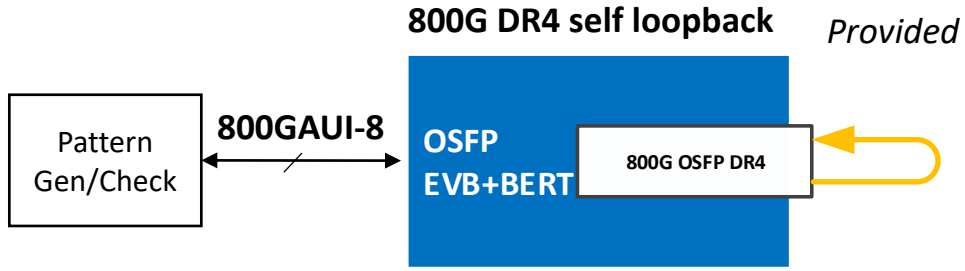
	2308.2	2312.1	2316.0	2319.9	2324.0	2327.7	2331.6	2335.5	2339.4
preFEC ber	7.13E-012	7.15E-012	7.16E-012	7.16E-012	7.18E-012	7.18E-012	7.18E-012	7.18E-012	7.18E-012
postFEC ber	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000	0.00E+000
frame_cnt	90132312914.00	90287178062.00	90438073176.00	90589083206.00	90746390176.00	90897131340.00	91048594960.00	91200561828.00	91365163326.00
uncorr_cnt	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
bits_corr_cnt0	2085.00	2094.00	2101.00	2105.00	2113.00	2119.00	2121.00	2123.00	2128.00
bits_corr_cnt1	1411.00	1416.00	1421.00	1425.00	1430.00	1433.00	1437.00	1438.00	1440.00
frames_err_cnt0	90132310405.00	90287175642.00	90438070649.00	90589080674.00	90746387635.00	90897128793.00	91048592389.00	91200559275.00	91365160766.00
frames_err_cnt1	2489.00	2500.00	2507.00	2511.00	2520.00	2526.00	2530.00	2532.00	2537.00
frames_err_cnt2	20.00	20.00	20.00	21.00	21.00	21.00	21.00	21.00	21.00
frames_err_cnt3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00

Provided by Dirk Lutz (Eoptolink)

Transmitter Testing

	800G-DR4 (ILD)	1.6T-DR8 (ELD)	2x800G-FR4 (ELD)
212G (FECo)			
227G (FECi)			

Four Channel Testing



Provided by Dirk Lutz (Eoptolink)

Time Of Duration:	2706			
FUNC MODE:	CAPI_MODE_200G	CAPI_MODE_200G	CAPI_MODE_200G	CAPI_MODE_200G
FEC MODE:	CAPI_FEC_CLIENT	CAPI_FEC_CLIENT	CAPI_FEC_CLIENT	CAPI_FEC_CLIENT
FEC TYPE_CLIENT:	FEC_TYPE_RS544	FEC_TYPE_RS544	FEC_TYPE_RS544	FEC_TYPE_RS544
Global LOS State:	LOSD	LOSD	LOSD	LOSD
Global LOL State:	Locked	Locked	Locked	Locked
PRBS LOL State:	Locked	Locked	Locked	Locked
Pre-fec BER:	6.033247E-7	3.966538E-7	3.882661E-7	4.820284E-7
Post-fec BER:	0.000000E+0	0.000000E+0	0.000000E+0	0.000000E+0
Projected Post-fec BER:	0.000000E+0	0.000000E+0	0.000000E+0	0.000000E+0
Total CW Received Count:	52858450339	52867143847	52869539205	52876296106
Total CW Corrected Count:	171144495	114222258	111098080	137811703
Total CW Uncorrected Count:	0	0	0	0
Total Symbol Corrected Count:	171604516	114379853	111291069	138146019
Total Corrected 0's Count:	30041389	56289534	14633881	68101011
Total Corrected 1's Count:	141564517	58090807	96657838	70045664
Total CW with 0 Symbol Corrected:	52687305844	52752921589	52758441125	52738484403
Total CW with 1 Symbol Corrected:	170686174	114064878	110905478	137479140
Total CW with 2 Symbol Corrected:	456647	157165	192215	330816
Total CW with 3 Symbol Corrected:	1648	215	387	1741
Total CW with 4 Symbol Corrected:	26	0	0	6
Total CW with 5 Symbol Corrected:	0	0	0	0
Total CW with 6 Symbol Corrected:	0	0	0	0
Total CW with 7 Symbol Corrected:	0	0	0	0
Total CW with 8 Symbol Corrected:	0	0	0	0
Total CW with 9 Symbol Corrected:	0	0	0	0
Total CW with 10 Symbol Corrected:	0	0	0	0
Total CW with 11 Symbol Corrected:	0	0	0	0

RS Bin 4

800G OSFP DR4 BER result without Inner-FEC

Stop Time:	2023/9/25 17:35:23			
Time Of Duration:	13			
FUNC MODE:	CAPI_MODE_200G	CAPI_MODE_200G	CAPI_MODE_200G	CAPI_MODE_200G
FEC MODE:	CAPI_FEC_CLIENT	CAPI_FEC_CLIENT	CAPI_FEC_CLIENT	CAPI_FEC_CLIENT
FEC TYPE_CLIENT:	FEC_TYPE_RS544	FEC_TYPE_RS544	FEC_TYPE_RS544	FEC_TYPE_RS544
Global LOS State:	LOSD	LOSD	LOSD	LOSD
Global LOL State:	Locked	Locked	Locked	Locked
PRBS LOL State:	Locked	Locked	Locked	Locked
Pre-fec BER:	1.473147E-8	1.232794E-9	1.055129E-9	2.004074E-9
Post-fec BER:	0.000000E+0	0.000000E+0	0.000000E+0	0.000000E+0
Projected Post-fec BER:	9.567784E-31	0.000000E+0	0.000000E+0	0.000000E+0
Total CW Received Count:	263429044	267971658	272497241	276981934
Total CW Corrected Count:	14192	1608	1105	2485
Total CW Uncorrected Count:	0	0	0	0
Total Symbol Corrected Count:	14500	1608	1105	2485
Total Corrected 0's Count:	12445	986	968	1781
Total Corrected 1's Count:	8505	797	589	1223
Total CW with 0 Symbol Corrected:	263414852	267970050	272496136	276979449
Total CW with 1 Symbol Corrected:	13906	1608	1105	2485
Total CW with 2 Symbol Corrected:	265	0	0	0
Total CW with 3 Symbol Corrected:	20	0	0	0
Total CW with 4 Symbol Corrected:	1	0	0	0
Total CW with 5 Symbol Corrected:	0	0	0	0
Total CW with 6 Symbol Corrected:	0	0	0	0
Total CW with 7 Symbol Corrected:	0	0	0	0
Total CW with 8 Symbol Corrected:	0	0	0	0
Total CW with 9 Symbol Corrected:	0	0	0	0
Total CW with 10 Symbol Corrected:	0	0	0	0

800G OSFP DR4 BER result with Inner-FEC

Provided by Dirk Lutz (Eoptolink)

Module in Switch Testing

Only FECo performance available at time of publication

800G OSFP DR4 test results on TH5 port with self-loopback and without inner FEC enable (212G):

```
====
88 : 8.97e-07
90 : 6.08e-07
91 : 3.76e-07
92 : 3.81e-07
```

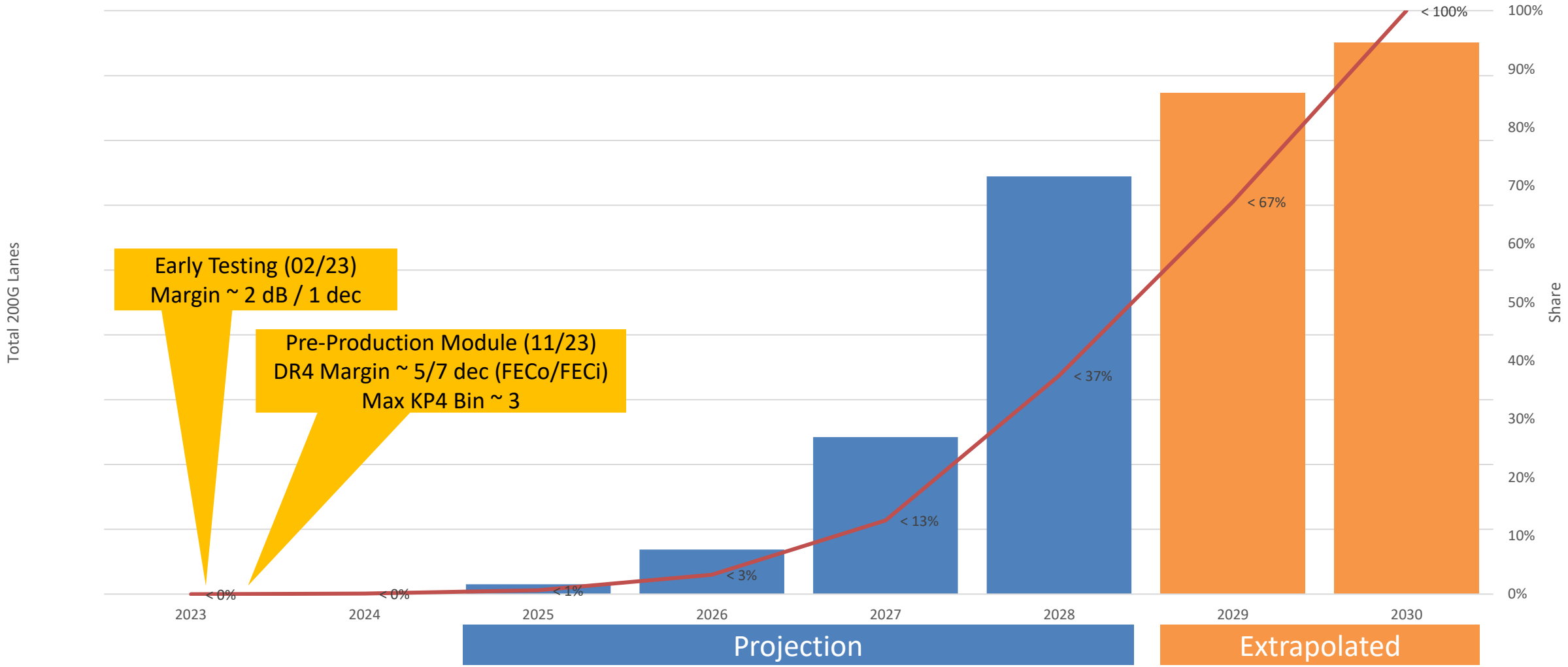
```
BCM.0> dsh -c "phydiag 88,90,91,92 fdrstat counter"
port 88: Collecting Data ...
FDR start to collect data timestamp: 6794.838646784 sec
FDR end to collect data timestamp: 6844.829230848 sec
Number of Uncorrected codewords:                    0                   0
Number of codewords:                    28900425372           390547034
Symbol errors:                            153702405             2098217
code words err S0:                      28747247865           388455987
code words err S1:                        152653797             2083894
code words err S2:                           521823                7129
code words err S3:                             1642                  22
code words err S4:                                9                   0
code words err S5:                                0                   0
code words err S6:                                0                   0
code words err S7:                                0                   0
code words err S8:                                0                   0
code words err S9:                                0                   0
code words err S10:                               0                   0
code words err S11:                               0                   0
code words err S12:                               0                   0
code words err S13:                               0                   0
code words err S14:                               0                   0
code words err S15:                               0                   0
code words err S16:                               0                   0
port 90: Collecting Data ...
FDR start to collect data timestamp: 6794.838673152 sec
FDR end to collect data timestamp: 6844.829257216 sec
Number of Uncorrected codewords:                    0                   0
Number of codewords:                    28900425484           390547021
Symbol errors:                            104825248             1452266
code words err S0:                      28795901445           389099166
code words err S1:                        104223216             1443458
code words err S2:                           299770                4384
code words err S3:                              829                  13
code words err S4:                                1                   0
code words err S5:                                0                   0
code words err S6:                                0                   0
code words err S7:                                0                   0
code words err S8:                                0                   0
code words err S9:                                0                   0
code words err S10:                               0                   0
code words err S11:                               0                   0
code words err S12:                               0                   0
code words err S13:                               0                   0
code words err S14:                               0                   0
code words err S15:                               0                   0
code words err S16:                               0                   0
```

```
port 91: Collecting Data ...
FDR start to collect data timestamp: 6794.838698496 sec
FDR end to collect data timestamp: 6844.829282304 sec
Number of Uncorrected codewords:                    0                   0
Number of codewords:                    28900425543           390547014
Symbol errors:                             73749323             1040746
code words err S0:                      28826893043           389509531
code words err S1:                        73316337             1034246
code words err S2:                          214866                3230
code words err S3:                            1070                  14
code words err S4:                              11                   0
code words err S5:                               0                   0
code words err S6:                               0                   0
code words err S7:                               0                   0
code words err S8:                               0                   0
code words err S9:                               0                   0
code words err S10:                              0                   0
code words err S11:                              0                   0
code words err S12:                              0                   0
code words err S13:                              0                   0
code words err S14:                              0                   0
code words err S15:                              0                   0
code words err S16:                              0                   0
port 92: Collecting Data ...
FDR start to collect data timestamp: 6794.838724864 sec
FDR end to collect data timestamp: 6844.829307648 sec
Number of Uncorrected codewords:                    0                   0
Number of codewords:                    28900425611           390547034
Symbol errors:                             71825841              957093
code words err S0:                      28828737884           389591752
code words err S1:                        71549902              953467
code words err S2:                          136859                1793
code words err S3:                             736                  13
code words err S4:                               3                   0
code words err S5:                               0                   0
code words err S6:                               0                   0
code words err S7:                               0                   0
code words err S8:                               0                   0
code words err S9:                               0                   0
code words err S10:                              0                   0
code words err S11:                              0                   0
code words err S12:                              0                   0
code words err S13:                              0                   0
code words err S14:                              0                   0
code words err S15:                              0                   0
code words err S16:                              0                   0
```

MAX RS(544,514) = BIN4

Data from LightCounting Sept 2023 Report
Note: LightCounting reports do not break out 800G-DR8 and 800G-DR4 volumes separately. Data here is compiled from 1.6T module forecasts (and faster)

200G/L Market Evolution



Summary

200G/L is Technically Feasible

- History of 100G/L suggests that rapid improvements happen in the early phases of a new speed transition

- Early production grade parts are back from fabrication and testing has begun
  - Performance is consistent with current baseline proposals.

- The initial results provide excellent confidence that 200G lanes are technically feasible with both FEC modes (FECi and FECo)
  - Initial testing of 800G-DR4 shows > 5 decades of BER margin (max KP4 BIN ≤ 4)
  - Testing continues, including on 800G-FR4 modules.

END