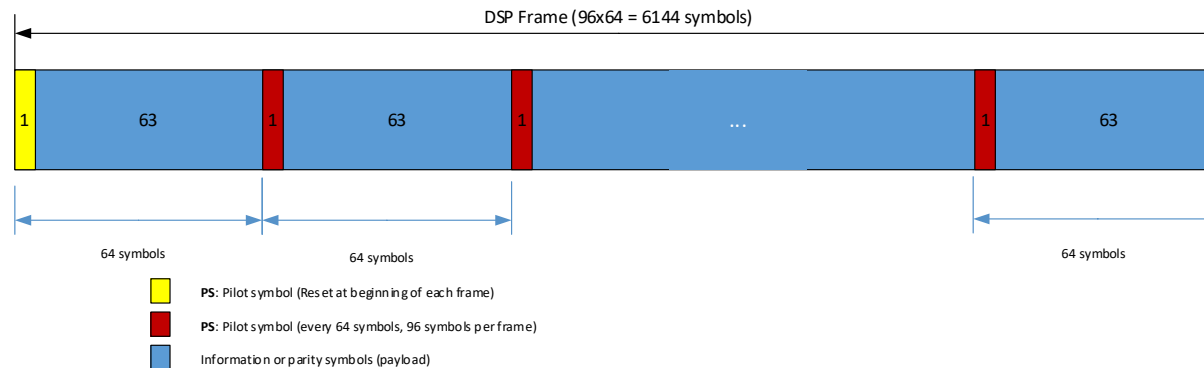# 800GBASE-LR1 state diagrams

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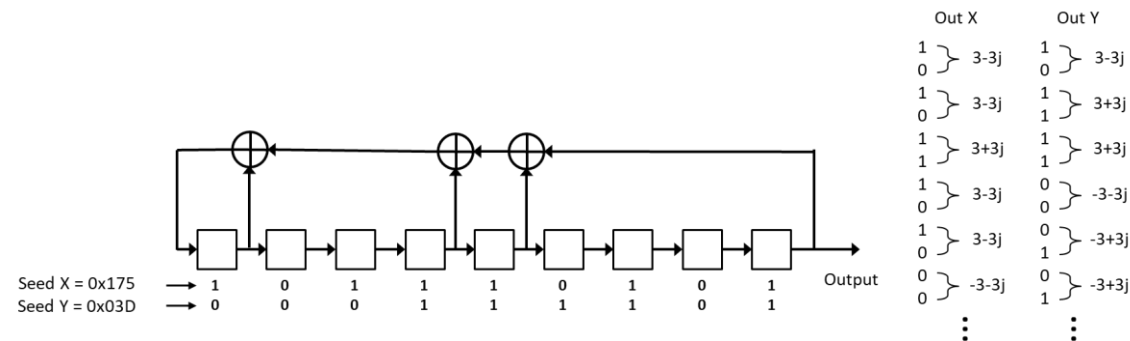
The 800GBASE-LR1 DSP frame

- The 800GBASE-LR1 DSP frame is defined as a set of 96x64=6144 4–bit blocks
  - 4–bit pilot symbols (PS) are inserted every 64 4-bit blocks (1 pilot 4–bit symbol, 63 message 4–bit blocks)

- Two 800GBASE-LR1 DSP frames are generated by the Inner FEC sublayer
  - The 4–bit blocks for DSP frame_0 are constructed from two consecutive bits from output_0 (to be mapped to X_I) and two consecutive bits from output_1 (to be mapped to X_Q)
  - The 4–bit blocks for the DSP frame_1 are constructed from two consecutive bits from output_2 (to be mapped to Y_I) and two consecutive bits from output_3 (to be mapped to Y_Q)

DSP Frame (96x64 = 6144 symbols)

| 1 | 63 | 1 | 63 | 1 | ... | 1 | 63 |

64 symbols   64 symbols   64 symbols

PS: Pilot symbol (Reset at beginning of each frame)

PS: Pilot symbol (every 64 symbols, 96 symbols per frame)

Information or parity symbols (payload)
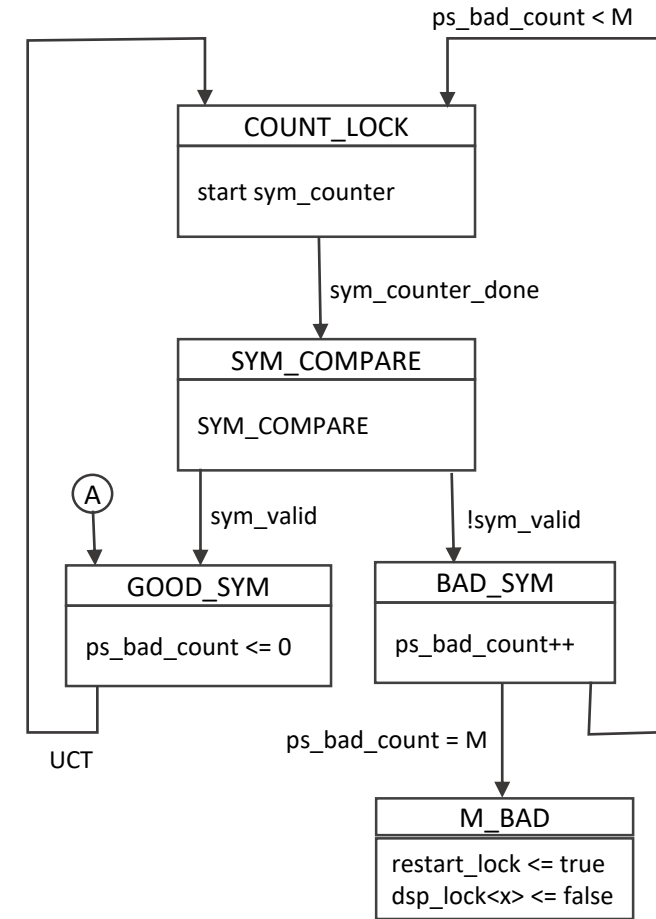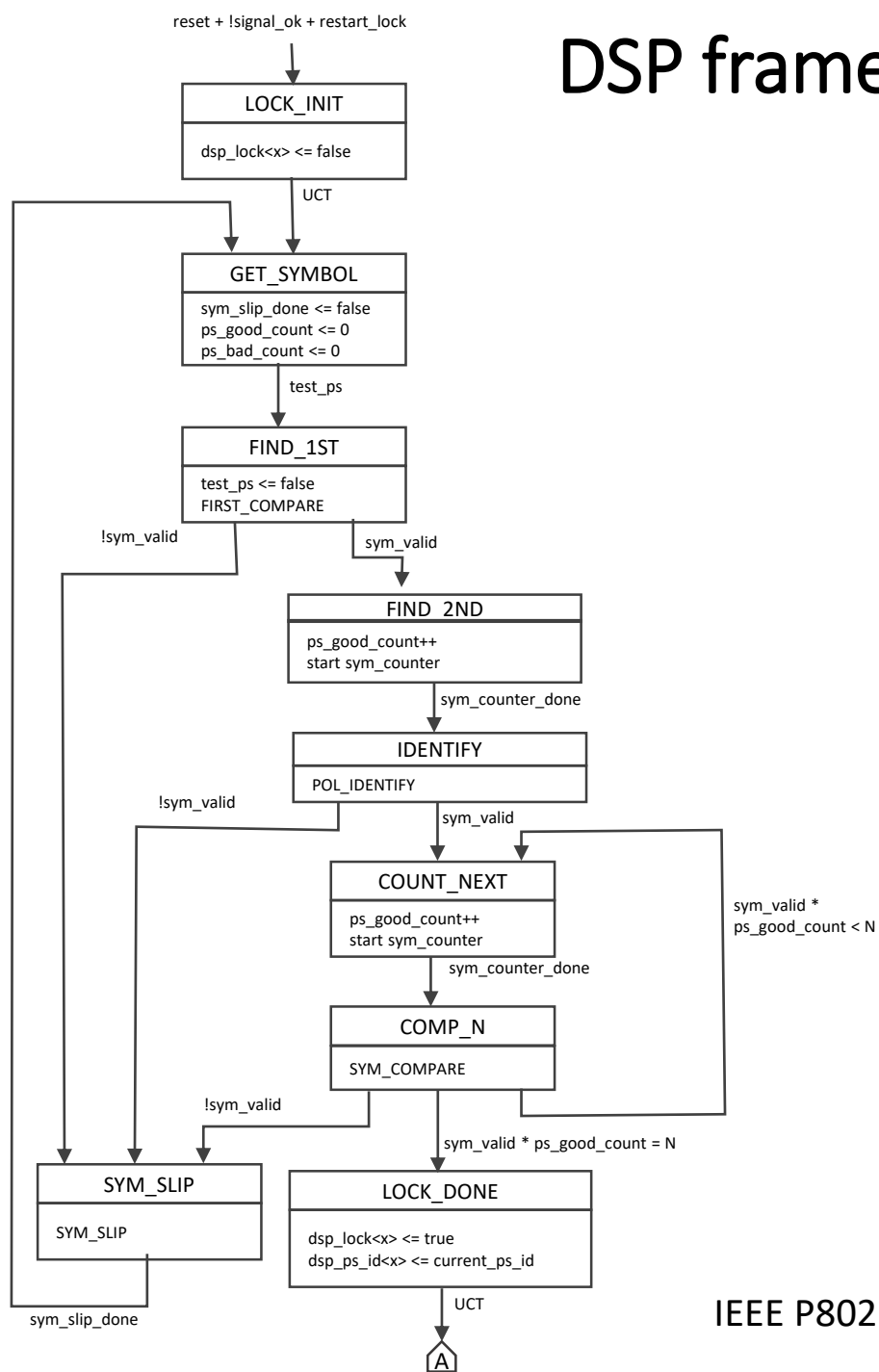
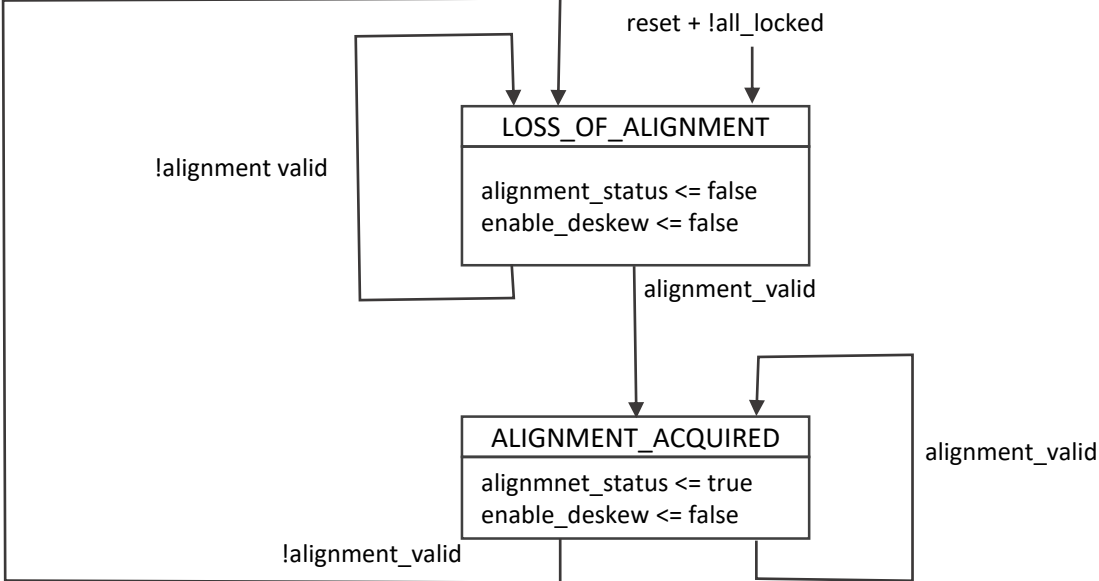IEEE P802.3dj Task Force, January 2024

Pilot Sequences (PSs)

- The pilot sequence is a fixed PRBS9 sequence with different seed values for DSP frame_0 and for DSP frame_1
    - The seeds are selected so that the pilot sequences are DC balanced.
- The generator is initialized using the seed at the start of every DSP frame, so that the same 96 PS symbols, [P0,...,P95] are inserted into every DSP frame PS field
- For each one of DSP frame_0 and DSP frame_1, the generator produces 192 bits PRBS[191:0] that are complemented by zeros to generate the 4–bit PS symbols.
    - These 4–bit PS symbols are mapped to outer symbols of the 16QAM constellation, allowing robust framing to the 16QAM constellation
- The pilot sequence bits are used to synchronize to the each of the two DSP frames and to identify DSP frame_0 and DSP frame_1
    - Note that the first symbol of both PSs is the same

DSP frame synchronization state diagrams

reset + !signal_ok + restart_lock

LOCK_INIT

dsp_lock<x> <= false

UCT

GET_SYMBOL

sym_slip_done <= false
ps_good_count <= 0
ps_bad_count <= 0

test_ps

FIND_1ST

test_ps <= false
FIRST_COMPARE

!sym_valid   sym_valid

FIND_2ND

ps_good_count++
start sym_counter

sym_counter_done

IDENTIFY

POL_IDENTIFY

!sym_valid   sym_valid

COUNT_NEXT

ps_good_count++
start sym_counter

sym_valid *
ps_good_count < N

sym_counter_done

COMP_N

SYM_COMPARE

!sym_valid

sym_valid * ps_good_count = N

SYM_SLIP

SYM_SLIP

sym_slip_done

LOCK_DONE

dsp_lock<x> <= true
dsp_ps_id<x> <= current_ps_id

UCT

Ⓐ

ps_bad_count < M

COUNT_LOCK

start sym_counter

sym_counter_done

SYM_COMPARE

SYM_COMPARE

Ⓐ   sym_valid   !sym_valid

GOOD_SYM

ps_bad_count <= 0

BAD_SYM

ps_bad_count++

UCT   ps_bad_count = M

M_BAD

restart_lock <= true
dsp_lock<x> <= false

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Deskew state diagram

alignment_valid
A Boolean variable that is set to true if the polarization symbol streams are aligned. Polarization symbol streams are considered to be aligned when dsp_lock<x> is true for both x, each polarization symbol stream has a unique identifier, and the polarization symbol streams are deskewed. Otherwise, this variable is set to false.
all_locked
A Boolean variable that is set to true when dsp_lock<x> is true for both x and is set to false when dsp_lock<x> is FALSE for either x.

Summary

- State diagrams for 800GBASE-LR1 presented
- Propose to adopt the state diagrams as a baseline for 800GBASE-LR1 (802.3dj Clause 184)
- Exact values of N and M are TBD
  - The plan is to bring a proposal next time