Low Latency Mode for Inner FEC

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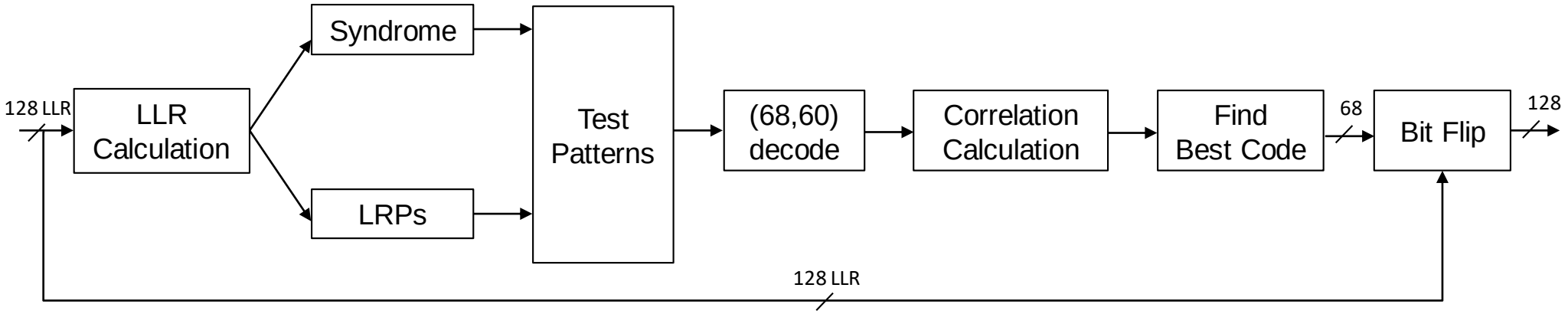
Introduction

- Latency is critical to AI and ML applications.
- Power limitation is another critical issue for 800GE/1.6TE in data center network.
- “Inner FEC bypass” has been proposed multiple times to achieve low latency/power.
  - See he_3dj_02a_230206, welch_3dj_03c_2305, welch_3dj_04a_2307, bernier_3dj_01_2309,…
- FECo mode has been adopted for 200GBASE-DR1, 400G-BASE-DR2, 800GBASE-DR4 and 1.6TBASE-DR8 for lower latency.
- This contribution proposes an option to operate the inner FEC (aka FECi mode) with the convolutional interleaver (CI) “bypassed” to lower the latency and power for other PMDs.
  - Performance of FECi w/o CI is analyzed.
  - The word “bypass” in this contribution means the CI is there, but is not used.

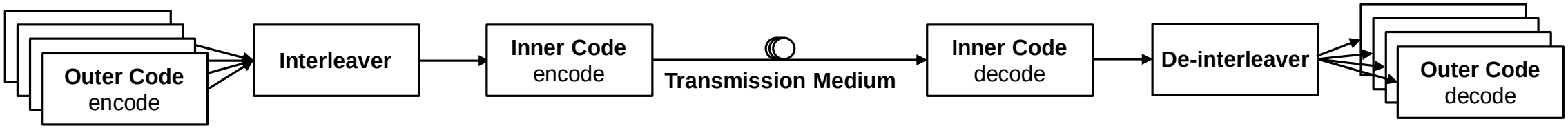
Revisit: Latency of Inner Code Decoder

- The decoding latency of the inner FEC code itself is minimal.
  - Short BCH/Hamming decoding latency is as low as 1~10ns depending on algorithm (HD or SD).
  - 200 GbE using 2xRS codewords interleaving has a PCS latency (including FEC) of 88.2 ns.
    - See brown_3dj_optx_01b_230413
    - Adding the 4x RS codewords interleaving conversion, the total FEC related latency would be 139.4ns.
  - Typical latency for the inner code encoding/decoding w/ the PAM4 interleaver is ~15ns (~10.8% of 139.4ns)
    - **Equivalent to 3m of optical fiber**.

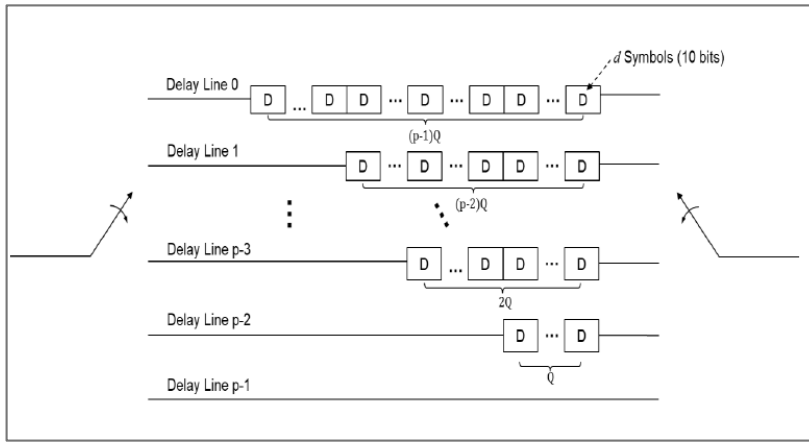


Typical Soft-decision Decoding Flow

Interleaver for Concatenated FEC



- Interleaver between outer and inner code can systematically distributed the “clustered” errors from inner code decoders.
- For block codes like RS FEC, convolutional interleaver (CI) is often used to lower latency compared to block interleaver of equivalent depth.
  - 12 RS codeword CI was adopted to maximize the performance, but with a latency penalty especially for 200/400GbE.



Rate	d (RS symbol)	P	Q	Depth	Latency ns	FEC_I Lane Rate
1.6TE	4	3	24	12x RS	27.1	200G/lane
800GE	4	3	48	12x RS	54.2	
400GE	4*	3	96	12x RS	108.4	
200GE	4*	3	192	12x RS	216.8	

he_3dj_01_2307.pdf

Type-2 FEC Performance vs Interleaving Depth of RS(544,514)

- bliss_3df_01a_220517 compared FEC performance with different interleavers.
  - 4-way RS interleaving gives ~2.45dB more NCG comparing to KP4 only, while 12-way RS interleaving gives 2.95dB.

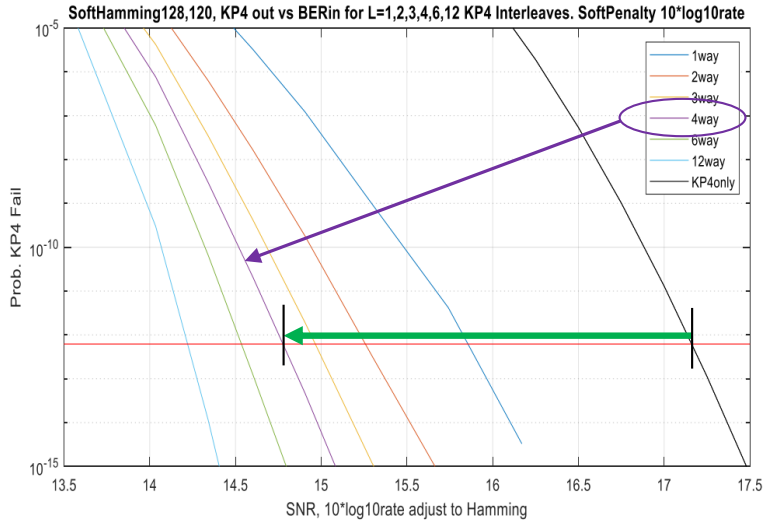
- ran_3dj_logic_01_230629 analyzed distribution of RS-FEC symbol errors caused by inner FEC failure.
  - Following measured BER at module output is suggested:

- To get CER=8e-13 (equivalent of the FLR target):
  - Without inner FEC: <2.4e-4
  - With inner FEC and 12-way interleaving: **<2.85e-4**
  - With inner FEC and 4-way interleaving (800G/1.6T): **<8e-5**
  - With inner FEC and 2-way interleaving (200G/400G) : **<2.1e-5**

ran_3dj_logic_01_230629

  - This does not mean having inner FEC with 4-way RS interleaving performs worse than KP4 only (FECo mode).
  - Equivalent PMD BER shall be evaluated.

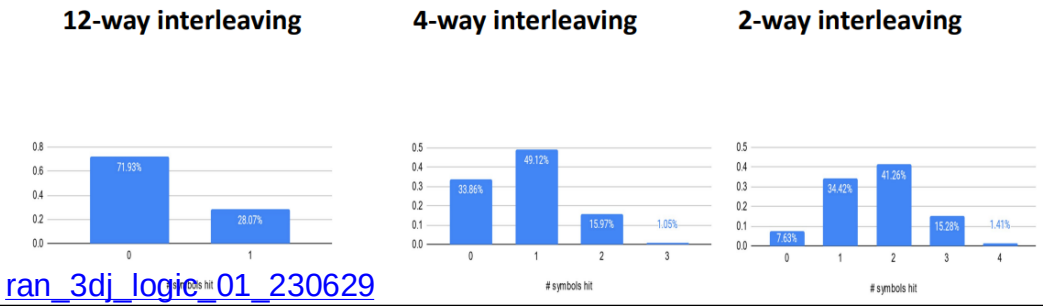
Performance; KP4 failure rate vs SNR, for different interleavers;



- The Hamming codes are penalized 10*log10(rate) = 0.28 dB (result of AWGN model)
- Without interleaver, the 'net coding gain' is only ~1.35dB
- A 12 way interleaver is optimal (fully randomizes the errors within a Hamming payload) and gives net coding gain of ~2.95dB

bliss_3df_01a_220517

Distribution of RS symbol errors given an inner FEC failure



ran_3dj_logic_01_230629

Performance Evaluation of Different FEC Schemes

- We compared the FEC performance in terms of PMD BER threshold and latency, with the following variables:
  - **FEC scheme:** Type 1, Type 2 w/ CI, Type 2 w/o CI.
  - **Ethernet Rates:** 100 GbE, 200 GbE, 400 GbE, 800 GbE and 1.6 TbE.
  - **Physical lane rates:** 100G/lane and 200G/lane PMDs.
  - **RS-FEC interleaving depth:** 2x for 100G/lane PMDs, 4x for 200G/lane PMDs
  - **AUI error propagation factor:** 0, 0.75
  - **AUI BER per PHY** (Measured): 2E-5, 4E-5 (assuming precoding used for a = 0.75)

- Latency for RS-FEC follows the model used in brown_3dj_optx_01b_230413.

Note: The soft-decision decoder used in this presentation was a textbook Chase-II decoder, with 42 test patterns.

BER Threshold and Latency for Different FEC Schemes

Rate	Rate per lane	RS-FEC codeword interleaving	PCS latency (incl. Outer FEC) (ns)	Inner FEC latency (ns)	CI depth	CI latency (ns)	Total Latency (ns)	AUI DER0 per PHY	AUI Measured BER per PHY	AUI error extension probability	Available random BER for optics.
100GE	**100G**	2	139.4	NA			139.4		2E-5	0.75	2.40E-04
200GE	**100G**	2	88.2	NA			88.2		2E-5	0.75	2.40E-04
	200G	4	139.4	NA (FECo mode)			139.4	2.67E-5	2E-5	0	2.60E-04
									4E-5	0.75	**2.35E-04**
			139.4	15	Bypass	0	154.4		2E-5	0	3.65E-03
									4E-5	0.75	3.50E-03
			139.4	15	12-way	280	**434.4**		2E-5	0	5.00E-03
									4E-5	0.75	4.90E-03
400GE	**100G**	2	62.6	NA			62.6		2E-5	0.75	2.40E-04
	200G	4	88.2	NA (FECo mode)			88.2	2.67E-5	2E-5	0	2.60E-04
									4E-5	0.75	**2.35E-04**
			88.2	15	Bypass	0	103.2		2E-5	0	3.65E-03
									4E-5	0.75	3.50E-03
			88.2	15	12-way	140	**243.2**		2E-5	0	5.00E-03
									4E-5	0.75	4.90E-03
800GE	**100G**	4	62.6	NA			62.6		2E-5	0.75	2.40E-04
	200G	4	62.6	NA (FECo mode)			62.6	2.67E-5	2E-5	0	2.50E-04
									4E-5	0.75	**2.25E-04**
			62.6	15	Bypass	0	77.6		2E-5	0	3.55E-03
									4E-5	0.75	3.40E-03
			62.6	15	12-way	56	133.6		2E-5	0	5.00E-03
									4E-5	0.75	4.80E-03
1.6TE	**200G**	4	49.8	NA (FECo mode)			49.8	2.67E-5	2E-5	0	2.50E-04
									4E-5	0.75	**2.25E-04**
			49.8	15	Bypass	0	64.8		2E-5	0	3.55E-03
									4E-5	0.75	3.40E-03
			49.8	15	12-way	25.6	90.4		2E-5	0	5.00E-03
									4E-5	0.75	4.80E-03

Burst Error Analysis

- Independent studies have analyzed Type-2 FEC w/o CI, and with the 4-way interleaving of RS(544,514) FEC, 2E-3 – 3E-3 pre-FEC BER can be allowed for bursty channels based on different soft-decoding algorithms to maintain 1E-13 BER objective.

	Req. SNR for 6.2e-13 FER	Penalty wrst Full CI	Net Coding gain vs (HD DFE)	Req. Inner code Input BER
Full CI	14.5	0	3.17	4.85E-03
1/2 CI	14.75	0.25	2.92	3.60E-03
No CI, 4-way KP	14.85	0.35	2.82	3.00E-03
No CI, 2-way KP	15.2	0.7	2.47	2.20E-03
KP Only, 4-way KP+Symbol Int.	17.95	3.45	0	

riani_3dj_01a_2303.pdf, α = 0.75, SOVA + Chase decoding

RS-FEC codeword interleaving	Inner FEC	AUI DER0 per PHY	AUI error extension probability	Optical PMD 1-tap DFE	Optical PMD BER incl. bursts
4-way	Yes*, w/o CI	2.67E-5	0.75	0.5	2E-3
4-way	No	2.67E-5	0.75	0.5	3.3E-4

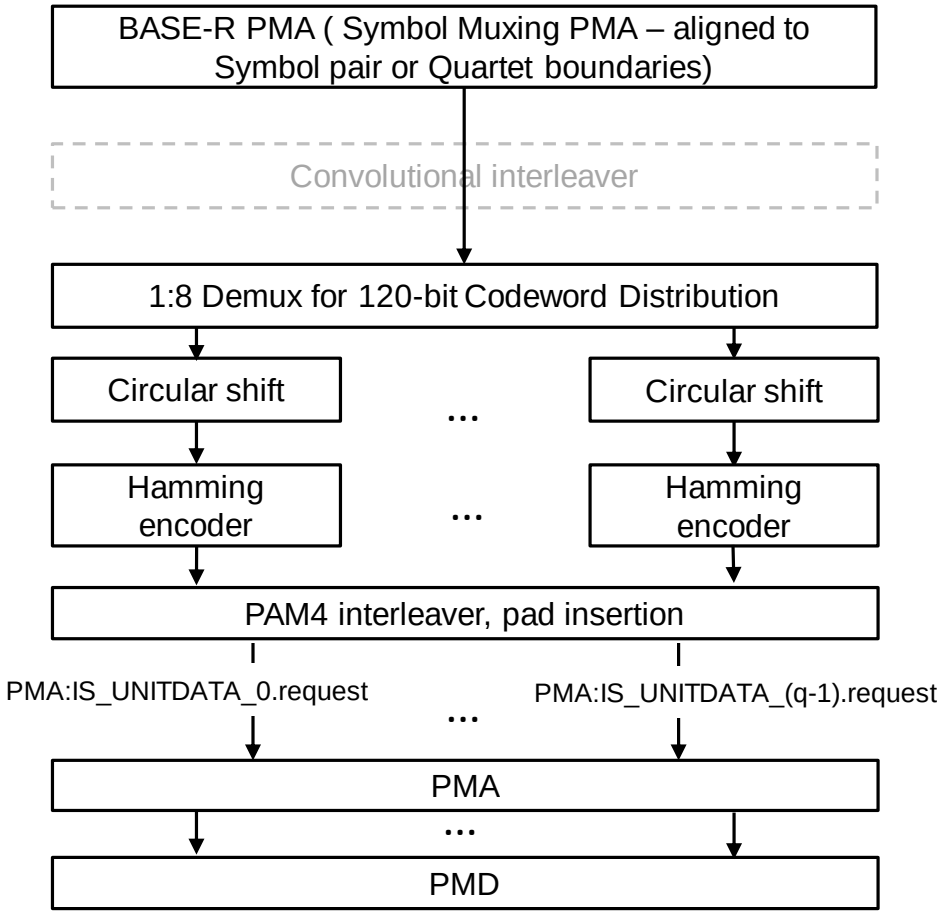
* This work, basic Chase-II decoding.

Advantages of Bypassing CI

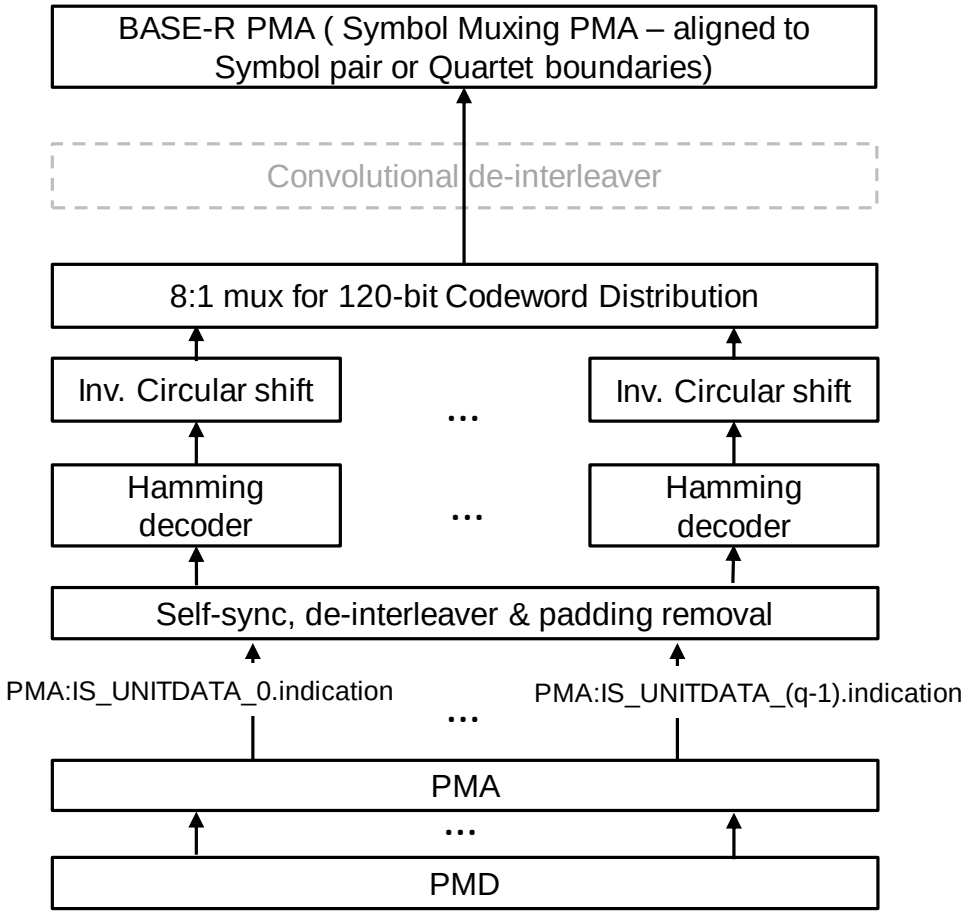
- With **~15ns** added latency for inner FEC, the pre-FEC BER threshold for optical PMD can be relaxed by **15x** compared to FECo (KP4 FEC only).
  - 3.5E-3 / 2.35E-4 = 14.89x
  - 3.4E-3 / 2.25E-4 = 15.11x
  - Under bursty cases, FECi w/o CI still maintains > 6x advantage over FECo for 1-tap DFE of 0.5.
- Bypassing CI does not affect the baud rate on the PMD.
  - No new PHYs will be introduced.
  - Whether the CI is bypassed or not can be established by the PMD, to avoid complications in PMD specs.
    - i.e. CI is bypassed for DR, (and probably FR, too); LR operates with CI.
- Bypassing CI does not affect how the padding is inserted or detected.
  - Padding can still be identified using the adopted method.

Illustration for Inner FEC w/o CI

Transmit path



Receive path



Summary

- For latency/power sensitive applications with good BER floor, we recommend to use the inner FEC without CI.
  - Inner FEC sublayer latency can be drastically reduced, to the equivalent of ~3 meters of fibre.
  - CI is also a key contributor to power consumption.
- CI-bypass is proposed for the following PMDs in P802.3dj:
  - 200GBASE-FR1
  - 400GBASE-DR2-2
  - 800GBASE-DR4-2, 800GBASE-FR4, 800GBASE-FR4-500
  - 1.6TBASE-DR8-2
- **Data rate is not affect** whether using the CI or not.
  - Padding insertion mechanism is not affected, either.

Thank you!