

# Analysis of C2M updated Channels for 200Gbps - up to 34dB channels

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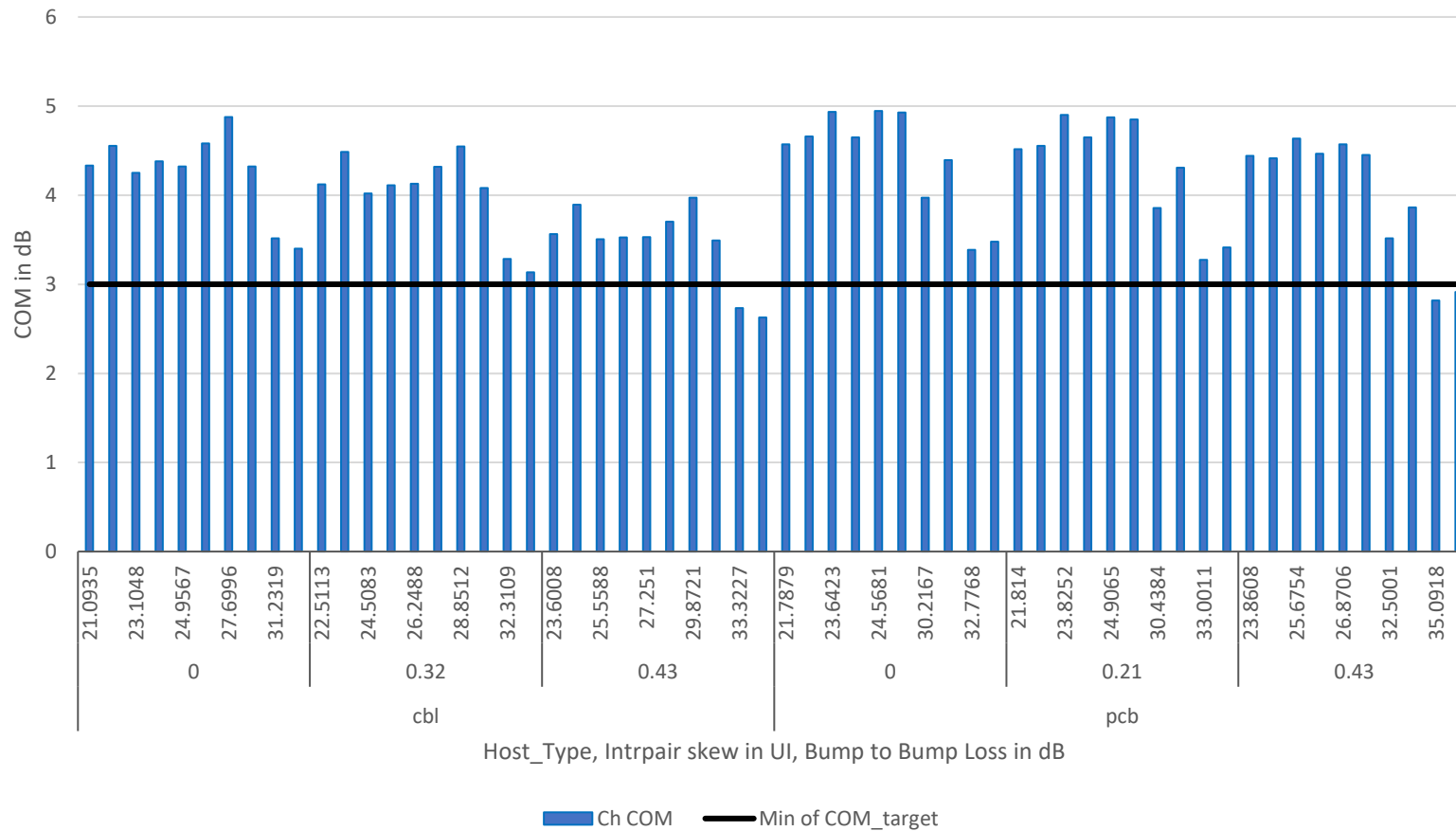
# C2M Channel Analysis -Goals

- Find a minimal reference Serdes without MLSE feature that meets the needs of updated channels based on 2 RU, 64 port, 512 Radix , 1.6T/port system design
  - Cover both Cabled\_host and PCB\_host channels with “Max feasible” skew version
  - No Skew and Excessive skew for comparison only

# C2M Channel Analysis - Setup

- Simulation setup Includes
  - Both types of packages ( Type A and Type B)
  - Mixing of Package types for
  - Package variations
    - Host Silicon package trace lengths – 8 mm to 45 mm
    - Module Silicon package trace lengths – 4 mm -12 mm
  - Cover all Cabled\_host and PCB\_host channels
    - All skew version(s)
  - Refer included COM table for other details of Reference Serdes.

# C2M Channel Analysis – PKG B



## Includes:

Packages B

Host side: 45 mm

Module side: 8 mm

all Skew versions of channels :

No skew, Max\_tolerable and excessive,

## Ref Serdes:

TX:

A\_v: 0.45V with Rd =50 Ohm

4 pre-tap

CTLE:

gDC =-10 dB; gDC\_HP = -4 dB

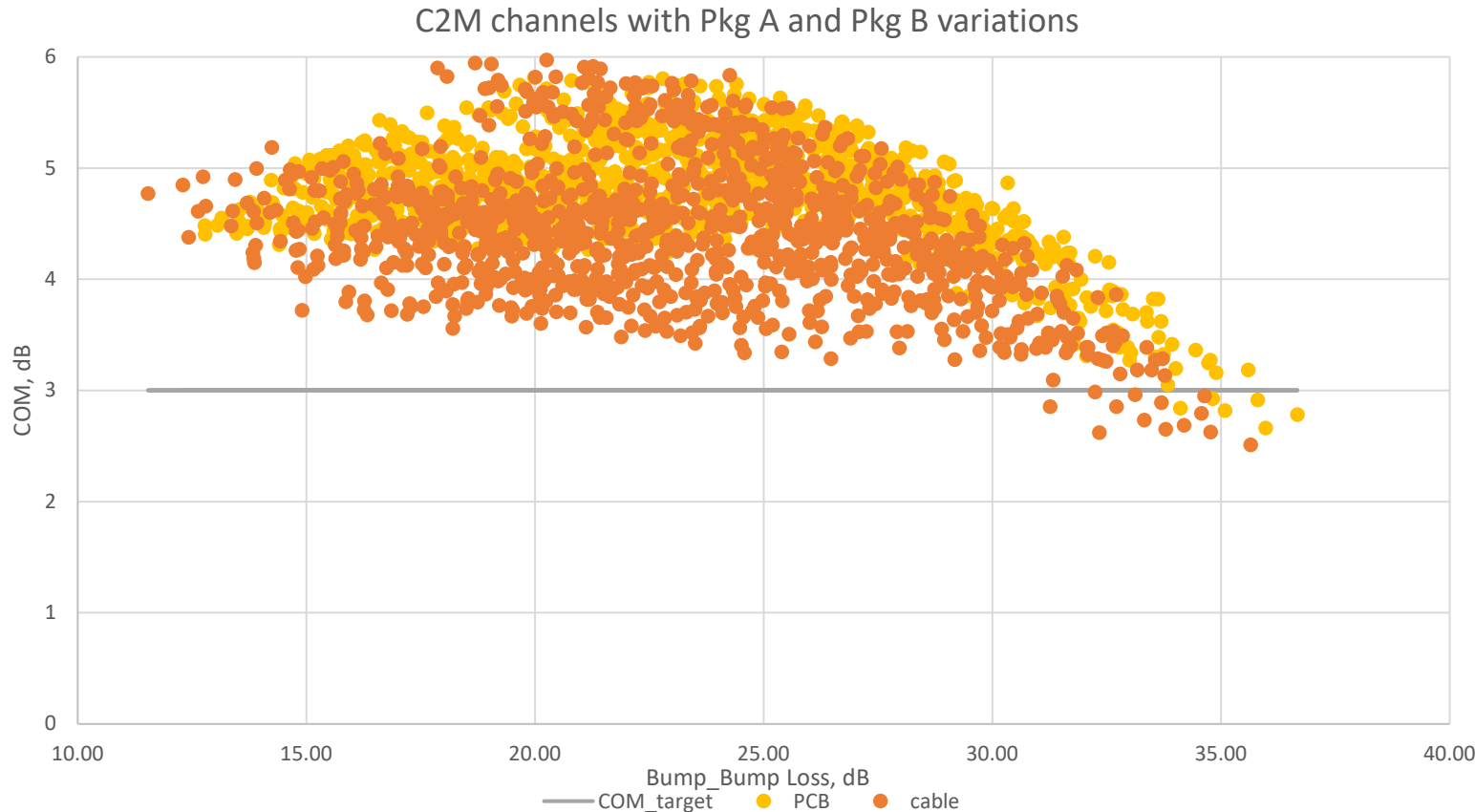
RX:

1 Tap DFE

40 post tap FFE: 8 fixed+ 8 banks of 4 floating up to 80UI

4 pre-tap

# C2M Channel Analysis – All conditions



## Includes:

Packages A and B

Host side: 8mm - 45 mm

Module side: 4mm – 12 mm

all Skew versions of channels :

No skew, Max\_tolerable and excessive,

## Ref Serdes:

TX:

A\_v: 0.45V with Rd =50 Ohm

4 pre-tap

CTLE:

gDC =-10 dB; gDC\_HP = -4 dB

RX:

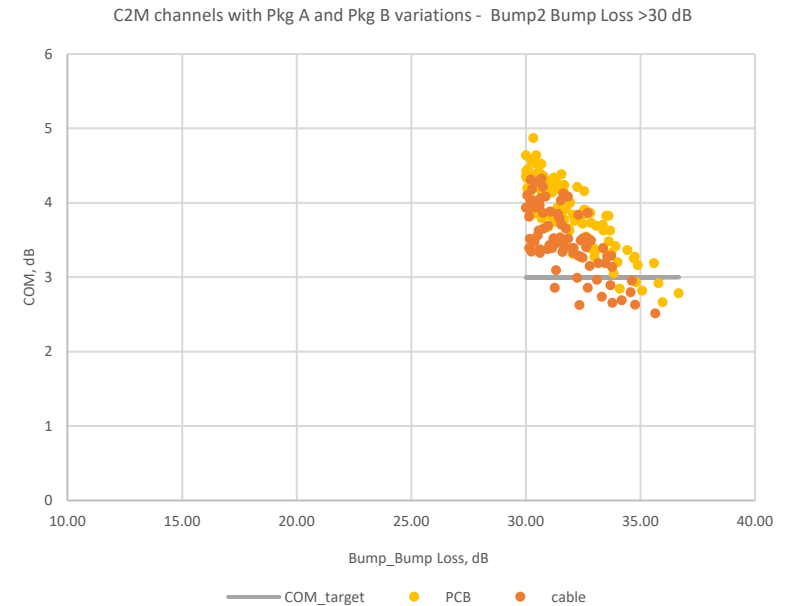
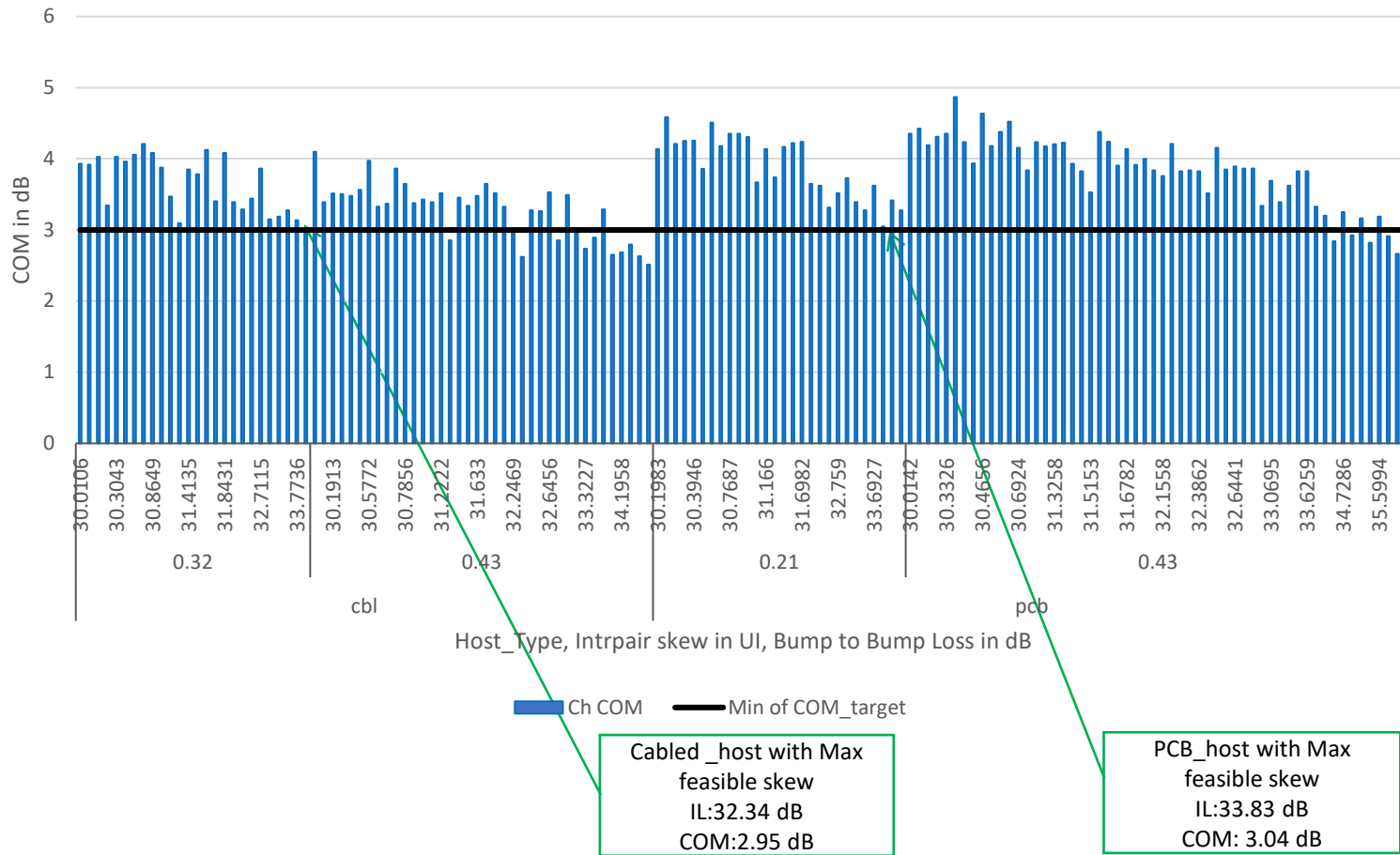
1 Tap DFE

40 post tap FFE: 8 fixed+ 8 banks of 4 floating up to 80UI

4 pre-tap

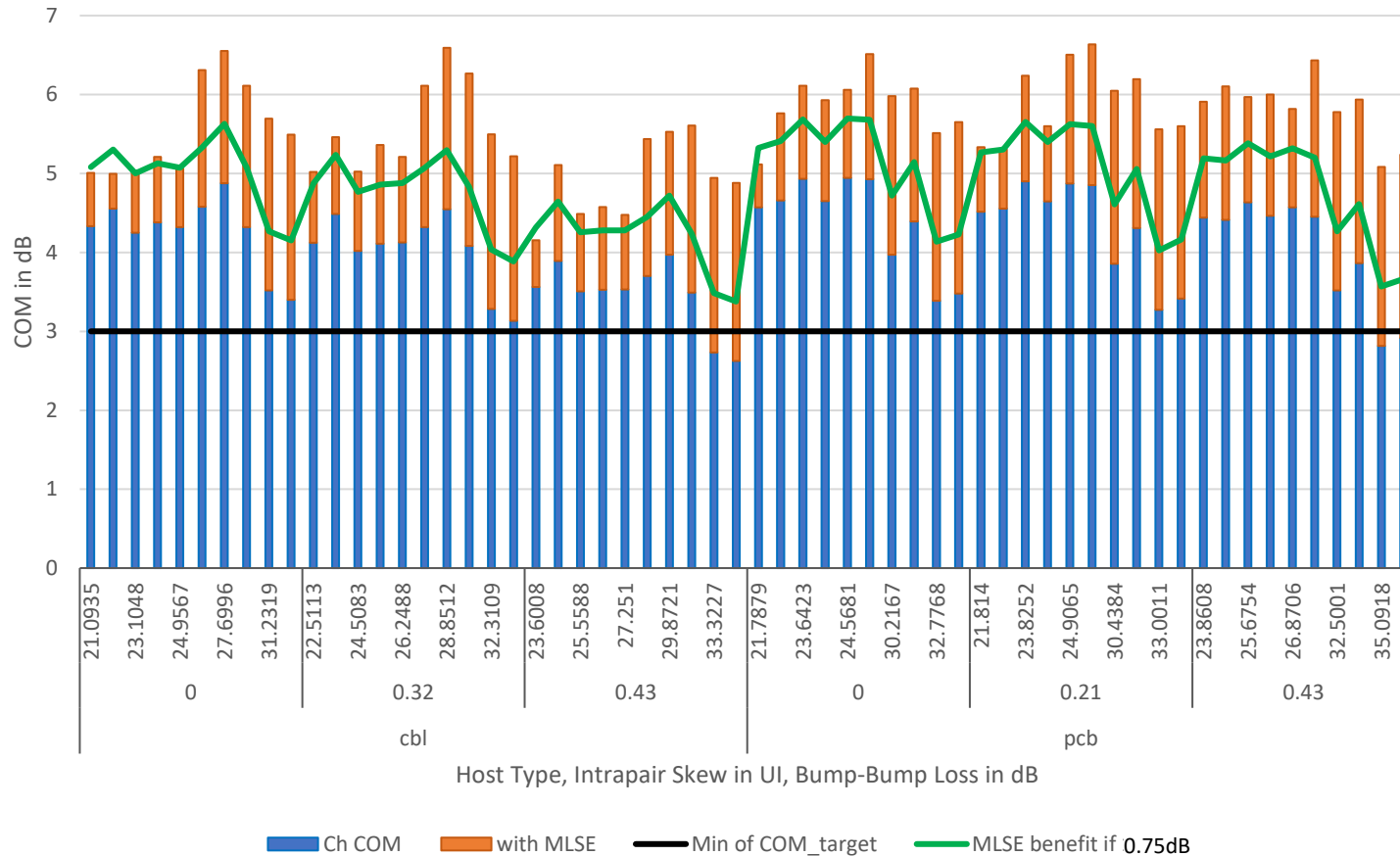
Observation: CTLE is adopting to lower range of capability. gDC: upto -7 dB

# C2M Channel Analysis – all conditions for channels >30 dB



This type of ref. Serdes is covering up to 32 dB of cabled host channels and up to 34 dB of PCB host channels

# C2M Channel Analysis – PKG B with MLSE



**Includes:**

Packages B

Host side: 45 mm

Module side: 8 mm

all Skew versions of channels :

No skew, Max\_tolerable and excessive,

**Ref Serdes (with MLSE):**

TX:

A\_v: 0.413V with Rd =50 Ohm

4 pre-tap

CTLE:

gDC =-10 dB; gDC\_HP = -4 dB

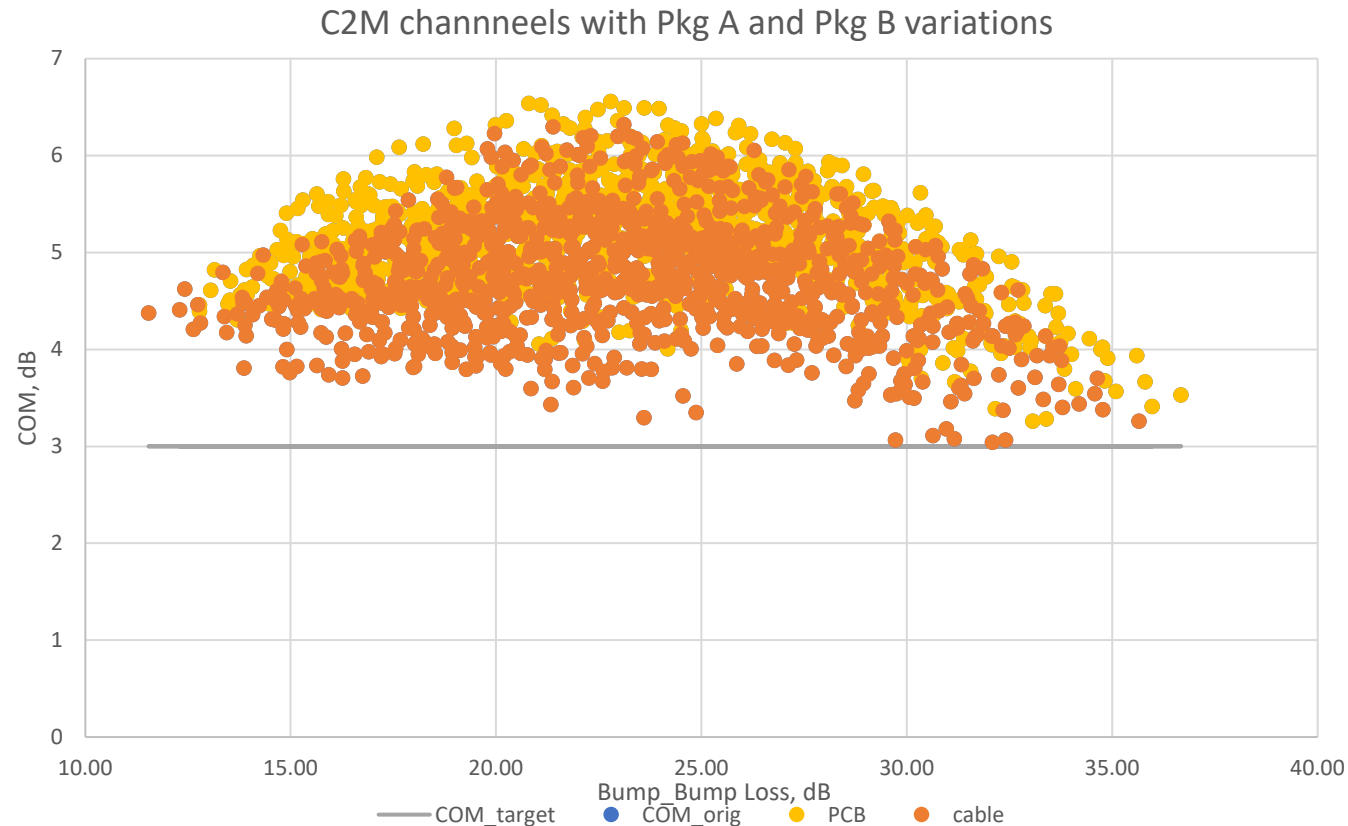
RX:

1 Tap DFE

40 post tap FFE: 8 fixed+ 8 banks of 4 floating up to 60UI

4 pre-tap

# C2M Channel Analysis with MLSE – All conditions



## Includes:

Packages A and B

Host side: 8mm - 45 mm

Module side: 4mm - 12 mm

all Skew versions of channels :

No skew, Max\_tolerable and excessive,

## Ref Serdes (with MLSE, max benefit capped at 0.75dB):

TX:

**A\_v: 0.413V** with Rd =50 Ohm

4 pre-tap

CTLE:

gDC =-10 dB; gDC\_HP = -4 dB

RX:

1 Tap DFE

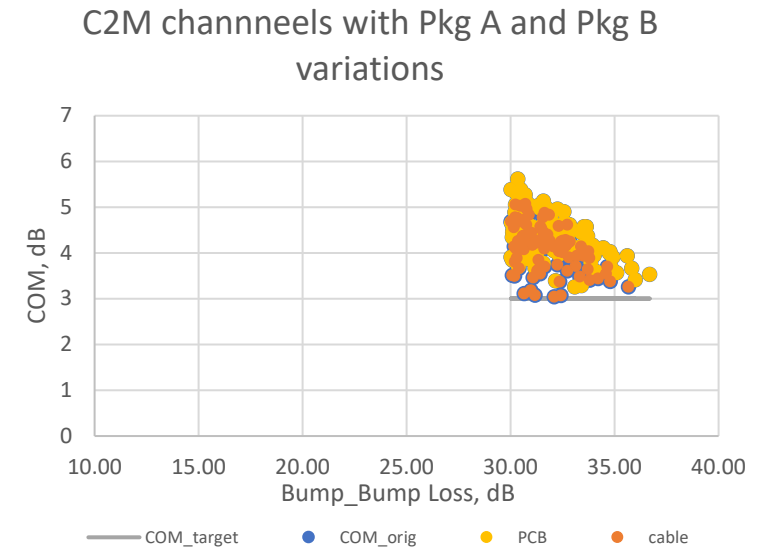
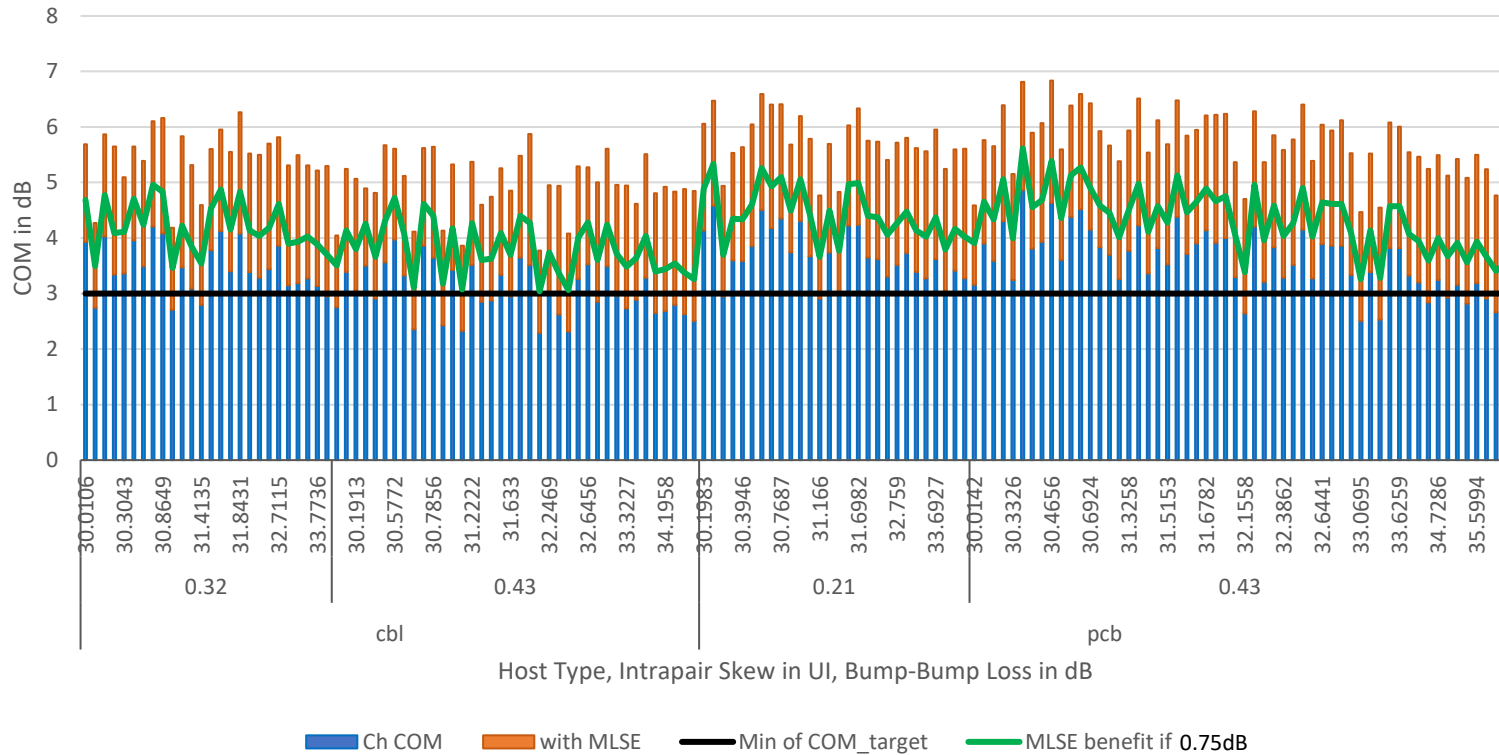
40 post tap FFE: 8 fixed+ 8 banks of 4 floating up to **60UI**

4 pre-tap

Observation: CTLE is adopting to lower range of capability. gDC : upto -7 dB



# C2M Channel Analysis w MLSE – all conditions for channels >30 dB



This type of ref. Serdes is covering up to 32 dB of cabled host channels and up to 34 dB of PCB host channels

# Conclusions

- For varying package conditions and max feasible system intrapair skew conditions, the same reference Serdes can support:
  - Cabled\_host channels up to 32 dB
  - PCB\_host channels up to 34 dB
- Recommend C2M Electrical Interfaces target max Loss up to 34dB.
- There is room for further simplification of Ref. Rx or additional noise margins based on future work – like the implementation of MMSE algorithms etc..

## Ref Serdes without MLSE:

TX:

A\_v: 0.45V with Rd =50 Ohm

4 pre-tap

CTLE:

gDC =-10 dB; gDC\_HP = -4 dB

RX:

1 Tap DFE

40 post tap FFE: 8 fixed+ 8 banks of 4 floating up to 80UI

4 pre-tap

## Ref Serdes (with MLSE, max benefit capped at 0.75dB):

TX:

A\_v: **0.413V** with Rd =50 Ohm

4 pre-tap

CTLE:

gDC =-10 dB; gDC\_HP = -4 dB

RX:

1 Tap DFE

40 post tap FFE: 8 fixed+ 8 banks of 4 floating up to **60UI**

4 pre-tap

# Backup



# COM Configuration file with Package A

Table 93A-1 parameters				
Parameter	Setting	Units	Information	
f_b	106.25	Gbd		
f_min	0.05	GHz		
Delta_f	0.01	GHz		
C_d	[0.4e-4 0.9e-4 1.1e-4; 0.4e-4 0.9e-4 1.1e-4]	nF		[TX RX]
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH		[TX RX]
C_b	[0.3e-4 0.3e-4]	nF		[TX RX]
z_p_select	[1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18]			[test cases to run]
z_p (TX)	[8 15 24 30 40 45 8 15 24 30 40 45 8 15 24 30 40 45; 1.8]	mm		[test cases]
z_p (NEXT)	[4 4 4 4 4 8 8 8 8 8 12 12 12 12 12 12; 0]	mm		[test cases]
z_p (FEXT)	[8 15 24 30 40 45 8 15 24 30 40 45 8 15 24 30 40 45; 1.8]	mm		[test cases]
z_p (RX)	[4 4 4 4 4 8 8 8 8 8 12 12 12 12 12 12; 0]	mm		[test cases]
PKG_Tx_FFE_preset	0			
C_p	[0.5e-4 0.5e-4]	nF		[TX RX]
R_0	50	Ohm		
R_d	[50 50]	Ohm		[TX RX]
A_v	0.45	V		vp/vf=
A_fe	0.45	V		vp/vf=
A_ne	0.45	V		
L	4			
M	32			
filter and Eq				
f_r	0.75	*fb		
c(0)	0.54			min
c(-1)	[-0.4:0.02:-0.3]		[-0.4:0.02:0]	[min:step:max]
c(-2)	[0:0.02:0.04]		[0:0.02:0.2]	[min:step:max]
c(-3)	[-0.04:0.02:0]		[-0.04:0.02:0]	[min:step:max]
c(-4)	[-0.02:0.02:0.04]		[0.02:0.02:0.02]	[min:step:max]
c(1)	[-0.04:0.02:0.04]		[-0.12:0.02:0.04]	[min:step:max]
N_b	1	UI		
b_max(1)	1			As/dffe1
b_max(2...N-b)	[0.3 0.2*ones(1,22)]			As/dffe2...N_b
b_min(1)	0			As/dffe1
b_min(2...N-b)	[-0.2 - 0.2*ones(1,22)]			As/dffe2...N_b
g_DC	[-20:1:0]	dB		[min:step:max]
f_z	42.5	GHz		
f_p1	42.5	GHz		
f_p2	106.25	GHz		
g_DC_HP	[-6:1:0]			[min:step:max]
f_HP_PZ	1.328125	GHz		
Butterworth	1	logical		include in fr
Raised_Cosine	0	logical		include in fr
RC_Start	6.70E+10	Hz		start freq for RCos
RC_end	7.97E+10	Hz		end freq for RCos

ffe_pre_tap_len	4	UI	
ffe_post_tap_len	8	UI	
ffe_tap_step_size	0		
ffe_main_cursor_min	0		
ffe_pre_tap1_max	0.7		
ffe_post_tap1_max	0.7		
ffe_tapn_max	0.7		
ffe_backoff	0		

Sample adjustment	[0 0]	phase	
ts_anchor	0		

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\C2M_A (date)\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	C2M_A	
COM_CONTRIBUTION	0	logical
Operational		
ERL Pass threshold	9.7	dB
COM Pass threshold	3	db
VEC Pass threshold	10.69073041	db
DER_0	2.67E-05	
T_r	4.00E-03	ns
FORCE_TR	1	logical
PMD_type	C2Mcom	
EW	1	
TDR and ERL options		logical
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	2000	logical
TDR Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	0	
fixture delay time	[0 0]	
Tukey_Window	1	
Noise_jitter		UI
sigma_RJ	0.01	UI
A_DD	0.02	V^2/GHz
eta_0	6.00E-09	dB
SNR_TX	33	
R_LM	0.95	

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highlighted are under re-consideration

MLSE	1	
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AC\_CM\_RMS 0

Table 93A-3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[5e-4 8.9e-4 2e-4]	
package_tl_tau	0.006141	ns/mm
package_Z_c	[87.5 87.5; 92.5 92.5]	Ohm

Table 93A-3 parameters		
Parameter	Setting	Units
board_tl_gamma0_a1_a2	[0 6.44084e-4 3.6036e-05]	1.5 db/in @ 56G
board_tl_tau	5.790E-03	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	125	mm
z_bp (NEXT)	0	mm
z_bp (FEXT)	125	mm
z_bp (RX)	0	mm
C_0	[0.2e-4 0]	nF
C_1	[0.2e-4 0]	nF
<b>Include PCB</b>	<b>0</b>	<b>logical</b>

Seleltions (rectangle, gaussian, dual_rayleigh, triangle)		
Histogram_Window_Weight	gaussian	selection
Qr	0.02	UI

ICN parameters		
f_v	0.594	Fb
f_f	0.594	Fb
f_n	0.594	Fb
f_2	79.688	GHz
A_ft	0.450	V
A_nt	0.450	V

Floating Tap Control		
N_bg	8	0 1 2 or 3 groups
N_bf	4	taps per group
N_f	80	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps
B float_RSS_MAX	0.1	rss tail tap limit
N_tail_start	61	(UI) start of tail tap limit

Receiver testing		
RX_CALIBRATION	0	logical
Sigma_BBN_step	5.00E-03	V