Intrapair Skew Considerations for 224Gbps/lane Electrical signaling

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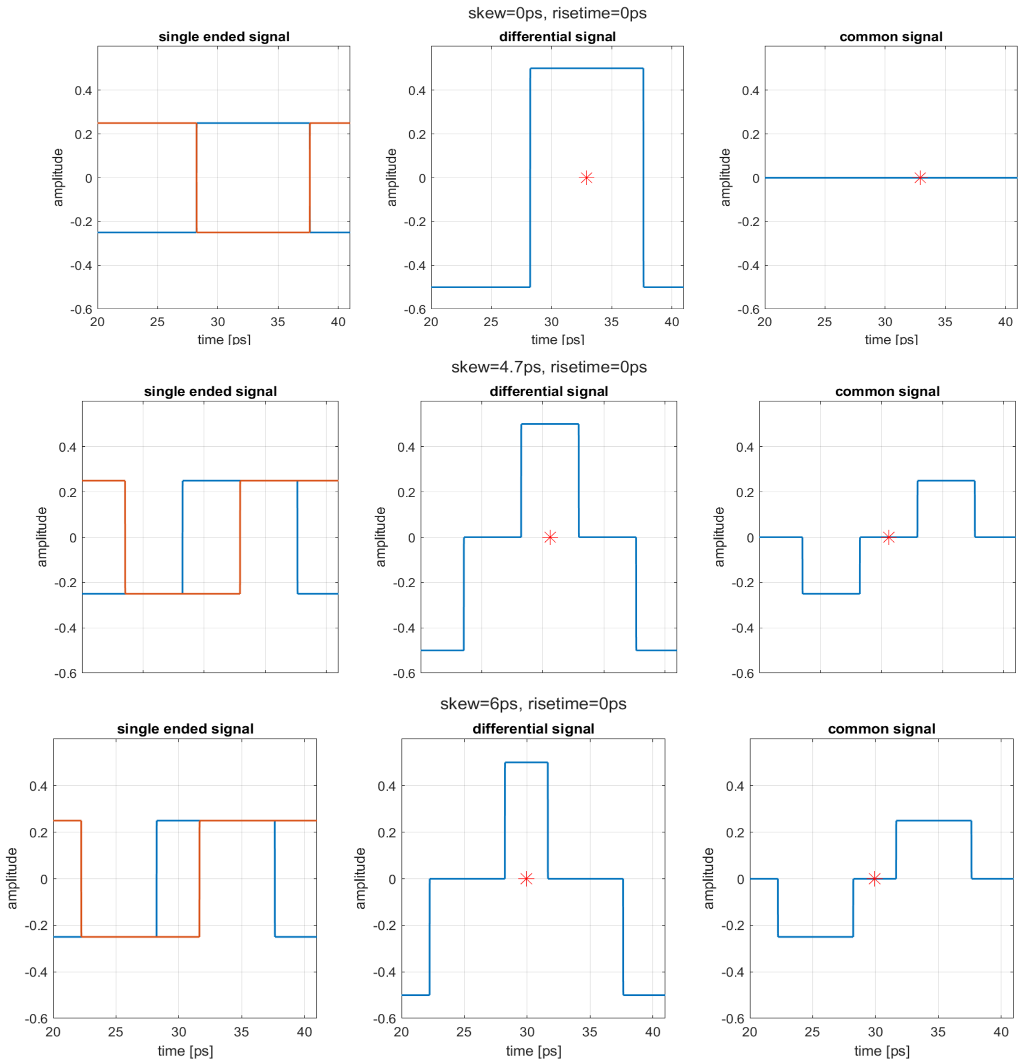
Overview

- Introduction and essential Ideas
- Impact of Intrapair skew
- Types of systems and Skew considerations
- Summary

Introduction - Essential Ideas

- Most High-speed Electrical Interfaces use differential signaling for high noise immunity compared to single ended signaling, except for some ultra short reaches, where noise conditions can be better controlled.
- In differential signaling:
    - True signal and equal and complementary signal is generated by transmitter and drives the two conductors of the differential pair of the channel.
    - These signals arrives at the receiver differential amplifier after passing through channel and analog front end (AFE), where a difference signal is built cancelling the noise picked up along the way equally by these two conductors
- Intrapair skew refers to the difference in time or phase between two signals that are supposed to be identical but complementary. This difference can occur due to factors such as variations in trace lengths, differences in propagation delays, or other physical or design-related factors . From here onwards we refer intrapair skew, simply as skew for convenience
- The data signals are supposed to arrive at the same time for proper cancellation of common-mode noise and signal recovery. When there is a skew, the signals do not arrive exactly at the same time, which means that the noise cancellation is not perfect, leading to potential signal integrity issues, reduced noise margins and Serdes performance and thus increases the bit error rate (BER) of a system.

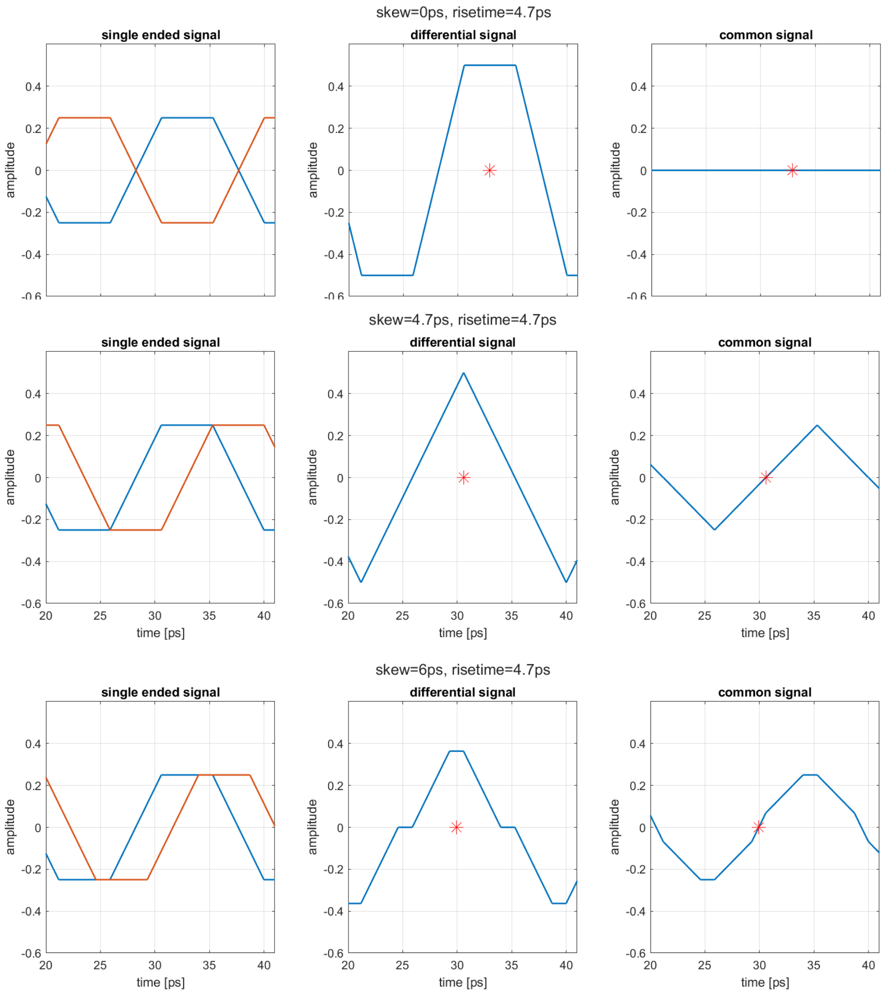
Skew impact – Ideal square pulse



Square Pulse:
UI: 9.4ps for 212.5 Gbps data rate.

- As the skew approaches to 0.5 UI the difference signal width reduces
- If the skew is 1 UI, the difference signal would be null signal
- Note corresponding Common mode signal profiles

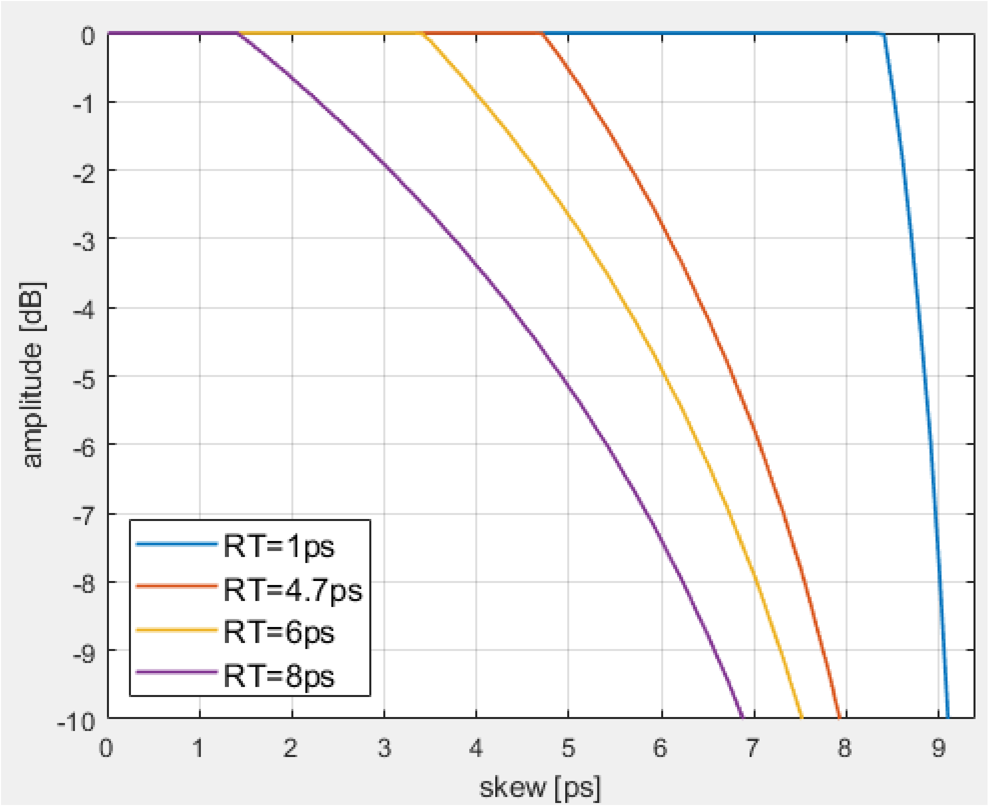
Skew impact – Pulse with Rise/Fall ramps



Pulse:
UI: 9.4ps for 212.5 Gbps data rate.

- As the skew approaches to 0.5 UI the difference signal width reduces
- Once skew goes above 0.5 UI not only difference signal width reduces its amplitude also reduces
- If the skew is 1 UI, the difference signal would be null signal
- Note corresponding Common mode signal profiles

Skew impact – Rise/Fall time and skew

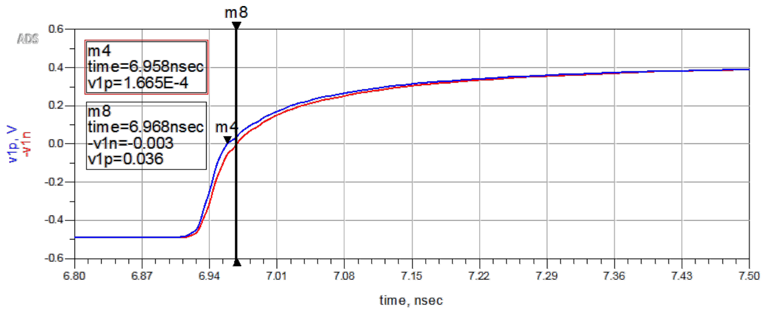


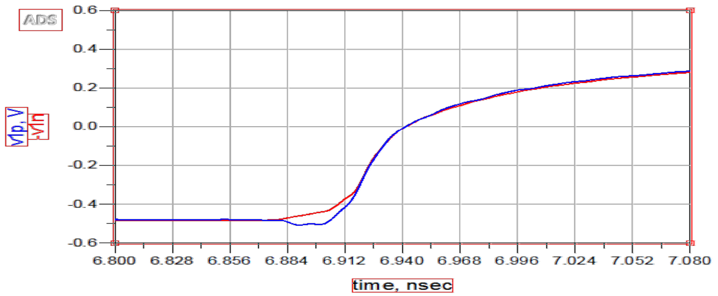
Pulse:
UI: 9.4ps for 212.5 Gbps data rate.

- For all cases, If the skew is 1 UI, the difference signal would be null.
- As rise/fall time increases, the skew impact on difference signal amplitude becomes more significant.

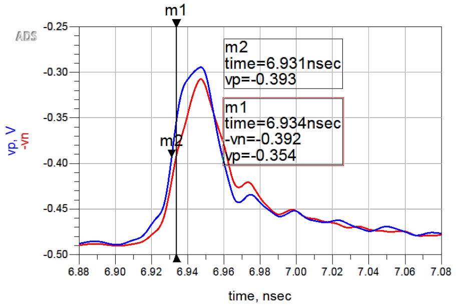
Skew impact – Time domain profiles

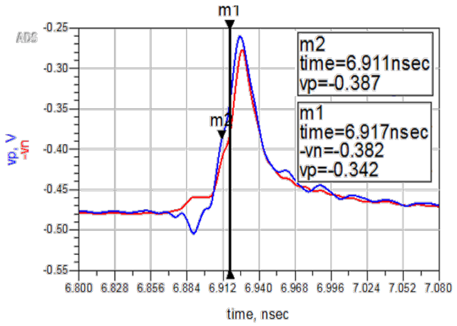
Step Response





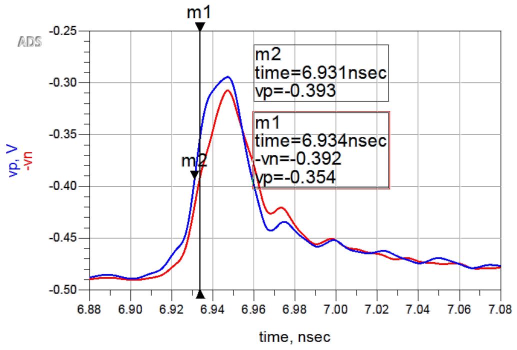
Pulse Response

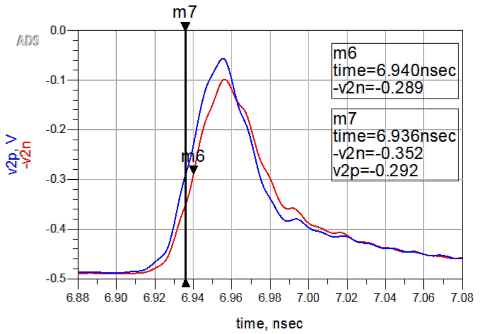


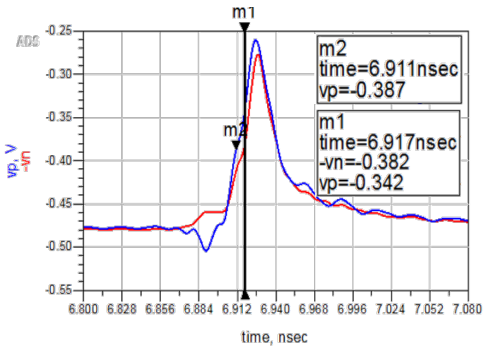


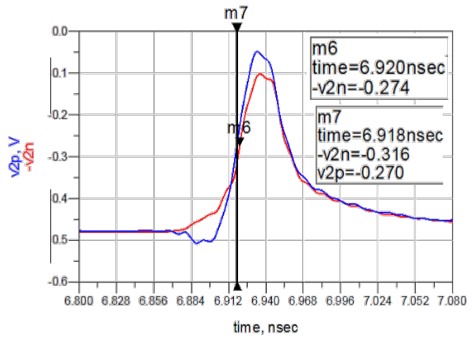
- Step response doesn't reveal adequate information about the skew time domain profile. Pulse response is more useful.

Skew impact – Time domain profiles









- Skew can occur due to various factors such as
  - differences in trace length,
  - impedance mismatches,
  - temperature variations,
  - manufacturing tolerances, and propagation delays.
  - Construction elements – like fabric weave, dielectric variation in different dimensions etc.. (too many to list here)
- These factors not only impact the delay between true and complementary signals and their respective signal profiles

System construction types

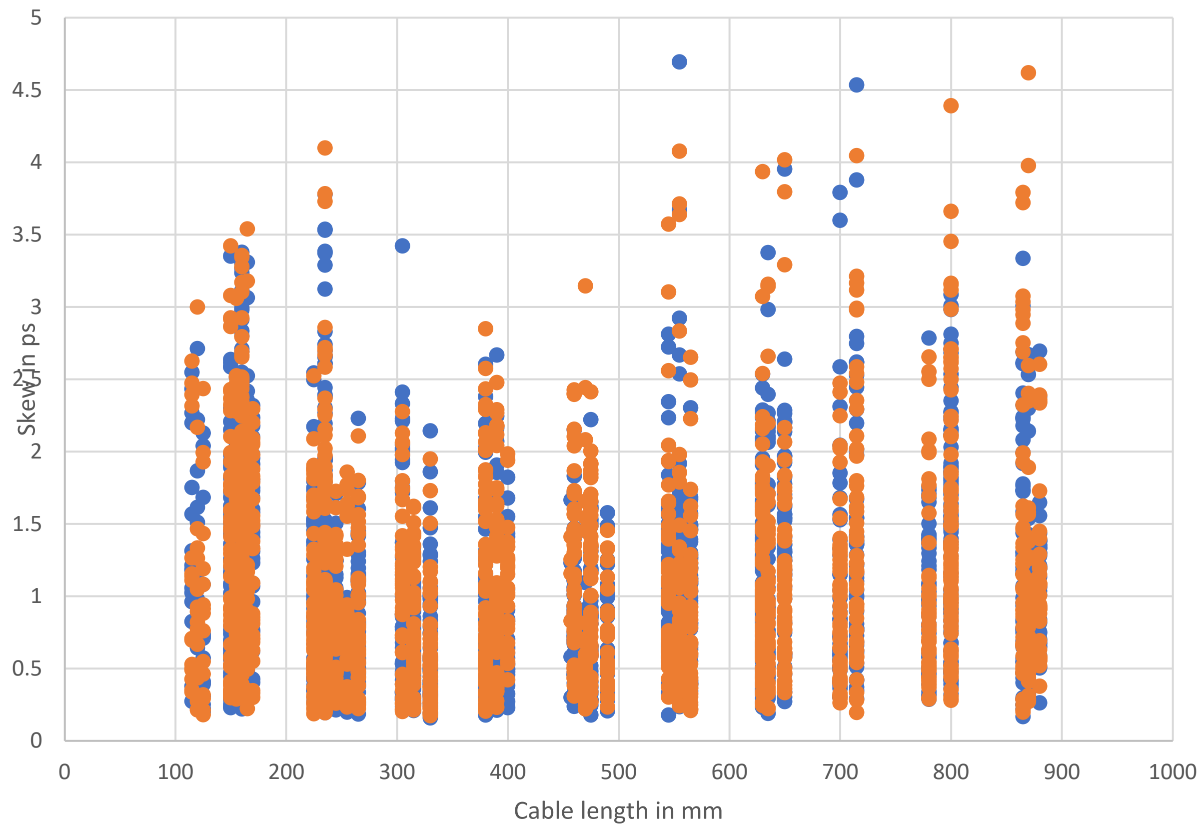
- Systems constructions in broad context can be categorized in to two.
    - Rigid construction
    - Semi-rigid construction
- Rigid constructions are typically multi-layered structures where signal conductors and their reference plane are built into these layers. These multilayered structures are then assembled with various assembly processes and /or Connectors to build a final system. These are planar structures in nature. e.g., Silicon die, Chip package substrates, PCBs
- In Semi-rigid construction some or portions of rigid structures in a system are substituted by flexible cylindrical structures like copper twin-ax cables. These cables are terminated to rigid structures either directly in the assembly or with connectors.

System construction types – skew contribution

- Effective Skew compensation techniques differ to each construction type.
- In rigid structures: like PCBs
  - to most extent the skew contribution can be quantified for each sub structure and one can try to compensate for it in other sub-structures – not only for physical length match but also for electrical length matching.
  - Skew mitigation by tightly coupling the conductors in the differential is difficult as max coupling that can achieved is limited to approx. 10% in high connectivity and dense designs.
  - Some level of statistical skew coming from glass fabric weave effects, DE variations needs to be budgeted in the design as they cannot be accurately quantified per instance due to instance to instance variation
- In semi-rigid structures: like Cables
  - loss contributions are much lower compared to rigid structures
  - Much higher coupling between differential conductors can be archived to reduce skew

  But
  - It is difficult to quantify these types of substructure skew contributions as it differs per instance to instance. i.e., cable segment to cable segment, or cable to cable in the same design (or system to system).
  - Poses additional skew and other impairments under stress conditions like Bend and twist, higher temp and humidity
  - Much higher level of statistical skew contribution budget needs to be allocated into the design for the stress conditions.
  - Cable skew tend to be not linearly distributed over length of the cable (see the next slide)

System construction types – skew contribution



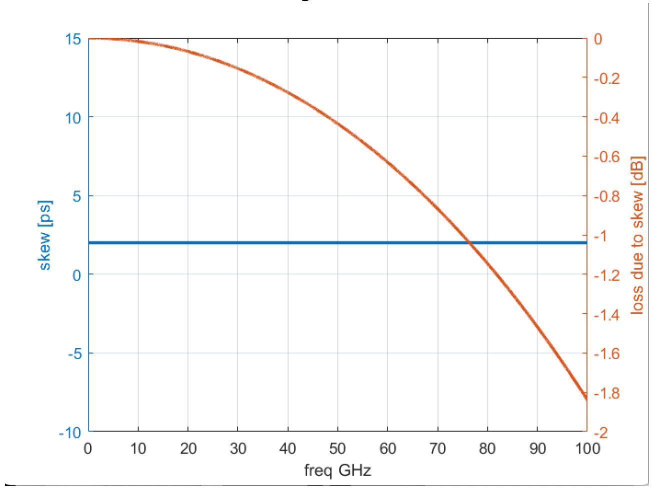
skew varies :

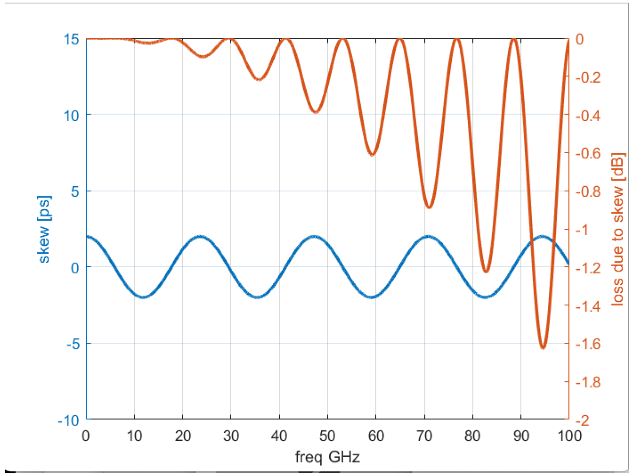
- Instance to instance of Cable segment
- Skew contribution is not linearly related to length of the cable

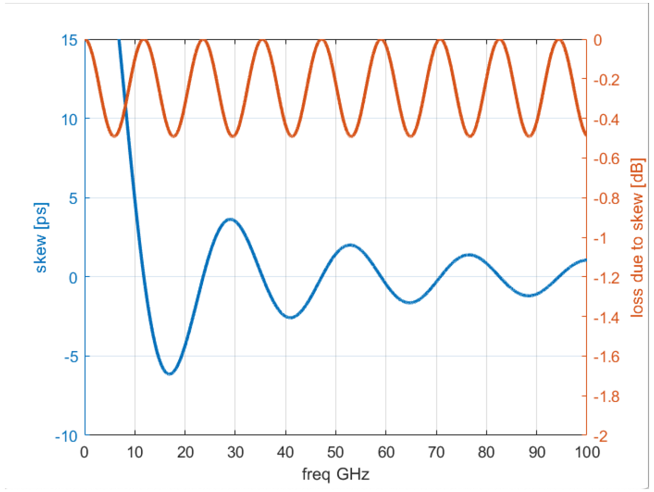
System construction types – Freq. Domain profiles

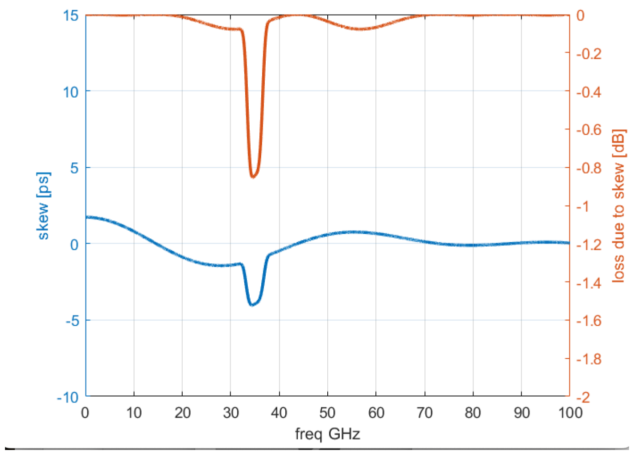
- Rigid structures tend to have different skew profiles compared to semi-rigid structures and each Construction type poses different types of limitations in controlling the skew.
- These differences somewhat difficult to notice or distinguish in time domain , but can be observed better in frequency domain
- Freq. domain skew profiles exhibit 4 basic types of profiles- see next slide
- Each channel skew profile is combinations of these basic profiles and depends on type of construction and stress conditions subjected on these structures.

Basic Freq. Domain profiles - Basic



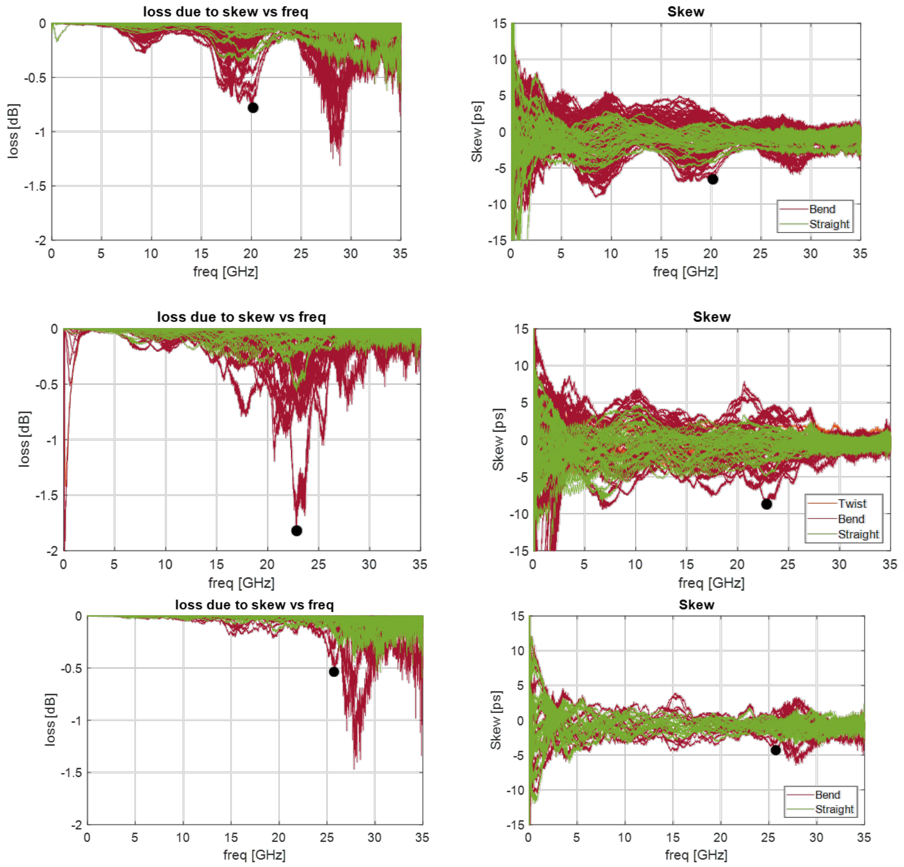




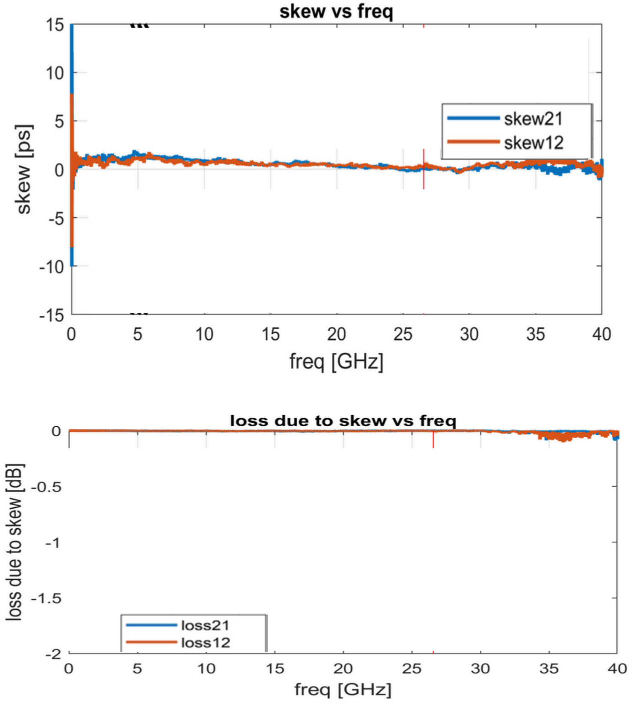


Basic skew profiles

Freq. Domain profiles of real channel components - measurements

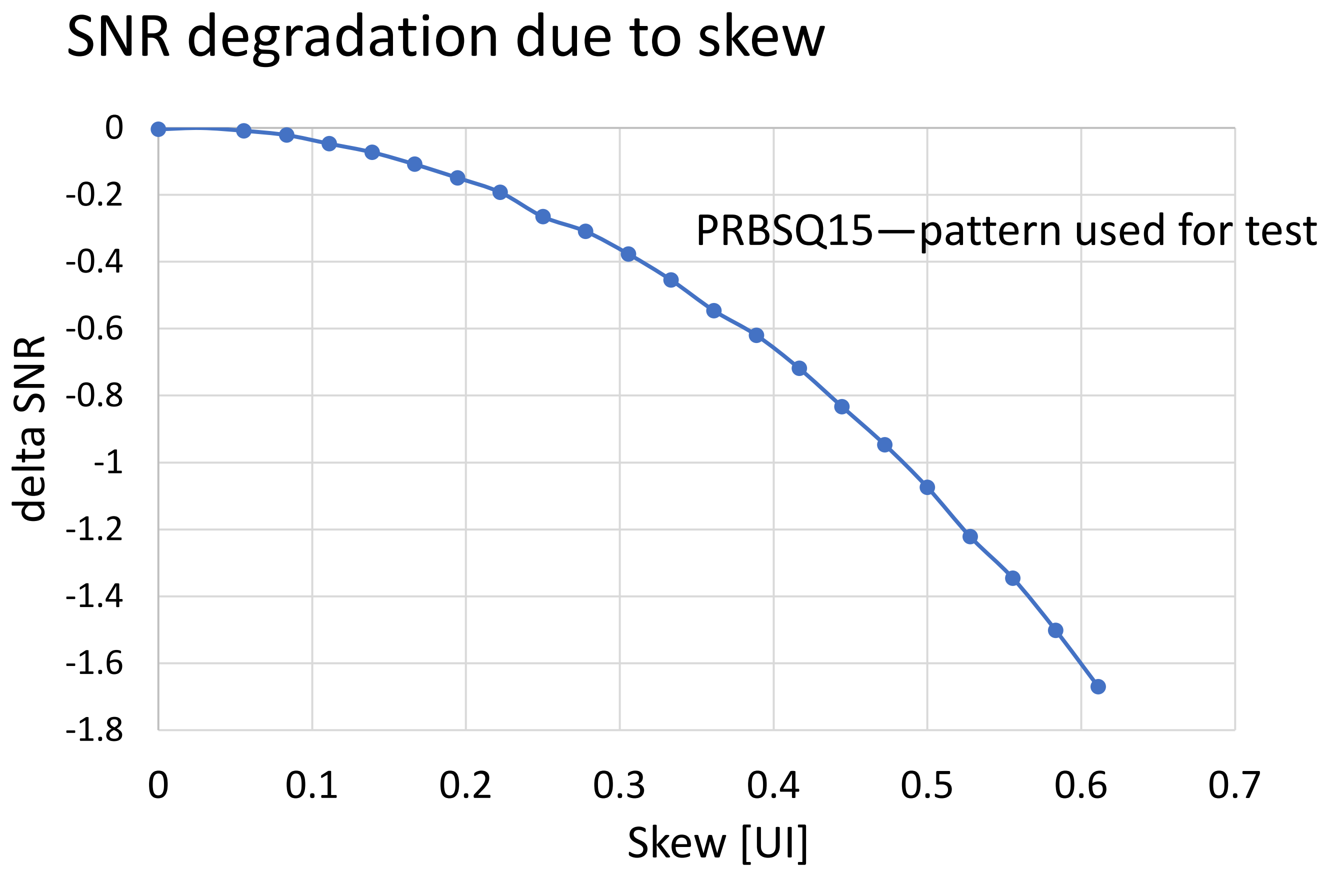


Example of Semi- Rigid structure (Cables) skew profiles



Example of Rigid structure(PCB) skew profiles

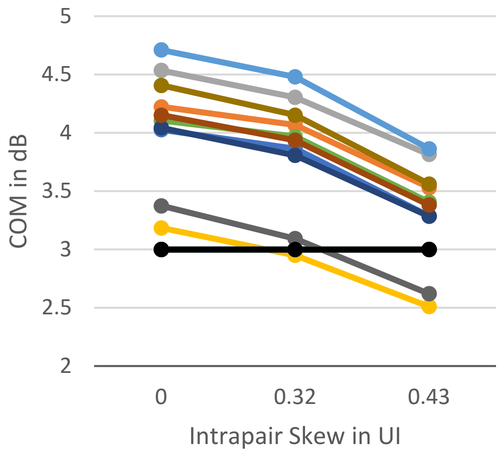
Skew Impact on Serdes performance



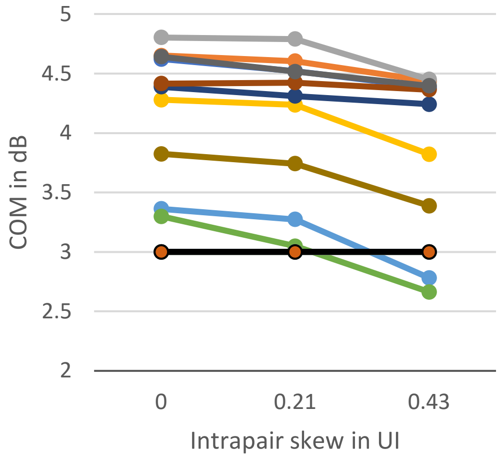
- Bit-by-bit simulation with Jitter and Noise introduced with similar limits in the 802.3ck project
- Base lined with BER of 1e-7 as zero delta SNR (y-axis)
- Accounting for the end-to-end skew of 0.3 UI to 0.4 UI seems a reasonable starting point.
- The working group needs to agree on how much of a skew level the reference receiver must handle.

Skew Impact in COM Tool – on some of contributed channels

SL.NO	Intrapair Skew	0.0 UI			0.32UI	0.43 UI
	Channel File Name	ICN, mv	FOM_ILD	Ball_Ball Insertion Loss, dB/COM values, dB		
1	cbl_hst_S4_B2B_s0nl0_Ms1_9_t	4.32	0.20	9.0872/4.1057	10.169/3.9677	11.1061/3.4067
2	cbl_hst_S4_B2B_s0nl0_Ms11_11_t	3.64	0.19	10.6728/4.0439	11.7545/3.8071	12.6915/3.286
3	cbl_hst_S4_B2B_s0nl0_Ml2_11_t	3.59	0.19	10.8259/4.5344	11.9078/4.3038	12.845/3.8149
4	cbl_hst_S4_B2B_s0nl0_Ms13_13_t	3.24	0.17	12.3942/4.1514	13.4754/3.9365	14.4122/3.3815
5	cbl_hst_S4_B2B_s0nl0_Ml12_13_t	3.01	0.19	12.4141/4.2225	13.4959/4.0685	14.433/3.5305
6	cbl_hst_S4_B2B_s0nl0_Ms7_15_t	2.63	0.17	15.1212/4.4065	16.2018/4.1522	17.1384/3.5612
7	cbl_hst_S4_B2B_s0nl0_Ml6_15_t	2.41	0.17	15.3775/4.7111	16.4568/4.4805	17.3928/3.8628
8	cbl_hst_S4_B2B_s0nl0_Ml10_18_t	1.90	0.16	18.286/4.027	19.3681/3.8628	20.3054/3.2862
9	cbl_hst_S4_B2B_s0nl0_Ms18_18_t	2.10	0.16	18.5097/3.374	19.59/3.0927	20.5264/2.6205
10	cbl_hst_S4_B2B_s0nl0_Ml20_20_t	1.67	0.16	19.9252/3.1853	21.0069/2.9504	21.944/2.5104



SL.NO	Intrapair Skew	0.0 UI			0.21UI	0.43 UI
	Channel File Name	ICN, mv	FOM_ILD	Ball_Ball Insertion Loss, dB/COM values, dB		
1	pcb_hst_S4_B2B_s0nl0_Ms21_9_t	4.45	0.20	9.0691/4.3895	9.5286/4.3113	11.092/4.2427
2	pcb_hst_S4_B2B_s0nl0_Ms23_10_t	3.91	0.18	10.3062/4.4163	10.7662/4.4246	12.33/4.3649
3	pcb_hst_S4_B2B_s0nl0_Ml22_10_t	3.70	0.20	10.8312/4.6214	11.2908/4.5216	12.8543/4.3823
4	pcb_hst_S4_B2B_s0nl0_Ms25_12_t	3.45	0.17	11.5466/4.6425	12.007/4.5171	13.5715/4.3968
5	pcb_hst_S4_B2B_s0nl0_Ml24_12_t	3.24	0.18	12.061/4.651	12.5211/4.6043	14.085/4.4366
6	pcb_hst_S4_B2B_s0nl0_Ml28_16_t	2.52	0.16	15.0013/4.8037	15.4615/4.7901	17.0256/4.4511
7	pcb_hst_S4_B2B_s0nl0_Ms33_18_t	2.28	0.16	17.6729/3.8244	18.1331/3.7417	19.6972/3.3882
8	pcb_hst_S4_B2B_s0nl0_Ml32_18_t	2.01	0.16	17.9419/4.2792	18.4021/4.2366	19.9664/3.8223
9	pcb_hst_S4_B2B_s0nl0_Ms19_20_t	2.01	0.17	20.4587/3.2989	20.9188/3.0485	22.483/2.6624
10	pcb_hst_S4_B2B_s0nl0_Ml36_20_t	1.66	0.16	20.9862/3.3626	21.4463/3.2735	23.0104/2.7813



COM values :Worst case values with Package types A and B with Host ASIC package traces 8mm-45mm and Module Package traces 4mm-12mm

Skew – Silicon (Serdes) role

- Skew can also be introduced in Silicon analog paths both in Transmitter and Receiver analog paths and circuits.
- Silicon can also help with skew compensating circuits. Some of such solutions are:
  - Tunable Delay line on one of the differential legs
  - Tunable matching filter to compensate for skew (see loss due to skew in freq. domain
  - Pre-emphasis and de emphasis can help reduce the impact of skew
  - All these solutions comes at the cost of either additional power or reduced Serdes performance and with a difficult task of tuning them for varying skew due to system stress conditions like temperature, cable bend and twist etc..

Summary

- As we address higher data rates, the Unit interval (UI) reduces, and the percentage of intrapair skew level w.r.t UI becomes higher. It impacts Highspeed Serdes performance significantly
- Skew is contributed from every part of the serial link . i.e., Silicon, Packages, and system channel
- Different types of skew profiles are observed from different categories of system constructions.
- Active skew compensation solutions shall be considered to reduce the skew impact, although such solutions are expected to come at a cost.
- System design must budget for a certain skew tolerance to allow manufacturing, assembly, and environmental variations.
- The working group shall determine how much a skew level the reference receiver must handle. Suggest 0.3 UI to 0.4 UI as a starting point.

Backup

COM Configuration file with Package B

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18]		[test cases to run]
z_p (TX)	[8 15 24 30 40 45 8 15 24 30 40 45 8 15 24 30 40 45;1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1; 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 ; 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5]	mm	[test cases]
z_p (NEXT)	[4 4 4 4 4 4 8 8 8 8 8 8 12 12 12 12 12 12; 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0; 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ;0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0]	mm	[test cases]
z_p (FEXT)	[8 15 24 30 40 45 8 15 24 30 40 45 8 15 24 30 40 45;1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1; 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 ; 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5 0.5]	mm	[test cases]
z_p (RX)	[4 4 4 4 4 4 8 8 8 8 8 8 12 12 12 12 12 12; 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0; 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 ;0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0]	mm	[test cases]
PKG_Tx_FFE_preset	0		
C_p	[0.5e-4 0.5e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.45	V	vp/vf=
A_fe	0.45	V	vp/vf=
A_ne	0.45	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.4:0.02:-0.3]	[-0.4:0.02:0]	[min:step:max]
c(-2)	[0:0.02:0.04]	[0:0.02:0.2]	[min:step:max]
c(-3)	[-0.04:0.02:0]	[-0.04:0.02:0]	[min:step:max]
c(-4)	[-0.02:0.02:0.04]	[0.02:0.02:0.02]	[min:step:max]
c(1)	[-0.04:0.02:0.04]	[-0.12:0.02:0.04]	[min:step:max]
N_b	1	UI	
b_max(1)	1		As/dffe1
b_max(2...N-b)	[0.3 0.2*ones(1,22)]		As/dffe2...N_b
b_min(1)	0		As/dffe1
b_min(2...N-b)	[-0.2 - 0.2*ones(1,22)]		As/dffe2...N_b
g_DC	[-10:1:0]	dB	[min:step:max]
f_z	42.5	GHz	
f_p1	42.5	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-4:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
Butterworth	1	logical	include in fr
Raised_Cosine	0	logical	include in fr
RC_Start	6.70E+10	Hz	start freq for RCos
RC_end	7.97E+10	Hz	end freq for RCos

ffe_pre_tap_len	4	UI	
ffe_post_tap_len	8	UI	
ffe_tap_step_size	0		
ffe_main_cursor_min	0		
ffe_pre_tap1_max	0.7		
ffe_post_tap1_max	0.7		
ffe_tapn_max	0.7		
ffe_backoff	0		

Sample adjustment	[0 0]	phase	
ts_anchor	0		

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\C2M_B_{date}\	
SAVE_FIGURES	0	logical
Port Order	**[1 3 2 4]**	
RUNTAG	C2M_B	
COM_CONTRIBUTION	0	logical
Operational		
ERL Pass threshold	9.7	dB
COM Pass threshold	3	db
VEC Pass threshold	10.69073041	db
DER_0	2.67E-05	
T_r	4.00E-03	ns
FORCE_TR	1	logical
PMD_type	C2Mcom	
EW	1	
TDR and ERL options		logical
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	2000	logical
TDR_Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	0	
fixture delay time	[0 0]	
Tukey_Window	1	
Noise, jitter		UI
sigma_RJ	0.01	UI
A_DD	0.02	V^2/GHz
eta_0	6.00E-09	dB
SNR_TX	33	
R_LM	0.95	
11-2022 BenArtsi pkg	oif2022.065.02	

highlighted are under re-consideration

MLSE	1	

AC_CM_RMS 0

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0008455 0.000340225]	
package_tl_tau	0.00644805	ns/mm
package_Z_c	[92 92 ; 70 70; 80 80; 100 100]	Ohm

Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 6.44084e-4 3.6036e-05]*	1.5 db/in @ 56G
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*125*	mm
z_bp (NEXT)	*0*	mm
z_bp (FEXT)	*125*	mm
z_bp (RX)	*0*	mm
C_0	[0.2e-4 0]	nF
C_1	[0.2e-4 0]	nF
Include PCB	**0**	**logical**

Seletions (rectangle, gaussian,dual_rayleigh,triangle		
Histogram_Window_Weight	gaussian	selection
Qr	*0.02*	UI

ICN parameters		
f_v	0.594	Fb
f_f	0.594	Fb
f_n	0.594	Fb
f_2	79.688	GHz
A_ft	0.450	V
A_nt	0.450	V

Floating Tap Control		
N_bg	8	0 1 2 or 3 groups
N_bf	4	taps per group
N_f	80	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps
B_float_RSS_MAX	0.1	rss tail tap limit
N_tail_start	61	(UI) start of tail taps limit

Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

COM Configuration file with Package A

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18]		[test cases to run]
z_p (TX)	[8 15 24 30 40 45 8 15 24 30 40 45 8 15 24 30 40 45;1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[4 4 4 4 4 4 8 8 8 8 8 8 12 12 12 12 12 12; 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0]	mm	[test cases]
z_p (FEXT)	[8 15 24 30 40 45 8 15 24 30 40 45 8 15 24 30 40 45;1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8]	mm	[test cases]
z_p (RX)	[4 4 4 4 4 4 8 8 8 8 8 8 12 12 12 12 12 12; 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0]	mm	[test cases]
PKG_Tx_FFE_preset	0		
C_p	[0.5e-4 0.5e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.45	V	vp/vf=
A_fe	0.45	V	vp/vf=
A_ne	0.45	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.4:0.02:-0.3]	[-0.4:0.02:0]	[min:step:max]
c(-2)	[0:0.02:0.04]	[0:0.02:0.2]	[min:step:max]
c(-3)	[-0.04:0.02:0]	[-0.04:0.02:0]	[min:step:max]
c(-4)	[-0.02:0.02:0.04]	[0.02:0.02:0.02]	[min:step:max]
c(1)	[-0.04:0.02:0.04]	[-0.12:0.02:0.04]	[min:step:max]
N_b	1	UI	
b_max(1)	1		As/dffe1
b_max(2...N-b)	[0.3 0.2*ones(1,22)]		As/dffe2...N_b
b_min(1)	0		As/dffe1
b_min(2...N-b)	[-0.2 - 0.2*ones(1,22)]		As/dffe2...N_b
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	42.5	GHz	
f_p1	42.5	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
Butterworth	1	logical	include in fr
Raised_Cosine	0	logical	include in fr
RC_Start	6.70E+10	Hz	start freq for RCos
RC_end	7.97E+10	Hz	end freq for RCos
ffe_pre_tap_len	4	UI	
ffe_post_tap_len	8	UI	
ffe_tap_step_size	0		
ffe_main_cursor_min	0		
ffe_pre_tap1_max	0.7		
ffe_post_tap1_max	0.7		
ffe_tapn_max	0.7		
ffe_backoff	0		
Sample adjustment	[0 0]	phase	
ts_anchor	0		

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\C2M_A_{date}\	
SAVE_FIGURES	0	logical
Port Order	**[1 3 2 4]**	
RUNTAG	C2M_A	
COM_CONTRIBUTION	0	logical
Operational		
ERL Pass threshold	9.7	dB
COM Pass threshold	3	db
VEC Pass threshold	10.69073041	db
DER_0	2.67E-05	
T_r	4.00E-03	ns
FORCE_TR	1	logical
PMD_type	C2Mcom	
EW	1	
TDR and ERL options		logical
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	2000	logical
TDR_Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	0	
fixture delay time	[0 0]	
Tukey_Window	1	
Noise, jitter		UI
sigma_RJ	0.01	UI
A_DD	0.02	V^2/GHz
eta_0	6.00E-09	dB
SNR_TX	33	
R_LM	0.95	
11-2022 BenArtsi pkg	oif2022.065.02	

highlighted are under re-consideration

MLSE	1	

AC_CM_RMS 0

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[5e-4 8.9e-4 2e-4]	
package_tl_tau	0.006141	ns/mm
package_Z_c	[87.5 87.5;92.5 92.5]	Ohm
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 6.44084e-4 3.6036e-05]*	1.5 db/in @56G
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*125*	mm
z_bp (NEXT)	*0*	mm
z_bp (FEXT)	*125*	mm
z_bp (RX)	*0*	mm
C_0	[0.2e-4 0]	nF
C_1	[0.2e-4 0]	nF
Include PCB	**0**	**logical**
Seletions (rectangle, gaussian,dual_rayleigh,triangle)		
Histogram_Window_Weight	gaussian	selection
Qr	*0.02*	UI
ICN parameters		
f_v	0.594	Fb
f_f	0.594	Fb
f_n	0.594	Fb
f_2	79.688	GHz
A_ft	0.450	V
A_nt	0.450	V
Floating Tap Control		
N_bg	8	0 1 2 or 3 groups
N_bf	4	taps per group
N_f	80	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps
B_float_RSS_MAX	0.1	rss tail tap limit
N_tail_start	61	(UI) start of tail tap limit
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V