Intrapair Skew Considerations for 224Gbps/lane Electrical signaling

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Overview

- Introduction and essential Ideas
- Impact of Intrapair skew
- Types of systems and Skew considerations
- Summary

Introduction - Essential Ideas

- Most High-speed Electrical Interfaces use differential signaling for high noise immunity compared to single ended signaling, except for some ultra short reaches, where noise conditions can be better controlled.
- In differential signaling:
 - True signal and equal and complementary signal is generated by transmitter and drives the two conductors of the differential pair of the channel.
 - These signals arrives at the receiver differential amplifier after passing through channel and analog front end (AFE), where a difference signal is built cancelling the noise picked up along the way equally by these two conductors
- Intrapair skew refers to the difference in time or phase between two signals that are supposed to be identical but complementary. This difference can occur due to factors such as variations in trace lengths, differences in propagation delays, or other physical or design-related factors. From here onwards we refer intrapair skew, simply as <u>skew</u> for convenience
- The data signals are supposed to arrive at the same time for proper cancellation of commonmode noise and signal recovery. When there is a skew, the signals do not arrive exactly at the same time, which means that the noise cancellation is not perfect, leading to potential signal integrity issues, reduced noise margins and Serdes performance and thus increases the bit error rate (BER) of a system.

Skew impact – Ideal square pulse



Square Pulse: UI: 9.4ps for 212.5 Gbps data rate.

- As the skew approaches to 0.5 UI the difference signal width reduces
- If the skew is 1 UI, the difference signal would be null signal
- Note corresponding Common mode signal profiles

Skew impact – Pulse with Rise/Fall ramps



Pulse:

UI: 9.4ps for 212.5 Gbps data rate.

- As the skew approaches to 0.5 UI the difference signal width reduces
- Once skew goes above 0.5 UI not only difference signal width reduces its amplitude also reduces
- If the skew is 1 UI, the difference signal would be null signal
- Note corresponding Common mode signal profiles

Skew impact – Rise/Fall time and skew



Pulse: UI: 9.4ps for 212.5 Gbps data rate.

- For all cases, If the skew is 1 UI, the difference signal would be null.
- As rise/fall time increases, the skew impact on difference signal amplitude becomes more significant.

Skew impact – Time domain profiles



Step Response

• Step response doesn't reveal adequate information about the skew time domain profile. Pulse response is more useful.

Skew impact – Time domain profiles



- Skew can occur due to various factors such as
 - differences in trace length,
 - impedance mismatches,
 - temperature variations,
 - manufacturing tolerances, and propagation delays.
 - Construction elements like fabric weave, dielectric variation in different dimensions etc.. (too many to list here)
- These factors not only impact the delay between true and complementary signals and their respective signal profiles

System construction types

- Systems constructions in broad context can be categorized in to two.
 - Rigid construction
 - Semi-rigid construction
- Rigid constructions are typically multi-layered structures where signal conductors and their reference plane are built into these layers. These multilayered structures are then assembled with various assembly processes and /or Connectors to build a final system. These are planar structures in nature. e.g., Silicon die, Chip package substrates, PCBs
- In Semi-rigid construction some or portions of rigid structures in a system are substituted by flexible cylindrical structures like copper twin-ax cables. These cables are terminated to rigid structures either directly in the assembly or with connectors.

System construction types – skew contribution

- Effective Skew compensation techniques differ to each construction type.
- In rigid structures: like PCBs
 - to most extent the skew contribution can be quantified for each sub structure and one can try to compensate for it in other sub-structures not only for physical length match but also for electrical length matching.
 - Skew mitigation by tightly coupling the conductors in the differential is difficult as max coupling that can achieved is limited to approx. 10% in high connectivity and dense designs.
 - Some level of statistical skew coming from glass fabric weave effects, DE variations needs to be budgeted in the design as they cannot be accurately quantified per instance due to instance to instance variation
- In semi-rigid structures: like Cables
 - loss contributions are much lower compared to rigid structures
 - Much higher coupling between differential conductors can be archived to reduce skew

But

- It is difficult to quantify these types of substructure skew contributions as it differs per instance to instance. i.e., cable segment to cable segment, or cable to cable in the same design (or system to system).
- Poses additional skew and other impairments under stress conditions like Bend and twist, higher temp and humidity
- Much higher level of statistical skew contribution budget needs to be allocated into the design for the stress conditions.
- Cable skew tend to be not linearly distributed over length of the cable (see the next slide)

System construction types – skew contribution



skew varies :

- Instance to instance of Cable segment
- Skew contribution is not linearly related to length of the cable

System construction types – Freq. Domain profiles

- Rigid structures tend to have different skew profiles compared to semi-rigid structures and each Construction type poses different types of limitations in controlling the skew.
- These differences somewhat difficult to notice or distinguish in time domain , but can be observed better in frequency domain
- Freq. domain skew profiles exhibit 4 basic types of profiles- see next slide
- Each channel skew profile is combinations of these basic profiles and depends on type of construction and stress conditions subjected on these structures.

Basic Freq. Domain profiles - Basic







Basic skew profiles

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Freq. Domain profiles of real channel components - measurements





Example of Rigid structure(PCB) skew profiles

Example of Semi- Rigid structure (Cables) skew profiles

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Skew Impact on Serdes performance



- Bit-by-bit simulation with Jitter and Noise introduced with similar limits in the 802.3ck project
- Base lined with BER of 1e-7 as zero delta SNR (y-axis)
- Accounting for the end-to-end skew of <u>0.3 UI to 0.4 UI</u> seems a reasonable starting point.
- The working group needs to agree on how much of a skew level the reference receiver must handle.

Skew Impact in COM Tool – on some of contributed channels

	Intrapair Skew		0	.0 UI	0.32UI	0.43 UI
SL.NO	Channel File Name	ICN, mv	FOM_ILD	Ball_Ba	ll Insertion Loss, dB/	COM values, dB
1	cbl_hst_S4_B2B_s0nl0_Ms1_9_t	4.32	0.20	9.0872/4.1057	10.169/3.9677	11.1061/3.4067
2	cbl_hst_S4_B2B_s0nl0_Ms11_11_t	3.64	0.19	10.6728/4.0439	11.7545/3.8071	12.6915/3.286
3	cbl_hst_S4_B2B_s0nl0_Ml2_11_t	3.59	0.19	10.8259/4.5344	11.9078/4.3038	12.845/3.8149
4	cbl_hst_S4_B2B_s0nl0_Ms13_13_t	3.24	0.17	12.3942/4.1514	13.4754/3.9365	14.4122/3.3815
5	cbl_hst_S4_B2B_s0nl0_Ml12_13_t	3.01	0.19	12.4141/4.2225	13.4959/4.0685	14.433/3.5305
6	cbl_hst_S4_B2B_s0nl0_Ms7_15_t	2.63	0.17	15.1212/4.4065	16.2018/4.1522	17.1384/3.5612
7	cbl_hst_S4_B2B_s0nl0_Ml6_15_t	2.41	0.17	15.3775/4.7111	16.4568/4.4805	17.3928/3.8628
8	cbl_hst_S4_B2B_s0nl0_Ml10_18_t	1.90	0.16	18.286/4.027	19.3681/3.8628	20.3054/3.2862
9	cbl_hst_S4_B2B_s0nl0_Ms18_18_t	2.10	0.16	18.5097/3.374	19.59/3.0927	20.5264/2.6205
10	cbl_hst_S4_B2B_s0nl0_Ml20_20_t	1.67	0.16	19.9252/3.1853	21.0069/2.9504	21.944/2.5104



	Intrapair Skew		0.0 UI		0.21UI	0.43 UI
SL.NO	Channel File Name	ICN, mv	FOM_ILD	Ball_Ba	l Insertion Loss, dB/COM values, dB	
1	pcb_hst_S4_B2B_s0nl0_Ms21_9_t	4.45	0.20	9.0691/4.3895	9.5286/4.3113	11.092/4.2427
2	pcb_hst_S4_B2B_s0nl0_Ms23_10_t	3.91	0.18	10.3062/4.4163	10.7662/4.4246	12.33/4.3649
3	pcb_hst_S4_B2B_s0nl0_Ml22_10_t	3.70	0.20	10.8312/4.6214	11.2908/4.5216	12.8543/4.3823
4	pcb_hst_S4_B2B_s0nl0_Ms25_12_t	3.45	0.17	11.5466/4.6425	12.007/4.5171	13.5715/4.3968
5	pcb_hst_S4_B2B_s0nl0_Ml24_12_t	3.24	0.18	12.061/4.651	12.5211/4.6043	14.085/4.4366
6	pcb_hst_S4_B2B_s0nl0_Ml28_16_t	2.52	0.16	15.0013/4.8037	15.4615/4.7901	17.0256/4.4511
7	pcb_hst_S4_B2B_s0nl0_Ms33_18_t	2.28	0.16	17.6729/3.8244	18.1331/3.7417	19.6972/3.3882
8	pcb_hst_S4_B2B_s0nl0_Ml32_18_t	2.01	0.16	17.9419/4.2792	18.4021/4.2366	19.9664/3.8223
9	pcb_hst_S4_B2B_s0nl0_Ms19_20_t	2.01	0.17	20.4587/3.2989	20.9188/3.0485	22.483/2.6624
10	pcb_hst_S4_B2B_s0nl0_Ml36_20_t	1.66	0.16	20.9862/3.3626	21.4463/3.2735	23.0104/2.7813



COM values :Worst case values with Package types A and B with Host ASIC package traces 8mm-45mm and Module Package traces 4mm-12mm

Skew – Silicon (Serdes) role

- Skew can also be introduced in Silicon analog paths both in Transmitter and Receiver analog paths and circuits.
- Silicon can also help with skew compensating circuits. Some of such solutions are:
 - Tunable Delay line on one of the differential legs
 - Tunable matching filter to compensate for skew (see loss due to skew in freq. domain
 - Pre-emphasis and de emphasis can help reduce the impact of skew
 - All these solutions comes at the cost of either additional power or reduced Serdes performance and with a difficult task of tuning them for varying skew due to system stress conditions like temperature, cable bend and twist etc..

Summary

- As we address higher data rates, the Unit interval (UI) reduces, and the percentage of intrapair skew level w.r.t UI becomes higher. It impacts Highspeed Serdes performance significantly
- Skew is contributed from every part of the serial link . i.e., Silicon, Packages, and system channel
- Different types of skew profiles are observed from different categories of system constructions.
- Active skew compensation solutions shall be considered to reduce the skew impact, although such solutions are expected to come at a cost.
- System design must budget for a certain skew tolerance to allow manufacturing, assembly, and environmental variations.
- The working group shall determine how much a skew level the reference receiver must handle. Suggest <u>0.3 UI to 0.4 UI as a starting point</u>.

Backup

COM Configuration file with Package B

Ļ	able 93A-1 parameters			
┢				
Г	Parameter	Setting	Units	Information
	fb	106.25	GBd	
t	fmin	0.05	GH2	1
H	<u> </u>	0.05	012	
F	Delta_f	0.01	GHZ	
	C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
Γ	L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]
	C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
	z_p select	[1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18]		[test cases to run
	z_p (TX)	[8 15 24 30 40 45 8 15 24 30 40 45 8 15 24 30 40 45;1 111 111 111 111 111 11 1;1 1111111111	mm	[test cases]
	z_p (NEXT)	[4444448888888121212121212 00000000000000000000	mm	[test cases]
	z_p (FEXT)	[8 15 24 30 40 45 8 15 24 30 40 45 8 15 24 30 40 45;1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1;1 1 1 1	mm	[test cases]
	z_p (RX)	[44 44 44 88 88 88 88 12 12 12 12 12 12 12 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	mm	[test cases]
F	PKG_Tx_FFE_preset	0		
	C_p	[0.5e-4 0.5e-4]	nF	[TX RX]
Γ	RO	50	Ohm	
t	<u> </u>	[50,50]	Ohm	[TY PV]
+	<u>~</u> u	[30 30]	UIIII	
F	A_v	0.45	V	vp/vt=
	A_fe	0.45	V	vp/vf=
	A_ne	0.45	v	
t	1	4		
t	M	22		
H	IVI Classes I.C.	52		
F	filter and Eq			
L	f_r	0.75	*fb	
Γ	c(0)	0.54		min
t	c(-1)	[-0.4:0.02:0.2]	[-0.4-0.02-0]	[min:ston:mov]
+	C(-1)	[-0.4:0.02:-0.3]	[-0.4:0.02:0]	[[min:step:max]
	c(-2)	[0:0.02:0.04]	[U:U.U2:0.2]	[[min:step:max]
F	0(-2)		1 0 04-0 02-01	[min:sten:max]
╞	c(-3)	[-0.04:0.02:0]	-0.04.0.02.01	
	c(-4)	[-0.04:0.02:0]	[0.02:0.02:0] [0.02]	[min:step:max]
	c(-3) c(-4) c(1)	[-0.04:0.02:0] [-0.02:0.02:0.04] [-0.04:0.02:0.04]	[0.02:0.02:0] [0.02:0.02:0. 02] [- 0.12:0.02:0.0 4]	[min:step:max]
	c(-3) c(-4) c(1) N b	[-0.04:0.02:0] [-0.02:0.02:0.04] [-0.04:0.02:0.04] 1	[0.02:0.02:0] [0.02:0.02:0. 02] [- 0.12:0.02:0.0 4] UI	[min:step:max] [min:step:max]
	c(-3) c(-4) c(1) <u>N b</u> b_max(1)	[-0.04:0.02:0] [-0.02:0.02:0.04] [-0.04:0.02:0.04] 1 1	[0.02:0.02:0] [- 0.12:0.02:0.0 4] UI	[min:step:max] [min:step:max] As/dffe1
	c(-3) c(-4) c(1) <u>N b</u> <u>b max(1)</u> b max(2N-b)	[-0.04:0.02:0] [-0.02:0.02:0.04] [-0.04:0.02:0.04] 1 1 [0.3 0.2*ones(1.22)]	[0.02:0.02:0] [0.02:0.02:0. 02] [- 0.12:0.02:0.0 4] UI	[min:step:max] [min:step:max] As/dffe1 As/dffe2N b
	c(-3) c(-4) c(1) b max(1) b max(2N-b) b min(1)	[-0.04:0.02:0] [-0.02:0.02:0.04] [-0.04:0.02:0.04] 1 1 [0.3 0.2*ones[1,22]] 0	[-0.04.0.02:0] [0.02:0.02:0. 0.12:0.02:0.0 4] UI	[min:step:max] [min:step:max] As/dffe1 As/dffe2N b As/dffe1
	c(-3) c(-4) c(1) b max(1) b max(2N-b) b min(1) b min(2N-b)	[-0.04:0.02:0] [-0.02:0.02:0.04] [-0.04:0.02:0.04] 1 1 [0.3 0.2*ones(1,22)] 0 [0 2 0 0*cones(1,22)]	[0.02:0.02:0. 02] [- 0.12:0.02:0.0 4] UI	[min:step:max] [min:step:max] As/dffe1 As/dffe2N b As/dffe1 As/dffe1
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	c(-3) c(-4) c(1) b_max(1) b_max(2N-b) b_min(1) b_min(2N-b) g_DC	[-0.04:0.02:0] [-0.02:0.02:0.04] [-0.04:0.02:0.04] 1 1 [0.3 0.2*ones(1,22)] 0 [-0.2*ones(1,22)] [-10:1:0]	(0.02:0.02:0) [0.02:0.02:0) 0.02:0.02:0.0 4] UI dB	[min:step:max] [min:step:max] As/dffe1 As/dffe2N b As/dffe2N b [min:step:max]
	c(-3) c(-4) c(1) <u>b max(1)</u> <u>b max(2N-b)</u> <u>b min(1)</u> <u>b min(2N-b)</u> <u>g_DC</u> <u>f_z</u>	[-0.04:0.02:0] [-0.02:0.02:0.04] [-0.04:0.02:0.04] 1 1 [0.3 0.2*ones(1,22)] 0 [-0.2 - 0.2*ones(1,22)] [-10:1:0] 42.5	(0.02:0.02:0. 02] [- 0.12:0.02:0.0 4] UI UI GHz	[min:step:max] [min:step:max] As/dffe1 As/dffe2N b As/dffe2N b [min:step:max]
	c(-3) c(-4) c(1) <u>b max(1)</u> <u>b max(2N-b)</u> <u>b min(1)</u> <u>b min(2N-b)</u> <u>g_DC</u> <u>f_z</u> <u>f_p1</u>	[-0.04:0.02:0] [-0.02:0.02:0.04] 1 [-0.04:0.02:0.04] 1 [0.3 0.2*ones(1,22)] 0 [-0.2 - 0.2*ones(1,22)] [-10:1:0] 42.5 42.5	(0.02:0.02:0. 02] [- 0.12:0.02:0.0 4] UI UI dB GHz GHz	[min:step:max] [min:step:max] As/dffe1 As/dffe2N b As/dffe2N b [min:step:max]
	c(-3) c(-4) c(1) b max(1) b max(1) b min(1) b min(2N-b) g_DC f_z f_p1 f_p2	[-0.04:0.02:0] [-0.02:0.02:0.04] 1 [-0.04:0.02:0.04] 1 [0.3 0.2*ones(1,22)] 0 [-0.2 - 0.2*ones(1,22)] [-10:1:0] 42.5 42.5 106.25	(0.02:0.02:0, 02] [- 0.12:0.02:0.0 4] UI dB GHz GHz GHz	[min:step:max] [min:step:max] As/dffe1 As/dffe2N b As/dffe2N b [min:step:max]
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	c(-3) c(-4) c(1) b max(1) b max(1) b min(1) b min(2N-b) g_DC f_z f_p1 f_p2 g_DC HP f_HP_P2 Butterworth Raised_Cosine	[-0.04:0.02:0] [-0.02:0.02:0.04] [-0.04:0.02:0.04] 1 1 [0.3 0.2*ones(1,22)] 0 [-0.2 - 0.2*ones(1,22)] [-10:1:0] 42.5 42.5 106.25 [-4:1:0] 1.328125 1 0 0	(0.02.00.22.0) (0.02:0.02:0.0 (0.2:0.02:0.0 (0.2:0.02:0.0 (0.2:0.02:0.0 (0.2:0.02:0.0 (0.2:0.02:0.0 (0.2:0.02:0.0 (0.2:0.02:0.0 (0.2:0.02:0.0 (0.2:0.02:0.0) (0.2:0.00:0) ([min:step:max] [min:step:max] As/dffe1 As/dffe1 As/dffe2N b [min:step:max] [min:step:max] include infr include infr
	c(-3) c(-3) c(-1) c(1) b max(1) b max(2N-b) b_min(1) b min(2N-b) g_DC f_z f_p1 f_p2 g_DC HP f_HP_P2 Butterworth Raised_Cosine RC Cosine	[-0.04:0.02:0] [-0.02:0.02:0.04] [-0.04:0.02:0.04] 1 1 [0.3 0.2*ones(1,22)] 0 [-0.2- 0.2*ones(1,22)] [-10:1:0] 42.5 42.5 106.25 [-4:1:0] 1.328125 1 0 6.70E+10	(0.02.00.22.0) (0.02.00.20.0) (0.02.00.20.0) (0.02.00.20.0) (0.02.00.20.0) (0.02.00.20.0) (0.02.00.20.0) (0.02.00.20.0) (0.02.00.20.0) (0.02.00.20.0) (0.02.00.20.0) (0.02.00.20.0) (0.02.00.20.0) (0.02.00.20.0) (0.02.00.20.0) (0.02.00.20.0) (0.02.00.20.0) (0.02.00.20.0) (0.02.00.20.0) (0.02.	[min:step:max] [min:step:max] As/dffe1 As/dffe2N b As/dffe2N b [min:step:max] [min:step:max] include infr include in fr start freq for Rco
	c(-3) c(-3) c(-3) c(1) N b b max(1) b max(2N-b) b_min(1) b min(2N-b) g_DC f_z f_p1 f_p2 g_DC HP f_HP_p2 Butterworth Raised_Cosine RC_end	[-0.04:0.02:0] [-0.02:0.02:0.04] 1 1 [-0.04:0.02:0.04] 1 1 [0.3 0.2*ones(1,22)] 0 [-0.2*ones(1,22)] [-10:1:0] 42.5 42.5 106.25 [-4:1:0] 1.328125 1 0 0 6.70E+10 7.97E+10	(0.02.0.02.0) (0.02:0.02.0) (0.02:0.02.0) (0.2:0.02:0.02:0.0 (0.2:0.02:0.02:0.0 (0.2:0.02:0.02:0.02:0 (0.2:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0.02:0.02:0.02:0 (0.02:0.02:0.02:0.02:0.02:0.02:0.02:0.02	[min:step:max] [min:step:max] As/dffe1 As/dffe2N b As/dffe2N b [min:step:max] [min:step:max] include in fr include in fr start freq for RCo end freq for RCo
	c(-3) c(-3) c(-4) c(1) <u>b</u> max(1) <u>b</u> max(1) <u>b</u> max(1) <u>b</u> min(1) <u>b</u> min(2N-b) <u>g</u> _DC <u>f_z</u> <u>f_p1</u> <u>f_p2</u> <u>g</u> _DC HP <u>f_HP_PZ</u> <u>Butterworth</u> <u>Raised Cosine</u> <u>RC Start</u> <u>RC start</u> <u>RC cend</u>	[-0.04:0.02:0] [-0.02:0.02:0.04] 1 1 [0.3 0.2*ones(1,22)] 0 [-0.2 + 0.2*ones(1,22)] [-10:1:0] 42.5 42.5 106.25 [-4:1:0] 1.328125 1 0 6.70E+10 7.97E+10 4	(0.02.00.20) (0.02:0.02:0) (0.02:0.02:0) (0.2:0.02:0.0 4] UI UI UI dB GHz GHz GHz GHz Iogical Hz Hz Hz III	[min:step:max] [min:step:max] As/dffe1 As/dffe2N b As/dffe2N b [min:step:max] [min:step:max] include infr include infr include infr end freq for RCos
	c(-3) c(-4) c(1) N b max(1) b max(1) b max(2N-b) b min(1) b min(2N-b) g_DC f_z f_p1 f_p2 g_DC HP f_HP_PZ Butterworth Raised Cosine RC Start RC_end ffe_pre_tap_len	[-0.04:0.02:0] [-0.02:0.02:0.04] 1 1 [-0.04:0.02:0.04] 1 1 [0.3 0.2*ones(1,22)] 0 [-0.2-0.2*ones(1,22)] [-10:1:0] 42.5 42.5 106.25 [-4:1:0] 1.328125 1 0 6.70E+10 7.97E+10 4 4 6 6 7 9 4 6 7 9 7 1 1 1 1 1 1 1 1 1 1 1 1 1	(0.02.00.22.0) (0.02:0.02:0.0 0.22 (- 0.12:0.02:0.02 (- 0.12:0.02:0.0 (- 0.2:0.02:0.0 (- 0.2:0.02:0.0 (- 0.2:0.02:0.0 (- 0.2:0.02:0.0 (- 0.2:0.02:0.0 (- 0.2:0.02:0.0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0 (- 0.2:0.02:0.02:0.02:0 (- 0.2:0.02:0.02:0.02:0 (- 0.2:0.02:0.02:0.02:0.02:0 (- 0.2:0.02:0.02:0.02:0.02:0.02:0.02:0 (- 0.2:0.02:0.02:0.02:0.02:0.02:0.02:0.02:	[min:step:max] [min:step:max] As/dffe1 As/dffe2N b As/dffe1 As/dffe2N b [min:step:max] [min:step:max] include in fr include in fr start freq for RCo end freq for RCos
	c(-3) c(-3) c(-3) c(1) N b b max(1) b max(1) b max(1) b min(2N-b) g_DC f_z f_p1 f_p2 g_DC HP f_HP_PZ Butterworth Raised Cosine RC Start RC end ffe_pre tap_len ffe_post tap_len	[-0.04:0.02:0] [-0.02:0.02:0.04] 1 1 [-0.04:0.02:0.04] 1 1 [0.3 0.2*ones(1,22)] 0 0 [-0.2*ones(1,22)] [-10:1:0] 42.5 42.5 106.25 [-4:1:0] 1.328125 1 0 6.70E+10 7.97E+10 4 8	(0.02:0.02:0) (0.02:0.02:0) (0.02:0.02:0) (0.2:0.02:0.0 4] UI UI UI dB GHz GHz GHz GHz Iogical Hz Logical Hz UI UI UI UI UI	[min:step:max] [min:step:max] As/dffe1 As/dffe2N b As/dffe2N b [min:step:max] [min:step:max] include in fr include in fr include in fr clare for RCo end freq for RCo
	C(-3) C(-3) C(-4) C(1) b max(1) b max(1) b max(2N-b) b min(1) b min(2N-b) g_DC f_z f_p1 f_p2 g_DC HP f_HP_PZ Butterworth Raised Cosine RC Start RC_end ffe_post tap len ffe_tap step size	[-0.04:0.02:0] [-0.02:0.02:0.04] [-0.04:0.02:0.04] 1 1 [0.3 0.2*ones(1,22)] 0 [-0.2 - 0.2*ones(1,22)] [-10:1:0] 42.5 106.25 [-4:1:0] 1.328125 1 0 6.70E+10 7.37E+10 4 8 0 0	(0.02:0.02:0) (0.02:0.02:0) (0.02:0.02:0.02:0) (0.02:0.02:0.02:0.0 (0.02:0.02:0.02:0) (0.02	[min:step:max] [min:step:max] As/dffe1 As/dffe2N b As/dffe1 As/dffe2N b [min:step:max] [min:step:max] [min:step:max] include in fr include in fr start freq for RCos
	c(-3) c(-3) c(-1) c(1) <u>N b</u> <u>b max(1)</u> <u>b max(1)</u> <u>b max(1)</u> <u>b max(1)</u> <u>b min(2N-b)</u> <u>g_DC</u> <u>f_z</u> <u>f_p1</u> <u>f_p2</u> <u>g_DC HP</u> <u>f_HP PZ</u> <u>Butterworth</u> <u>Raised Cosine</u> <u>RC Start</u> <u>RC Start</u> <u>RC Start</u> <u>RC start</u> <u>RC start</u> <u>RC start len</u> <u>ffe post tap len</u> <u>ffe main cursor min</u>	[-0.04:0.02:0] [-0.02:0.02:0.04] 1 1 [-0.04:0.02:0.04] 1 1 [0.3 0.2*ones(1,22)] 0 [-0.2*ones(1,22)] [-10:1:0] 42.5 42.5 106.25 [-4:1:0] 1.328125 1 0 6.70E+10 7.97E+10 4 8 0 0 0	(0.02:0.02:0) (0.02:0.02:0) (0.02:0.02:0) (0.2:0.02:0.0 4] UI UI UI dB GHz GHz GHz GHz Iogical Hz UI UI UI UI UI UI UI	[min:step:max] [min:step:max] As/dffe1 As/dffe2N b As/dffe2N b [min:step:max] [min:step:max] include in fr include in fr include in fr catt freq for RCos
	C(-3) C([-0.04:0.02:0] [-0.02:0.02:0.04] [-0.04:0.02:0.04] 1 1 [0.3 0.2*ones(1,22)] 0 [-0.2 - 0.2*ones(1,22)] [-10:1:0] 42.5 106.25 [-4:1:0] 1.328125 1 0 6.70E+10 7.37E+10 4 8 0 0 0 0 0 0 0 0 0 0 0 0 0	(0.02:0.02:0) (0.02:0.02:0) (0.02:0.02:0.02:0) (0.02:0.02:0.02:0.0 (0.02:0.02:0.02:0) (0.02	[min:step:max] [min:step:max] As/dffe1 As/dffe2N b As/dffe1 As/dffe2N b [min:step:max] [min:step:max] [min:step:max] include in fr include in fr start freq for RCos
	c(-3) c(-3) c(-1) c(1) N b b max(1) b max(1) b max(1) b max(1) b min(2N-b) g_DC f_z f_p1 f_p2 g_DC HP f_HP_P2 Butterworth Raised Cosine RC Cant RC_end ffe_pre_tap_len ffe_past tap_len ffe_pre_tap_len ffe_main cursor min ffe_pre_tap_len maxet ffe_main cursor min ffe_pre_tap_tap_max	[-0.04:0.02:0] [-0.02:0.02:0.04] [-0.04:0.02:0.04] 1 1 [0.3 0.2*ones(1,22)] 0 [-0.2*o.02*ones(1,22)] [-10:1:0] 42.5 42.5 106.25 [-4:1:0] 1.328125 1 1 0 6.70E*10 7.97E*10 4 8 0 0 0 0 7 9 7 9 7 9 1 1 0 0 0 0 0 0 0 0 0 0 0 0 0	(0.02.00.20) (0.02:0.02:0) (0.02:0.02:0) (0.02:0.02:0) (0.02:0.02:0) (0.02:0.02:0) (0.02:0.02:0) (0.02	[min:step:max] [min:step:max] As/dffe1 As/dffe2N b As/dffe2N b [min:step:max] [min:step:max] include in fr include in fr include in fr cath freq for RCos
	C(-3) C([-0.04:0.02:0] [-0.02:0.02:0.04] [-0.04:0.02:0.04] 1 1 1 [0.3 0.2*ones(1,22)] 0 (-0.2 - 0.2*ones(1,22)] [-10:1:0] 42.5 42.5 106.25 [-4:1:0] 1.328125 1 0 6.70E+10 7.97E+10 4 8 0 0 0 0 0 0 0 0 0 0 0 0 0	(0.02:0.02:0) (0.02:0.02:0) (0.02:0.02:0.0 (0.2:0.02:0.0 (0.2:0.02:0.0 (0.2:0.02:0.0 (0.2:0.02:0) (0.2:0.02	[min:step:max] [min:step:max] As/dffe1 As/dffe1 As/dffe2N b As/dffe1 As/dffe2N b [min:step:max] [min:step:max] include in fr include in fr include in fr cond freq for RCos
	c(-3) c(-3) c(-3) c(1) N b b max(1) b max(1) b max(1) b max(1) b min(2N-b) g_DC f_z f_p1 f_p2 g_DC HP f_HP_P2 Butterworth Raised Cosine RC Cart RC_end ffe_pre_tap_len ffe_pre_tap_len ffe_pre_tap_len ffe_pre_tap_len ffe_pre_tap_len ffe_pre_tap_len ffe_pre_tap_len ffe_pre_tap_len ffe_pre_tap_len ffe_pre_tap_max	[-0.04:0.02:0] [-0.04:0.02:0.04] 1 1 [-0.04:0.02:0.04] 1 1 [0.3 0.2*ones(1,22)] 0 [-0.2*0.02*ones(1,22)] [-10:1:0] 42.5 42.5 106.25 [-4:1:0] 1.328125 1 0 6.70E*10 7.97E*10 4 8 0 0 0 0 0 0 0 0 0 0 0 0 0	Clock (0.22) (0.02:0.02:0) (0.02:0.02:0) (0.02:0.02:0) (0.02:0.02:0) (0.02:0.02:0) (0.02:0	[min:step:max] [min:step:max] [min:step:max] As/dffe1 As/dffe2N b As/dffe1 As/dffe2N b [min:step:max] [min:step:max] include in fr inclu

I/O control		
DIAGNOSTICS	1	logical
DISPLAY WINDOW	1	logical
CSV REPORT	1	logical
RESULT DIR	\results\C2M B {date}\	logical
SAVE_FIGURES	0	logical
_ Dort Order	[1224]	
RUNTAG	C2M B	
	0	logical
Operational		
ERL Pass threshold	9.7	dB
COM Pass threshold	3	db
VEC Pass threshold	10.69073041	db
DER_0	2.67E-05	
Tr	4.00E-03	ns
FORCE TR	1	logical
PMD type	C2Mcom	
FW	1	
TDR and ERL ontions		logical
Tok and Eke options		logical
700		logical
TDK	1	In pinel
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	2000	logical
TDR_Butterworth	1	
beta x	0	
rho x	0.618	
TDR W TXPKG	0	UI
N_bx	0	
fixture delay time	[00]	
Tukey Window	1	
Noise, jitter		UI
sigma RJ	0.01	UI
A DD	0.02	V^2/GHz
eta 0	6.00F-09	dB
SNR_TX	33	0.5
R_LM	0.95	
11-2022 BenArtsinkø	oif2022.065.02	-
highlighted are under re-	consideration	_
MLSE	1	

0

AC_CM_RMS

Table 93A–3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0008455 0.000340225]	
package_tl_tau	0.00644805	ns/mm
package_Z_c	[92 92 ; 70 70; 80 80; 100 100]	Ohm

Parameter	Setting	
board_tl_gamma0_a1_a2	[0 6.44084e-4 3.6036e-05]	1.5 db/in@56G
board_tl_tau	5.790E-03	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	125	mm
z_bp (NEXT)	0	mm
z_bp (FEXT)	125	mm
z_bp (RX)	0	mm
C_0	[0.2e-40]	nF
C_1	[0.2e-40]	nF
Include PCB	0	logical

Seletions (rectangle, gaussian,dual_rayleigh,trian gle		
Histogram_Window_Weight	gaussian	selection
Qr	0.02	UI

ICN parameters		
fv	0.594	Fb
f_f	0.594	Fb
f_n	0.594	Fb
f_2	79.688	GHz
A_ft	0.450	v
A nt	0.450	v

Floating Tap Control		
N_bg	8	0 1 2 or 3 groups
N bf	4	taps per group
N É	80	UI span for floating
N_1	80	taps
hmaya	0.2	max DFE value for
DIIIaxg	0.2	floating taps
B_float_RSS_MAX	0.1	rss tail tap limit
N tail start	61	(UI) start of tail taps
N_tan_start	61	limit

Receivertesting		
RX CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

802.3.dj Interim meet

Sample adjustment	[0 0]	phase	
ts anchor	0		

COM Configuration file with Package A

Fable 93A-1 parameters			
Parameter	Setting	Units	Information
fh	106.35	GRd	linoindeion
1_U	100.25	GBU	
t_min	0.05	GHZ	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
1.0	[0 12 0 15 0 14: 0 12 0 15 0 14]	nH	[TV DV]
<u>_</u>	[0.15 0.15 0.14, 0.15 0.15 0.14]	110	
C_D	[0.3e-4 0.3e-4]	n⊦	[IX KX]
z_p select	[1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18]		[test cases to rur
z_p (TX)	[8 15 24 30 40 45 8 15 24 30 40 45 8 15 24 30 40 45;1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[44444488888812121212121212; 000000000000000000000000	mm	[test cases]
z_p (FEXT)	[8 15 24 30 40 45 8 15 24 30 40 45 8 15 24 30 40 45;1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8	mm	[test cases]
z_p (RX)	[4 4 4 4 4 4 8 8 8 8 8 8 12 12 12 12 12 12 12; 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	mm	[test cases]
PKG_Tx_FFE_preset	0		
Ср	[0.5e-4 0.5e-4]	nF	[TX RX]
RO	50	Ohm	
 P.d	[50 50]	Ohm	[TV PV]
<u>n_u</u>	[30 30]		
A_V	0.45	V	vp/vt=
A_fe	0.45	V	vp/vf=
A_ne	0.45	v	
1	4		
M	32		
Alter and Fra	52		
Tilter and Eq			
t_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.4:0.02:-0.3]	[-0.4:0.02:0]	[min:step:max]
c(-2)	[0:0.02:0.04]	[0:0.02:0.2]	[min:step:max]
c(-3)	[-0.04:0.02:0]	[-0.04:0.02:0]	[min:step:max]
c(-4)	[-0.02:0.02:0.04]	[0.02:0.02:0. 02]	[min:step:max]
c(1)	[-0.04:0.02:0.04]	[- 0.12:0.02:0.0 4]	[min:step:max]
N_b	1	UI	
b max(1)	1		As/dffe1
b max(2N-b)	[0.3.0.2*ones(1.22)]		As/dffe2N b
h min(1)	0		Δs/dffe1
h min(2 M-b)	[-0.2-0.2*ones(1.22)]		As/dffo2 N b
g DC	[-0.2 - 0.2 - 01es(1,22)]	dB	[min:step:max
fz	42.5	GHz	
-	40.5	C11-	
f_p1	42.5	GHZ GH7	
g DC HP	[-6:1:0]	5/12	[min:step:max
f HP P7	1.328125	GHz	
Butterworth	1	logical	include in fr
Baicod Cosine	0	logical	include in fr
Kaiseu_Cosine	0	logical	include in fr
RC_end	6.70E+10 7.97E+10	HZ HZ	end freq for RCo
ffe_pre_tap_len	4	UI	
ffe_post_tap_len	8	UI	
ffe tap step size	0		
ffe main cursor min	0		
ffe pre tan1 may	0.7		
ffo_poct_tap1_max	0.7		
ne_post_tap1_max	0.7		
ffe_tapn_max	0.7		
ffe backoff	0		1

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\C2M_A_{date}\	
SAVE FIGURES	0	logical
Port Order	[1324]	
BUNTAG	C2M A	-
NONTAG	C2III_A	-
	0	logical
Operational		
ERL Pass threshold	9.7	dB
COM Pass threshold	3	db
VEC Pass threshold	10.69073041	db
DER_0	2.67E-05	
T_r	4.00E-03	ns
FORCE_TR	1	logical
PMD type	C2Mcom	
EW	1	
TDR and ERL options		logical
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	2000	logical
TDR_Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	0	
fixture delay time	[00]	
Tukey Window	1	
Noise, iitter	-	UI
sigma RJ	0.01	UI
A DD	0.02	V^2/GHz
	6.005.00	dB
eta 0 I	0.UUE-U9	
eta_0 SNR_TX	33	
eta_0SNR_TXR_LM	33 0.95	
eta_0 SNR_TX R_LM	33 0.95	

MLSE	1	
AC_CM_RMS	0	

Table 93A–3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[5e-48.9e-42e-4]	
package_tl_tau	0.006141	ns/mm
package Z c	[87.5 87.5;92.5 92.5]	Ohm

Parameter	Setting	
board_tl_gamma0_a1_a2	[0 6.44084e-4 3.6036e-05]	1.5 db/in @ 56G
board_tl_tau	5.790E-03	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	125	mm
z_bp (NEXT)	0	mm
z_bp (FEXT)	125	mm
z_bp (RX)	0	mm
C_0	[0.2e-40]	nF
C_1	[0.2e-40]	nF
Include PCB	0	logical

Seletions (rectangle, gaussian,dual_rayleigh,triang le		
Histogram_Window_Weight	gaussian	selection
Qr	0.02	UI

ICN parameters		
f_v	0.594	Fb
f_f	0.594	Fb
f_n	0.594	Fb
f_2	79.688	GHz
A_ft	0.450	v
A_nt	0.450	V

Floating Tap Control		
N_bg	8	0 1 2 or 3 groups
N_bf	4	taps per group
N É	90	UI span for floatin
1_1	80	taps
hmaya	0.3	max DFE value for
Dillaxg	0.2	floating taps
B_float_RSS_MAX	0.1	rss tail tap limit
N toil start	61	(UI) start of tail tap
ni_tall_start		limit

Receivertesting		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

802.3.dj Interim me

Sample adjustment	[0 0]	phase	
ts_anchor	0		