FECi interoperability test vectors

Omri Levy, Matt Brown (Alphawave Semi)

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Supporters (of this presentation)

- Vasu Parthasarathy, Broadcom
- Lenin Patra, Marvell
- Xiang He, Huawei
- Zvi Rechtman, Nvidia

Supporters (of the accompanying test vectors)

- Vasu Parthasarathy, Broadcom
- Xiang He, Huawei
- Lenin Patra, Marvell

Link to the accompanying test vectors:

https://www.ieee802.org/3/dj/public/24_01/levy_3dj_02a_2401.7z

This presentation

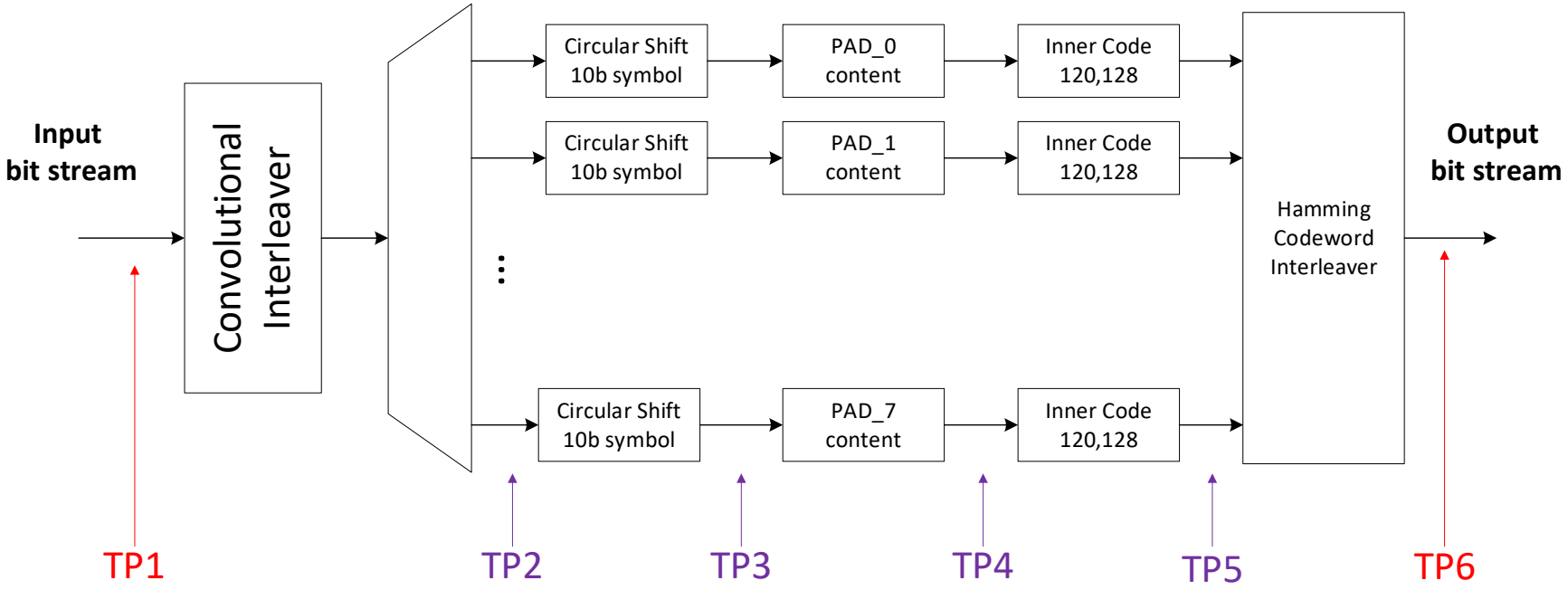
- Provides FECi sublayer (CL177) interoperability test vectors

Background

- The inner FEC in patra_3dj_01b_2303 with FEC lane rate, convolutional interleaver details in he_3dj_01_2307 was adopted in the P802.3dj March 2023 and July 2023 Plenary meetings, respectively.
- 4x RS codewords interleaving for 200GbE and 400 GbE using 200G/lane AUIs or PMDs he_3dj_02a_2307 was adopted July 2023 Interim, Motion #10
- Inner FEC Pad insertion changes of pad block from 384 bits to 1024 bits (8 Inner FEC CWs) and insertion period from 3264 CWs to 8704 CWs, including 8:1 Hamming interleaver protection for pad bits and FS content, as shown in rechtman_3dj_01a_2309 was adopted September 2023 Interim, Motion #4

Interoperability test vectors and test points

- The FECi baseline includes opportunities for ambiguity and misunderstanding.
- The interoperability test vectors are used during design development to check for interoperability.
- Test vectors are given as a plain-text file for the following test points (TP1-TP6)
  - TP1 and TP6 are required for interoperability.
  - TP2-TP5 are given as a reference for debug

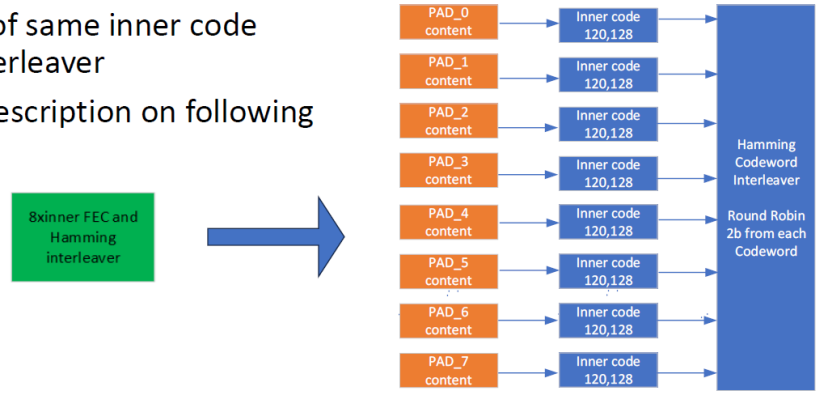


FECi Padding insertion process and FS

- Padding insertion process, pad structure and 48 FS bits are given as defined in rechtman_3dj_01a_2309
- 912 Padding bits were randomized and given as a reference in the padding text-file.

What the pad insertion process contains

- This diagram represent the padding insertion unit (green unit from previous slide):
- Allows the reuse of same inner code and Hamming interleaver
- PAD_i structure description on following slides



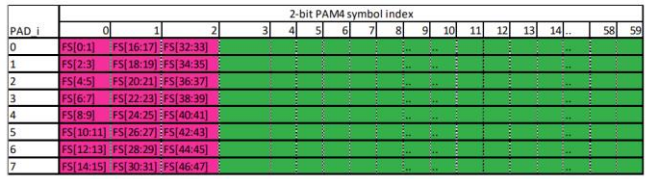
Source: rechtman_3dj_01a_2309 slide 7

Pad structure (prior to encoding function)

- Pad is 960 bits (prior to 128,120 encoder)
  - 48 bits for the Frame Sequence (FS)
  - 912 bits as padding bits (e.g. backchannel)
- 120-bit PAD_i bits per encoder (i.e. exactly inner-FEC CW)

In figure to right:

- 2-bit symbols (Hamming interleaver is 2 bits).
- Symbols 0-2 on each PAD_i are defined Frame Sequence (FS)
- Symbols 3-59 on each PAD_i contain the rest of the padding bits that can be used for backchanneling



FS[0:47]=01011001 01010010 01100100 10100110 10101101 10011011

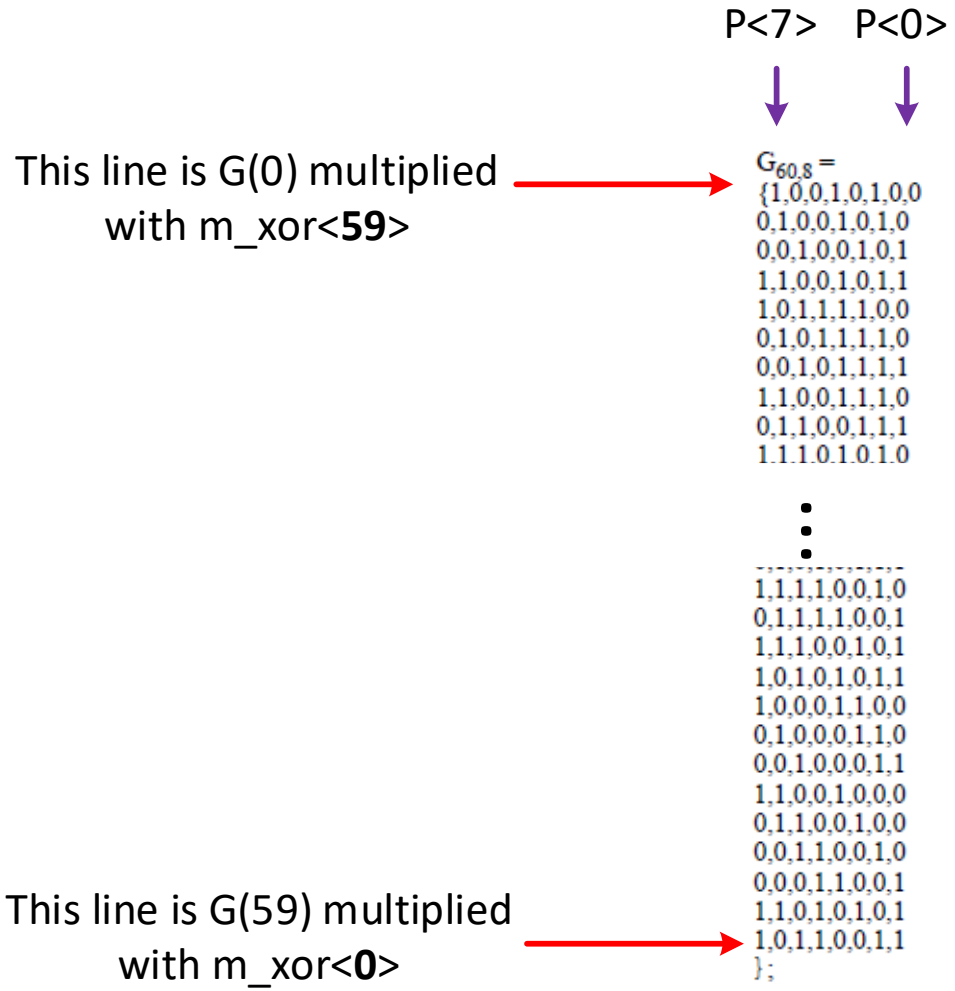
FS (48 bits)
PAD bits (912 bits)

- PAD_0[0:5]= 01 01 10
- PAD_1[0:5]= 01 10 10
- PAD_2[0:5]= 10 01 11
- PAD_3[0:5]= 01 00 01
- PAD_4[0:5]= 01 10 10
- PAD_5[0:5]= 01 10 01
- PAD_6[0:5]= 00 01 10
- PAD_7[0:5]= 10 10 11

Source: rechtman_3dj_01a_2309 slide 10

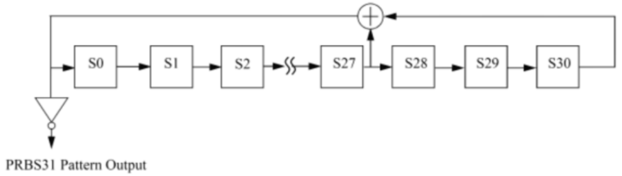
Hamming FEC encoder semantics

- Definitions:
  - m<119:0> would be the message word to encode.
  - For k = 0:59, m_xor<k> = m<2k> + m<2k+1>
  - p<7:0> = m_xor<59:0> • $G_{(60,8)}$ would be the parity bits.
  - c<127:8> = m<119:0> , c<7:0> = p<7:0> would be the codeword bits.
  - MSB is transmitted first.
- m_xor is multiplied with G per index as follows:
  - First bit to transmit is multiplied with the first row in the matrix.
  - G(0) with m_xor<59>,…, G(59) with m_xor<0>.
- Parity bits (P) has MSB to LSB from left to right



Test vectors format

- Transmission order inside a line is from left to right.
- TP1:
  - Serial bit stream Based on PRBS31 with Polynomial x31 + x28 + 1 and start Seed - 0x7fffffff
  - Each line has 120 bits.



first → (start of line 1); last → (end of line 4)

```
111111111111111111111111111100011111111111111111111111110000001111111111111111111111000111000111111111111111111100000000
000011111111111111110001111111110001111111111111000000111111000000111111111100011100011100011100011111110000000000000000
000000001111000111111111111111111111000100000011111111111111111100001101110001111111111111110001001110000000111111111111
000011100000111100011111111100010000001100010000001111110000110111001000110111000111000100111000111000111000000000001110
```

- TP2-TP4:
  - Each line has 120 bits that feed each of the 8 FECi flows
  - Xs at the beginning of the file means undetermined value due to CI's delays.

Flow	Line
Flow 0	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111000111000111111111111111111100000000
Flow 1	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1100011100011100011111110000000000000000
	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111111111110001001110000000111111111111
⋮	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0111000100111000111000111000000000001110
	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000000000001111111100011100100111111111
	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1100000000001110110010010001110001111111
	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000110100110110000011110001000100110110
Flow 7	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0011100100100011100011100011100000011111
Flow 0	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx1111111111100011111111110000001111111110
	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx0000001111111110110000111111000111000111

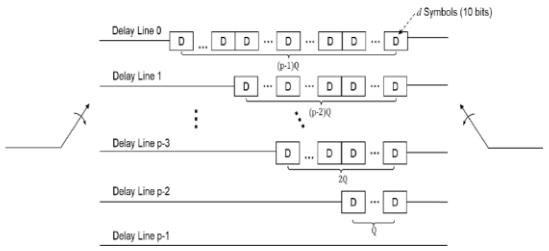
- TP5:
  - Same as TP2-TP4 only with 128 bits per line after encoding.
- TP6:
  - Single output serial bits stream after line interleaver.
  - 128b per line.
  - Xs at the beginning of the file means undetermined value due to CI's delays.

Test vectors folder content

- Plain text files for reference
  - Hamming (128,120) generator matrix
  - Padding content text file – 960 pad bits.
- TP1 serial input bit stream
- Vectors cover 3 frames:
  - 8704x3 CWs before padding. (TP1, TP2. TP3)
  - 8712x3 CWs including padding. (TP4, TP5. TP6)
  - Parity bits are added by the Hamming encoders
- Separate set of vectors is given per CI delay, considering D=4 as defined in [he_3dj_01_2307]

200G/lane Common Convolutional Interleaver Design for 200G/400G/800G/1.6TbE

- An universal 200G/lane convolutional interleaver is proposed for different MACs to unify the processing
  - If 4x RS CWs interleaving in the PMA proposal is adopted, the convolutional interleaver logics will be further shared among all the MACs .
- For latency sensitive applications, convolutional interleaver can be bypassed.



Rate	d (RS symbol)	P	Q	Depth	Latency ns	FEC_I Lane Rate
1.6TE	4	3	24	12x RS	27.1	200G/lane
800GE	4	3	48	12x RS	54.2	
400GE	4*	3	96	12x RS	108.4	
200GE	4*	3	192	12x RS	216.8	
400GE	2	6	48	12x RS	135.5	
200GE	2	6	96	12x RS	271.1	

*If 4x RS interleaving for 200GE/400GE is adopted.

Source: [he_3dj_01_2307] slide 10

Summary

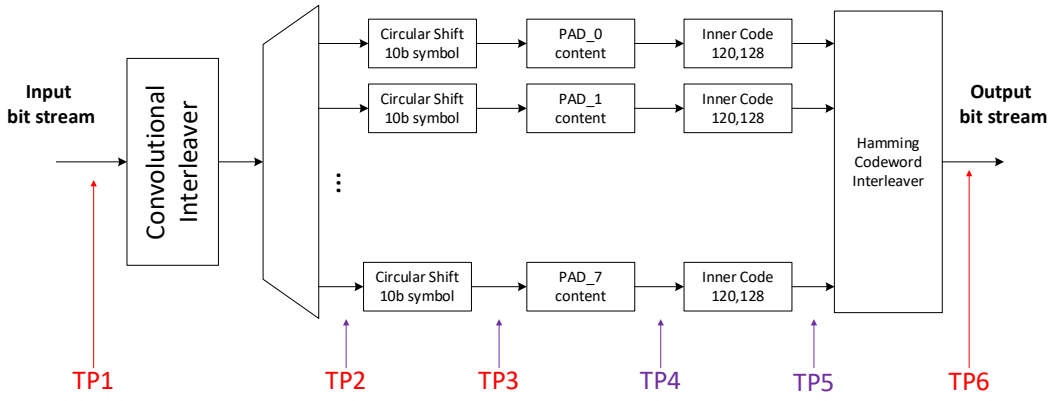
- FECi sublayer (CL177) interoperability vectors were proposed

Backup

Padding insertion schemes and test vectors

- Two padding equivalent insertion schemes are shown below
- Two schemes are interop with each other. i.e TP1, TP2,TP3 and TP6 are the same.
- Debug points TP4-TP5 would be different.
- Vectors proposal of this presentation refers to scheme A

Padding insertion scheme A



Padding insertion scheme B