# IEEE P802.3dj Electrical
# Ad Hoc Report

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## Electrical Track Ad Hoc Chair

# Report

- 3 ad hoc calls since November 2023 meeting
  - 7 Dec 2023, 4 Jan 2024, 11 Jan 2024
  - 75+ attendees
  - 14 contributions
    - 1 additional channel contributions
- Next meeting series:
  - Announced over the electrical track email reflector
  - 8 Feb and 29 Feb 2024

# Presentations

- Meeting minutes and presentation materials:
https://www.ieee802.org/3/dj/public/adhoc/electrical/index.html


- 7 December
  - "212Gb/s Per Lane PAM4 CR Channels with Flexible Host Architectures and Longer Reach Cables - Switch Perspective" – Jim Weaver
  - "Priority of Next Steps for IEEE P802.3dj Electrical Track - 7 December Update" – Kent Lusted
  - "Baseline proposals for electrical interfaces at 200 Gb/s per lane" – Adee Ran
  - "Skew … The Rest of the Story.  SCMR (signal to common mode ratio) for Channel" – Rich Mellitz

# Presentations (Cont'd)

- 4 Jan 2024
  - "Demonstrated implementation feasibility of suggested 224G C2M test fixture loss with measurement data", Steve Sekel
  - "Workshop report out on 212.5Gbps TP2 and TP1a Phy layer measurement capabilities", John Calvin
  - "A Study on 200G/Lane electrical interface parameters", Phil Sun
  - "Baseline Proposal for In-band training functions for 200 Gb/s per lane Electrical Interfaces", Adee Ran and Kent Lusted
  - "MLSE Proposal Update", Hossein Shakiba
- 11 Jan 2024
  - "C2M Channels for 200Gbps Update to contributed channels", Upen Reddy Kareti
  - "Towards baseline proposals for electrical interfaces at 200 Gb/s per lane - January 2024 update", Adee Ran
  - "Moving Forward on AUI C2M IL Target and Ref EQ", Kent Lusted
  - "Reference receiver framework for 200G/lane electrical interfaces and PHYs", Adam Healey
  - "An Executive Summary of the MLSE Proposal", Hossein Shakiba

# Straw Polls (4 Jan)

**Straw Poll #1:** I would support adopting link training based on IEEE Std. 802.3ck-2022, Cl 162.8.11 as the baseline for 200G/lane Backplane and Copper Cable PMDs

- Results (all): Y: 34, N: 1, A: 15

**Straw Poll #2:** I would support adopting in-band training based on the clause 136 training frame structure (Figure 136-3) for all AUI segments with electrical interfaces at 200 Gb/s per lane

- Results (all): Y: 36, N: 2, A: 15

# Straw Polls (11 Jan, 1 of 2)

**Straw Poll #1:** I would support adopting the 200G/lane electrical baseline proposals for CR in ran_3dj_elec_01_240111 slides 6-10

- Results (all):  Y: 50,  N: 0 ,  A: 11

**Straw Poll #2:** I would support adopting the 200G/lane electrical baseline proposals for KR in ran_3dj_elec_01_240111 slides 12-16 (with COM jitter as TBD on slide 16)

- Results (all): 50, Y: ,  N: 0,  A: 10

**Straw Poll #3:** I would support adopting the 200G/lane electrical baseline proposals for AUI C2C in ran_3dj_elec_01_240111 slides 18-22

- Results (all):  Y: 50 ,  N: 0,  A: 10

**Straw Poll #4:** I would support adopting the 200G/lane electrical baseline proposals for AUI C2M in ran_3dj_elec_01_240111 slides 24-29

- Results (all):  Y: 45,  N: 2,  A: 13

**Straw Poll #5:** For the 200G/lane AUI C2M electrical interfaces (using DER_0 = 2E-5), I would support adopting a recommended channel insertion loss ILdd (die-die) target of 32.5dB

- – Results (all):  Y: 32,  N: 9, A: 19
- – Results (802.3 voters):  Y: 24 ,  N: 11,  A: 9

# Straw Polls (11 Jan, 2 of 2)

**Straw Poll #6:** I would support including the MLSE effect in COM for 200G/lane CR:

- Results (all): Y: 33 N: 6 A: 10

**Straw Poll #7:** I would support including the MLSE effect in COM for 200G/lane KR:

- Results (all): Y: 33, N: 6, A: 10

**Straw Poll #8:** I would support including the MLSE effect in the reference RX for 200G/lane AUI C2M:

- Results (all): Y: 20, N: 16, A: 13

**Straw Poll #9:** I would support including the MLSE effect in COM for 200G/lane AUI C2C:

- Results (all): Y: 18, N:16, A: 14

**Straw Poll #10:** For the 200G/lane electrical interfaces having MLSE capability, the MLSE solution approach that I prefer is:

A. Include MLSE COM calculations based on shakiba_3dj_elec_01_240111, slide 5 with MLSE implementation penalty TBD)

B. Use MLSE coding gain as a rough estimate (i.e. shakiba_3dj_elec_01_240111, slide 6 middle graph and equation with MLSE implementation penalty TBD)

C. Relax COM margin by a fixed amount (exact amount is TBD)

(choose one) Results (all): A: 32 , B: 2 , C: 7

# Key Themes

- 200G/lane CR and C2M methodologies need more data as well as further exploration and consideration
- Electrical baselines for CR, KR, AUI C2M, AUI C2C
- Foundations to training for 200G/lane CR, KR, AUI C2M, AUI C2C
- Much discussion on MLSE capability in reference EQ and the use by interface type.

# THANKS!