Motions and Straw Polls

IEEE P802.3cw, IEEE P802.3df and P802.3dj Task Force Joint Meeting January 2024 Interim Kent Lusted, Intel John D'Ambrosia, Futurewei, U.S. Subsidiary of Huawei

Foreword

- Straw polls related to resolving comments may be found in the associated comment response files.
- This contribution summarizes motions and straw polls not related to comments.
- This contribution is not the official minutes of the meeting.

If there is any discrepancy between this contribution and the meeting minutes, then the minutes take precedence.

22 January 2024

I would support adopting the COM Die/Device model parameter values in lim_3dj_01_2401 slide 8 for 200G/Lane KR, CR, AUI chip-to-chip and chip-to-module

Results (all): Y: 49, N: 0, A: 23

I would support adopting the updated parameter values for Class B packages per benartsi_3dj_01_2401 slide 7

Results (all): Y: 44 , N: 1 , A: 39

I would support adopting the 200G/lane electrical baseline proposals summarized on ran_3dj_01a_2401 slide 29, with the addition that test fixtures for the CR PHYs are TBD.

Results (all): Y: 59, N: 0, A: 23

I would support adopting link training based on IEEE Std. 802.3ck-2022, Cl 162.8.11 as the baseline for 200G/lane Backplane and Copper Cable PMDs (with max_wait_timer = TBD) and in-band training based on the clause 136 training frame structure (Figure 136-3) for all PMAs with physically instantiated interfaces (AUIs) at 200 Gb/s per lane (within type 1/2 PHYs and extenders)

Results (all): Y: N: A:

I would support adopting the AN73 baseline proposal in lusted_3dj_04_2401, slides 6-14

Results (all) Y: 53 , N: 2 , A: 28

I would support the proposed reference receiver framework in healey_3dj_01_2401.pdf, slides 5-15

Results (all): Y: 65 , N: 0 , A: 21

For the 200G/lane electrical interfaces or PMDs having MLSE capability, the MLSE solution approach that I prefer is:

A. Include MLSE COM calculations based on equation U1.a in shakiba_3dj_01b_2401 slide 9

B. Include MLSE COM calculations based on equation U1.b in shakiba_3dj_01b_2401 slide 10

C. Include MLSE COM calculations based on equation U1.c in shakiba_3dj_01b_2401 slide 11

D. Need more information

E. None of the above

(choose one)

Results (all): A: 0 , B: 1 , C: 47 , D: 16 , E: 7

23 January 2024

I would support adopting a PMD control function based on 162.8.11 (IEEE Std. 802.3ck-2022) for 200G/lane Backplane and Copper Cable PMDs, with max_wait_timer = TBD

Results (all): Y: 64, N: 0, A: 22

I would support adopting in-band training for PMAs with physically instantiated chip-to-module interfaces (AUI-C2M) at 200 Gb/s per lane, based on 162.8.11 (IEEE Std. 802.3ck-2022) with training frame bit assignments and state diagrams TBD

Results (all): Y: 49 , N: 8 , A: 27

I would support adopting in-band training for PMAs with physically instantiated chip-to-chip interfaces (AUI-C2C) at 200 Gb/s per lane, based on 162.8.11 (IEEE Std. 802.3ck-2022) with training frame bit assignments and state diagrams TBD

Results (all): Y: 49, N: 2, A: 29

I would support the adoption of the 800GBASE-FR4-500 baseline as shown in welch_3dj_01a_2401 pages 10-16

Results (all): Y: 53 , N: 22 , A: 13

I would support removing the convolutional interleaver from the inner FEC sublayer for the following PHYs:

 200GBASE-FR1, 400GBASE-DR2-2, 800GBASE-DR4-2, 800GBASE-FR4, 1.6TBASE-DR8-2

Results (all): Y: 38 , N: 11 , NMI: 33 , A: 17

I support the adoption of a target SER limit of 9.6E-3 for TECQ/TDECQ/SECQ for the 2km FECi based PMDs

Results (all): Y: , N: , NMI: , A: