# P802.3dj Draft 0.2 Architectural considerations

Matt Brown, Alphawave, P802.3dj Editor-In-Chief Gary Nicholl, Cisco, Logic Track Lead Editor Adee Ran, Electrical Track Lead Editor Tom Issenhuth, Optical Track Lead Lead Editor

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### Introduction

- In Draft 0.2, the editorial team made some discussion-worthy decisions in favor of a concise and elegant standard.
- This presentation walks provides some visibility and rationalization for these decisions.

## **General Topics**

### **BER/FLR** specifications

- Definition of BER and FLR has become quite complex due to considerations of error correlation, inclusion of inner FEC, symbol vs bit multiplexing, combining AUI and PMD errors, etc.
- BER/FLR specification methodologies and targets are common for a set of similar PMD types.
- Created normative Annex 174A to provide big picture error consideration and error specifications for classes of PMDs.
  - PMD and AUI BER subclauses will point to one of the subclauses in Annex 174A
  - e.g., BER for IMDD PMDs using Clause 177 Inner FEC are specified in 174A.7 "Bit error ratio for 200 Gb/s per lane PMDs with 200GBASE-R Inner FEC"

### **BER/FLR specifications Example references**

178.2 Bit Error Ratio

Bit error ratio shall meet the requirements specified in 174A.6.

#### 178.3 Conventions

This clause describes four PMDs, 200GBASE-KR1, 400GBASE-KR2, 800GBASE-KR4, and 1.6TBASE-KR8, which have one, two, four, and eight lanes, respectively. For efficient description, the narameter n is used to describe the number of lanes in a specific PMD. Accordingly, n = 1 for

#### 180.1.1 Bit error ratio

Bit error ratio shall meet the requirements specified in 174A.6.

#### 180.2 Physical Medium Dependent (PMD) service interface

This subclause sp described in an a

a 182.1.1 Bit error ratio

Bit error ratio shall meet the requirements specified in 174A.7.

#### 182.2 Physical Medium Dependent (PMD) service interface

This subclause specifies the services provided by the PMD. The service interface for this PMD is described in an abstract manner and does not imply any particular implementation. The PMD service interface supports the exchange of encoded data between the PMD and the PMD client. The PMD translates the encoded data to and from signals suitable for the specified medium.

### **PMA/AUI** implementation examples

- In PMD and xMII Extender clauses we list the set of PMAs and AUI that are optional for the PHY or xMII Extender, but no further clarity is provided on when each element may or shall be used
  - We now have two PMD types (symbol-mux and bit-mux) which are to be used with the appropriate PMD or AUI.
  - We have a large number of PMDs.
- Annex 176B provides an exhaustive set of valid configurations for each PHY or xMII Extender.
- xMII Extender and PMD clauses may point to this annex to make sense of the AUI/PMA clauses listed in the PHY tables

### **PMA/AUI** implementation examples Annex 176B introduction

Annex 176B

(normative)

PMA instantiation options for 200 Gb/s, 400 Gb/s, 800 Gb/s, 1.6 Tb/s Physical Layer implementations

176B.1 Scope

This annex provides guidelines for implementing one or more 200GAUI-n, 400GAUI-n, 800GAUI-n, and 1.6TAUI-n within a PHY or xMII Extender.

#### 176B.2 Introduction

Each 200GBASE-R, 400GBASE-R, 800GBASE-R, and 1.6TBASE-R PHY is defined within the associated PMD clause to include PCS, PMA, and PMD sublayers. Some PHYs also include an Inner FEC sublayer in place of the PMA above the PMD. A set of generic examples are shown in Figure 176B-1. The PMA or Inner FEC below the PCS converts the number of PCS lanes (q) to the required number of PMD lanes (p).

### **PMA/AUI** implementation examples 800GMII extender examples



Figure 176B–5—800GBASE Physical Layer implementations with a 800GMII Extender with one and two physically instantiated interfaces

#### Table 176B-1-800 Gb/s 32:4:32 and 32:8:32 PMA instantiations

Sublayer	Clause/Annex	Description
800GBASE-R 32:n PMA	n = 8: 173 n = 4: 176	*
800GAUI-n	n = 8: 120F, 120G n = 4: 176D, 176E	
800GBASE-R n:32 PMA	n = 8: 173 n = 4: 176	

#### Table 176B-3-800 Gb/s PMA 32:4:8:32 and 32:8:4:32 (n ≠ m) instantiations

Sublayer	Clause/Annex	Description
800GBASE-R 32:m PMA	m = 8: 173 m = 4: 176	
800GAUI-m	m = 8: 120F, 120G m = 4: 176D, 176E	
800GBASE-R m:32 PMA	m = 8: 173 m = 4: 176	
800GBASE-R 32:n PMA	n = 8: 173 n = 4: 176	
800GAUI-n	n = 8: 120F, 120G n = 4: 176D, 176E	
800GBASE-R n:32 PMA	n = 8: 173 n = 4: 176	

### PMA/AUI implementation examples 800GBASE-R PHY examples



Figure 176B-6-800GBASE-R PHYs with one and two physically instantiated interfaces

Sublayer	Clause/Annex	Description
800GBASE-R 32:n PMA	n = 8: 173 n = 4: 176	
800GAUI-n	n = 8: 120F, 120G n = 4: 176D, 176E	
800GBASE-R n:n PMA	n = 8: 173 n = 4: 176	

Table 176B-4-800 Gb/s PMA 32:4:4 and 32:8:8 (n = p) instantiation

Table 176B-9-800 Gb/s PMA 32:4:8:4 and 32:8:4:8 ( $m \neq n, n \neq p$ ) instantiations

Sublayer	Clause/Annex	Description
800GBASE-R 32:m PMA	m = 8: 173 m = 4: 176	
800GAUI-m	m = 8: 120F, 120G m = 4: 176D, 176E	
800GBASE-R m:32 PMA	m = 8: 173 m = 4: 176	
800GBASE-R 32:n PMA	n = 8: 173 n = 4: 176	
800GAUI-n	n = 8: 120F, 120G n = 4: 176D, 176E	
800GBASE-R n:32 PMA	n = 8: 173 n = 4: 176	
800GBASE-R 32:p PMA	<i>p</i> = 8: 173 <i>p</i> = 4: 176	

### **PMA/AUI** implementation examples Example usage

Change the title and text of 171.4 as follows:

#### 171.4 800GAUI-n and 1.6TAUI-n

An 800GMII Extender may use any of the following electrical interfaces for the connection between its PMA sublayers, as shown in Figure 171–1:

- 800GAUI-8 chip-to-chip (Annex 120F)
- 800GAUI-8 chip-to-module (Annex 120G)
- <u>800GAUI-4 chip-to-chip (Annex 176C)</u>
- <u>800GAUI-4 chip-to-module (Annex 176D)</u>
- The 800GAUI-n may be instantiated using any form described in 176B.6.1.

A 1.6TMII Extender may use any of the following electrical interfaces for the connection between its PMA sublayers, as shown in Figure 171-1:

- <u>1.6TAUI-16 chip-to-chip (Annex 120F)</u>
- <u>1.6TAUI-16 chip-to-module (Annex 120G)</u>
- <u>1.6TAUI-8 chip-to-chip (Annex 176C)</u>
- <u>1.6TAUI-8 chip-to-module (Annex 176D)</u>
- The 1.6TAUI-n may be instantiated using any form described in 176B.7.1.

174.2.4 Physical Medium Attachment (PMA) sublayer

The PMA sublayer provides a medium-independent means to support the use of a range of physical media.

The 1.6TBASE-R SM-PMA is specified in Clause 176.

174.2.5 Attachment unit interface (1.6TAUI-n)

The 1.6 Tb/s Attachment Unit Interface (1.6TAUI-n) provides an electrical interface within a 1.6TBASE-R PHY or 1.6TMII Extender. The 1.6TAUI-n is defined for chip-to-chip (C2M) and chip-to-module (C2M) implementations.

The 1.6TAUI-n C2C is specified in Annex 120F and Annex 176D.

The 1.6TAUI-n C2M is specified in Annex 120G and Annex 176E.

The 1.6TAUI-n instantiations are described in 176B.7.

174.2.6 Inner FEC sublayer

# **Logic Topics**

### **MDIO**

- References to MDIO were interspersed through clauses.
- In practice, complex devices like these won't use MDIO.
- But will have some sort of management system.
- Proposing the following:
  - Use variables only throughout clause.
  - Then summarize these variables and point to MDIO subclauses in one place (table)
  - Clause 175 has already been modified in this way as an example
- If the TF agrees with this direction then the other new clauses will be updated to use the same approach

# Variable and MDIO references in Clause 119 (current approach)

#### 119.4 Loopback

When the PCS is in loopback, the PCS shall accept data on the transmit path from the 200GMII/400GMII and return it on the receive path to the 200GMII/400GMII. In addition, the PCS shall transmit what it receives from the 200GMII/400GMII to the PMA sublayer, and shall ignore all data presented to it by the PMA sublayer. If a Clause 45 MDIO is implemented, then the PCS is placed in the loopback when the loopback bit from the PCS control 1 register (bit 3.0.14) is set to a one.

MDIO references scattered throughout
clause, whenever a control/status variable is defined (redundant, can delete).

#### 119.3.1 PCS MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the PCS. If MDIO is implemented, it shall map MDIO control bits to PCS control variables, as shown in Table 119–4, and MDIO status bits to PCS status variables, as shown in Table 119–5.

#### Table 119-4—MDIO/PCS control variable mapping

MDIO control variable	PCS register name	Register/bit number	PCS control variable	
Reset	PCS control 1 register	3.0.15	reset	
Loopback	PCS control 1 register	3.0.14	Loopback	
Transmit test-pattern enable	BASE-R PCS test-pattern control register	3.42.3	tx_test_mode	
LPI_FW	EEE control and capability	3.20.0	LPI_FW	
PCS FEC bypass indication enable	PCS FEC control register	3.800.1	FEC_bypass_indication_enable	
PCS FEC degraded SER enable	PCS FEC control register	3.800.2	FEC degraded SER enable	

Single section that summarizes mapping between MDIO register/bit and control/status variables

No cross-reference provided to MDIO register/bit

No cross-reference provided to where the control variable is defined within this Clause (i.e. 119.4 in the case of loopback)

# Variable and MDIO references in Clause 175 (proposed approach)

#### 175.7 PCS management

The following objects apply to PCS management. If an MDIO Interface is provided (see Clause 45), they are accessed via that interface. If not, it is recommended that an equivalent access is provided.

175.7.1 PCS MDIO function mapping

The optional MDIO capability described in Clause 45 defines several registers that provide control and status information for and about the PCS. If MDIO is implemented, it shall map PCS control variables to MDIO control bits as shown in Table 175–2 and PCS status variables to MDIO status bits as shown in Table 175–3. MDIO registers relevant to the 1.6TBASE-R PCS are described in 45.2.3.

Table 175–2—MDIO/PCS control variable mapping

PCS control variable	Variable reference	Register/bit number	Register/bit reference
reset	175.2.6.2.2	3.0.15	45.2.3.1
loopback	175.3	3.0.14	45.2.3.1
tx_test_mode	175.2.4.11	3.42.3	45.2.3.19
FEC_bypass_indication_enable	175.2.5.3	3.800.1	45.2.3.60
FEC_degraded_SER_enable	175.2.5.3	3.800.2	45.2.3.60
FEC_degraded_SER_activate_threshold	175.2.5.3	3.806, 3.807	45.2.3.64
FEC_degraded_SER_deactivate_threshold	175.2.5.3	3.808, 3.809	45.2.3.65
FEC_degraded_SER_interval	175.2.5.3	3.810, 3.811	45.2.3.66

This section provides a list of all control and status variables that are accessible via a management system, and a specific mapping to an MDIO management system is provided for reference

cross-reference to the subclause where the control/status variable is defined

cross-reference to the subclause that define the MDIO register/bit associated with this control/status variable.

no other references to Clause 45 and MDIO registers elsewhere in the clause

## **Electrical topics**

### List

- Clause order
- Package classes, host and cable assembly designations
- COM parameters
- Insertion loss, return loss, ERL
- Training, and other PMD specifications

### Clause order 178/179

- In this project we chose to place the Backplane (Clause 178) before Copper cable (Clause 179) based on the reach.
- This makes clause order consistent with the convention determined during the 802.3-2022 revision project for lists of PMDs.
- 802.3 has been inconsistent about this choice:
  - The same order was used in **802.3ba** (Clauses 84 and 85)
  - It was the other way around in 802.3bj (92 and 93), 802.3by (110 and 111), 802.3cd (136 and 137) and 802.3ck (162 and 163)
  - The order is not substantial
- Results of this change of order:
  - In D0.2 a substantial number of the specifications in Clause 178 (based on 163) and point forward (rather than back) to Clause 179 (based on 162).

# Package classes, host and cable assembly designations

- The concepts are written down in D0.2
- Nomenclature for package classes (A / B) was included in the adopted baseline (motion #10 in <u>November 2023</u>)
- Nomenclature for host and cable assembly was left TBD (motion #11 in <u>November 2023</u>)

### Issues due to multiple host, package, cable types

- Many system permutations due multiple package types, cable types, host types
- What combinations of package and "host channel" (see previous slide) lengths should be used in COM tests of cable assemblies
- How are receiver tests performed (test channels and calibration)
- Host or (CR PMD Tx) output characteristics
- Labeling

### **Host channel**

- The term "host channel" is commonly used, but is not well defined in 802.3
- In this project we chose it to describe the part of the channel from TP0d (including the package) to the MDI
  - This is not TP0 to TP2
- In some cases where a "channel" extends to TP2, it is marked explicitly, e.g., "TP0d to TP2"

### Training and other PMD specifications (cont.)

- The functional specification subclauses are still included in the PMD (unchanged from clause 162)
  - A possible solution is to add text in these subclauses that these functions are defined in the PMD based on their effect, but implementation can be in the adjacent PMA's physical interface
- There are still PMD delay, skew, and skew variation limits
  - These parameters are (theoretically) measurable at the PMD's test points
  - But the PMD's contribution (even to delay) is negligible; it would be more reasonable to allocate large values to the PMA and zero to the PMD
- We encourage participants to think about what's really the PMD's functionality and how the specifications reflect it

### COM

- Created new Annex 178A for definition of COM
- Reference model has changes from 93A
  - FFE
  - MMSE
  - maybe MLSE
  - many new parameters
- Points back to 93A where common methods are used.

### **COM** parameters

- The reference receiver framework in slides 5-15 of <u>healey\_3dj\_01\_2401</u> was adopted (as part of a "bucket", motion #7)
- New Annex 178A (see previous slide) specifies a receiver based on this framework, with CTLE, FFE and DFE
  - Names/Values for new FFE parameters (length, pre/post, tap limits, ...) have not been adopted
  - Other parameters known from Annex 93A, some were included in the baseline proposal <u>ran\_3dj\_01a\_2401</u>
- COM tables in electrical PMDs and AUI-C2C have are defined by baseline except notably No Rx FFE parameters.
  - Some parameter names were chosen in D0.2
  - In D1.0, where names have not been adopted we intend to add any missing Rx FFE parameters with names selected as necessary and with values TBD

### Insertion loss, return loss, ERL

- ERL parameters and IL/RL (of various modes) were left as TBD in the baseline proposal
- In D0.2, IL/RL equations and graphs are blank and/or listed with TBDs
- Values of parameters for calculating ERL are either copied from 802.3ck or changed to TBD (not consistent)
  - Consider everything as equally TBD
- Contributions are required!

### **Training and other PMD specifications**

- Training (now in PMA) in all interfaces replaces PMD control function and the two C2M module output modes (short, long) from 802.3ck
  - The specification is moved from the PMD clause to an annex associated with the PMA (Annex 176A)
- The PMD service interface and the AUI interface are now signals (continuous time)
  - The PMD is not expected to have any digital/sampled content
- The PMD functional specifications (signal detect, output disable) are defined by effects that are observable at the PMD's test points
  - Implementation is more likely to be fully within the PMA
- PMD delay, skew, and skew variation can still exist, but should be negligible compared to previously specified maximum values

# **Optical Topics**

### List

- Rewrite of signal detect subclauses
- Test patterns
- Parameter alignment
- C band channel model

### **Rewrite of signal detect subclauses**

- The editorial team decided the wording in the previous PMD global signal detect function subclauses was incorrect
  - SIGNAL\_DETECT is defined as a parameter, not a variable
  - SIGNAL\_DETECT is based on both optical power level and signal being BASE-R; it then says the PMD does not need to detect the signal presence
- Subclauses 180.5.4, 180.5.5, 182.5.4 and 182.5.5 contain the new updated wording
- Based on review and agreement on the updated wording, the corresponding subclauses in 181, 183, 185 and 187 will be similarly updated.

### **Test patterns**

- Clauses 182 and 183 utilize the new inner FEC sublayer documented in clause 177
- The PBRS generation in 182.9.1 and 183.9.1 is stated as defined in 120.5.11.2.2 and 120.5.11.2.3
- These subclauses state the PMA may optionally include a PBRS generator which does not include the new inner FEC
- The use of a test pattern not including the effects of the inner FEC is not a relevant test
- Suggesting revised wording that clarifies the PRBS test patterns (if needed) are created by the PMA and encoded by the inner FEC

### **Parameter alignment**

- The parameters in the adopted optical baselines for LR1 and ER1 did not align with each other or similar parameters in 802.3cw.
- Many parameter descriptions were updated to ensure alignment
- Several parameters were added to parameter tables to ensure alignment
  - A new parameter is shown as not having a specific value or TBD
- Several parameters were moved between the parameter tables to ensure alignment between TX, RX, link power budget and channel characteristics in all the PMD clauses

### C band channel model

- The adopted ER1 baseline did not include any optical channel model parameters
- Previous work in 802.3ct and .cw could not be leveraged due to the use of the DWDM black link
- Previous contributions proposing C band optical channel model parameters were leveraged to justify the values stated

# Terminology

### **Terminology Considerations**

- We need to adopt official terminology for the following:
  - BM-PMA/SM-PMA
  - xBASE-R Inner FEC
  - 800GBASE-LR1 Inner FEC
  - 200 Gb/s per lane AUI
- Either adopt them as above or adopt another term that is acceptable to the task force.

## **Thanks!**