

IEEE 802.3 Ethernet Working Group
DRAFT Liaison Communication

Source: IEEE 802.3 Working Group¹

To: Stefan Dahlfort President, MOPA
[REDACTED]

Kenneth Jackson "Contributions to SDOs" Work Item Driver, MOPA
[REDACTED]

CC: Alpesh Shah Secretary, IEEE-SA Standards Board
Secretary, IEEE-SA Board of Governors
[REDACTED]

Paul Nikolich Chair, IEEE 802 LMSC
[REDACTED]

Adam Healey Vice-chair, IEEE 802.3 Ethernet Working Group
[REDACTED]

Jon Lewis Secretary, IEEE 802.3 Ethernet Working Group
[REDACTED]

John D'Ambrosia Chair, IEEE P802.3dj Task Force
[REDACTED]

Mark Nowell Vice-chair, IEEE P802.3dj Task Force
[REDACTED]

Karl Bois Technical Committee Chair, OIF
[REDACTED]

Kimberly Naughton Project Manager, OIF
[REDACTED]

From: David Law Chair, IEEE 802.3 Ethernet Working Group
[REDACTED]

Subject: Liaison reply to "MOPA addressing the contribution of Optical Pluggable Transceivers to time synchronisation error in PTP networks, concerns over "segmented" FEC", 2 November 2023

Approval: Agreed at IEEE 802.3 closing plenary meeting, Denver, CO, USA, 14 March 2024

Dear Mr Dahlfort and members of MOPA,

Thank you for your liaison raising your concern about "segmented" FEC schemes, and their potential impact on time variation and possible impact on the class of a module.

IEEE 802.3 is aware of the importance of time synchronization accuracy in Precision Time Protocol (PTP) networks, which is one of many different types of networks that leverage the

¹ This document solely represents the views of the IEEE 802.3 Working Group and does not necessarily represent a position of the IEEE, the IEEE Standards Association, or IEEE 802.

IEEE 802.3 Ethernet standard. To that end, the standard is written in a flexible manner to enable as many different types of implementation choices as possible.

For example, an MII extender may serve different architectural purposes. The XGMII Extender, as noted in Clause 47.1, extends “the physical separation between MAC and PHY components in a 10 Gigabit Ethernet system distributed across a circuit board.” Another potential use of an MII extender is to enable port flexibility, by providing a mechanism for a MAC component to communicate with PHY components, via an Attachment Unit Interface (AUI), that leverage different FEC codes. The FEC code of the MII extender used to enable communication between the MAC and PHY components is terminated, and the new FEC code is applied in the Physical Coding Sublayer (PCS) of the PHY. However, in this instance idles, alignment markers, and codeword markers may be inserted / removed in both the extender sub-layers (XS) of an MII Extender and the PCS of the PHY, impacting the timestamping accuracy of the implementation.

IEEE Std 802.3cx™-2023 subclause 90.7.2 includes the following note –

When TX_NUM_BIT_CHANGE and RX_NUM_BIT_CHANGE are not available (e.g., over physical interfaces such as instantiated xMII or AUI), it is recommended to avoid insertion and removal of idles, alignment markers, and codeword markers in the sublayers below the xMII/AUI, when possible, to reduce timestamping accuracy impairments (see Annex 90A).

Today’s Ethernet PHYs can address time stamping accuracy impairments by following the above note.

However, there are specification choices that would prevent following the above note, such as in the noted proposal for 800GBASE-ER1 (see [nicholl 3dj 02a 2307.pdf](#)).

The noted proposal and a new objective for 20km over single-mode fiber were adopted at the January 2024 Interim meeting of the IEEE P802.3dj Task Force. **At the March 2024 Plenary the IEEE P802.3dj Task Force adopted [nicholl 3dj 02a 2307.pdf](#) as the logic baseline for the new 20km SMF objective.**

However, given the underlying issue with the proposal noted above, the IEEE P802.3dj Task Force needs to consider this issue with the PHYs it is developing. To assist the Task Force, it would be beneficial if MOPA could provide guidance on allocation of constant time error budget that addresses the Physical Layer.

As the development of the IEEE P802.3dj project continues, we will inform you of any additional information that may be relevant to your concern. In the meantime, we will be reviewing the noted technical paper (https://mopa-alliance.org/wp-content/uploads/2023/10/MOPA_Technical_Paper-v2.2-Final.pdf) in your liaison and may have follow-up question at a later date.

Information regarding future IEEE P802.3dj meetings may be found at <https://www.ieee802.org/3/dj/public/index.html>. We would encourage individuals from MOPA interested in contributing to participate.

Please note that we have copied members of the Optical Internetworking Forum (OIF), as they have sent liaisons to IEEE 802.3 indicating that their organization is working on an Implementation Agreement specifying 800ZR and 800LR Coherent Interfaces.

We look forward to the continued interaction of our two groups to ensure that Ethernet will sufficiently service the time synchronization accuracy requirements of PTP networks.

Sincerely,
David Law
Chair, IEEE 802.3 Ethernet Working Group

DRAFT