Baseline CRU Implementation Text for FECo and FECi PMDs

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Supporter List

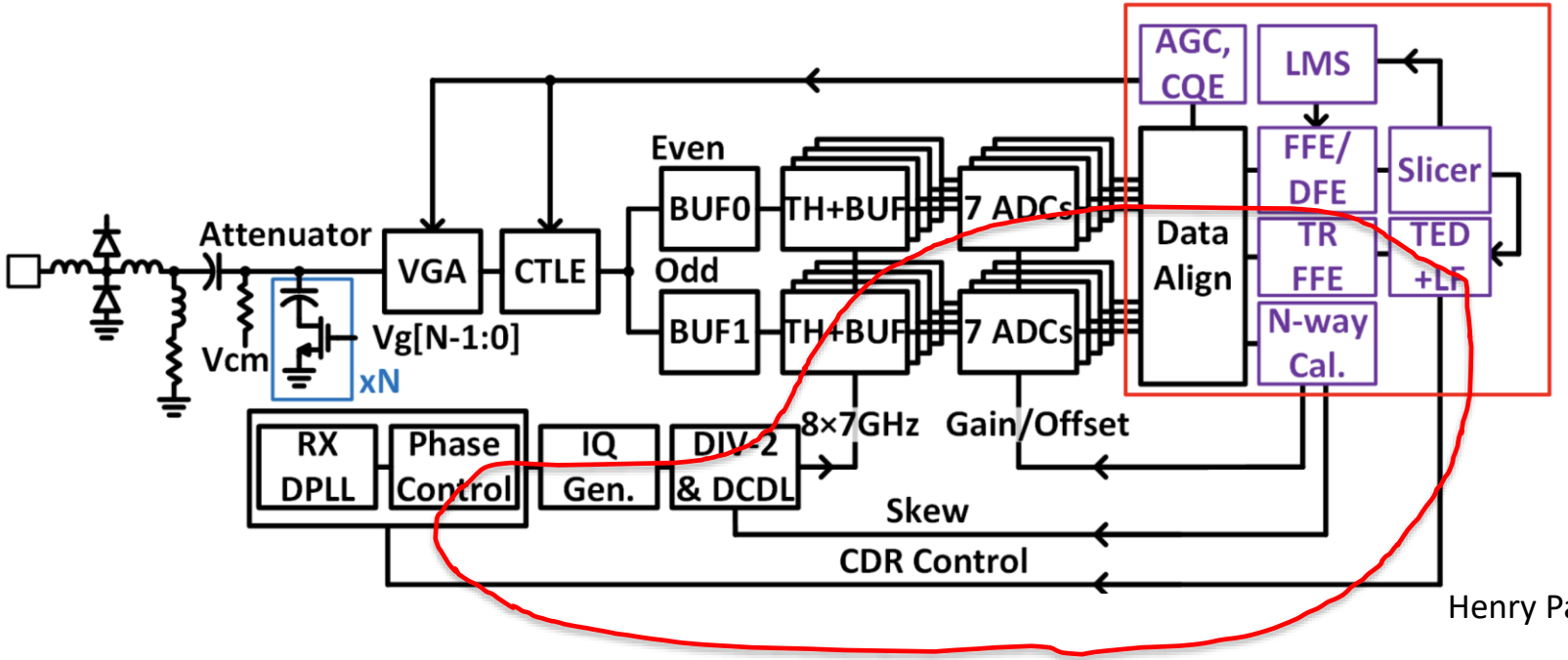
- Eric Maniloff – Ciena
- Adee Ran – Cisco
- Upen Kareti – Cisco
- Greg Le Cheminant – Keysight
- Arash Farhoodfar – Marvell
- Lenin Patra – Marvell
- Mike Dudek – Marvell
- Tobey P.-R. Li – MediaTek
- Pavel Zivny – Tek.

Overview

- Complexity of doubling CRU BW
- RJ estimation before 224 Gb/s SerDes availability
- RJ measured for three 224 Gb/s SerDes
- Baseline text to implement CRU BW for FECo PMDs motion 7 from May-23
- Need make a decision on FECi CRU BW
- Baseline text to implement CRU BW for FECi PMDs
- Summary.

The Challenge of Increasing CDR Tracking Bandwidth

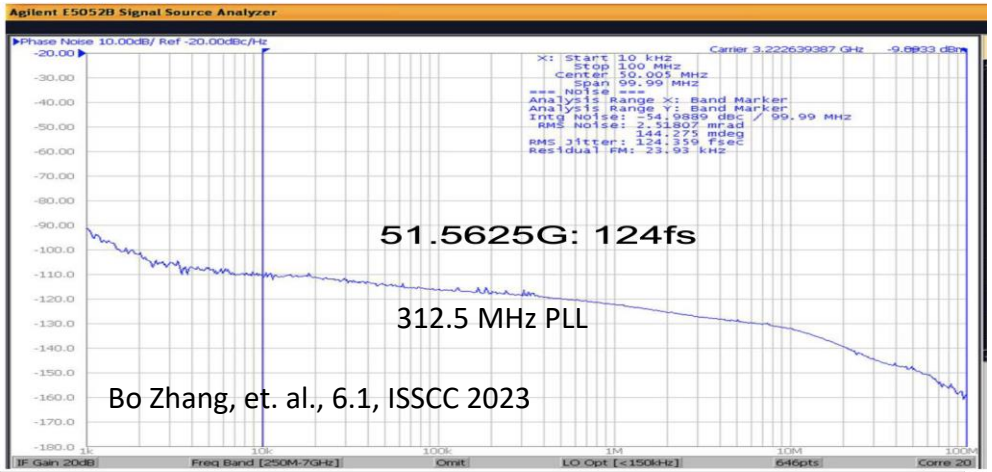
- **ADC SerDes ~112 GBd likely will use 32+ ways(64, 128) interleaved ADC with digital running at ~2 GHz requiring custom digital designs**
  - The latency introduced through large interleaved loop limits the CDR tracking BW
  - Doubling tracking BW to 8 MHz would require using much faster-higher power less interleaved ADCs and operating digital at 4+ GHz is just too fast.

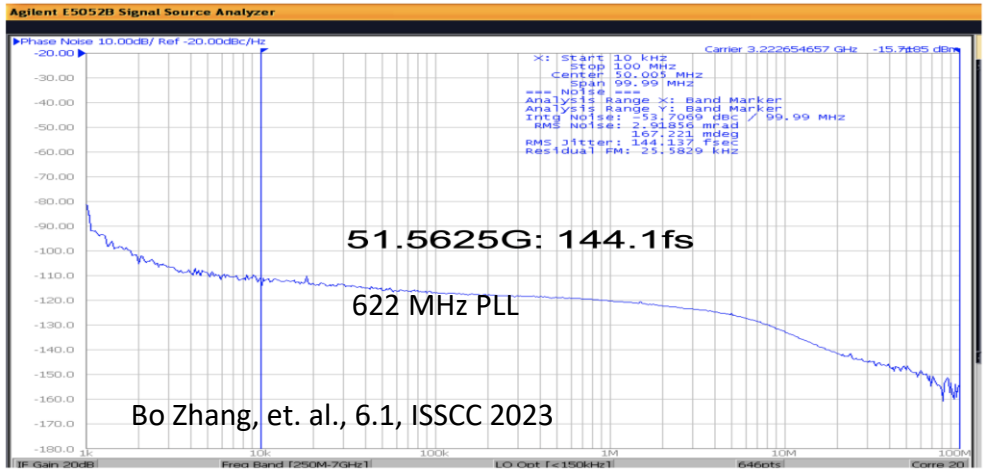


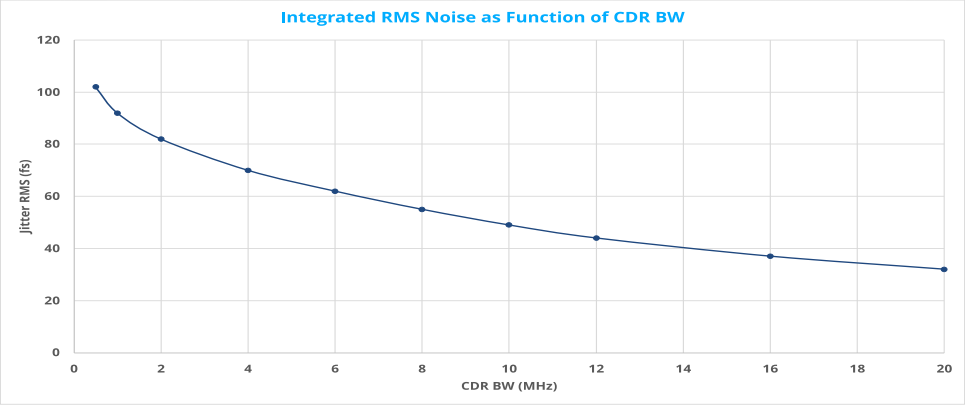
Henry Park, 6.2, ISSCC2023

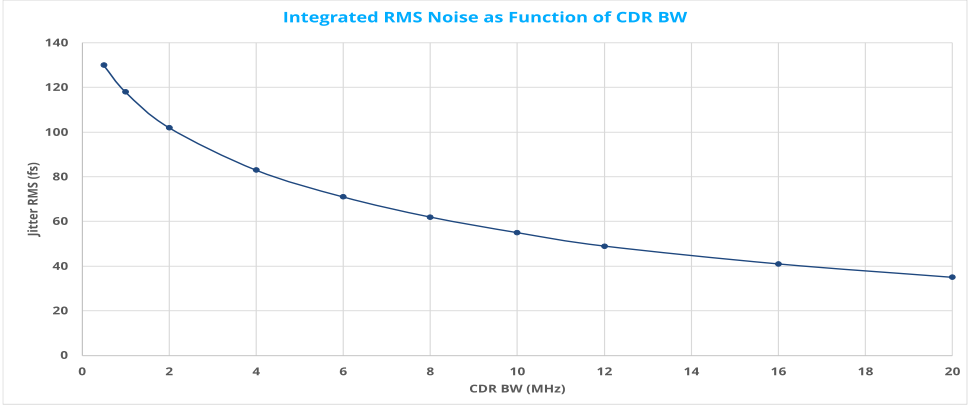
High Speed PLL Performance

- **Considering availability of low-cost oscillator doubling the CDR BW only provide small incremental relief to the transmitter, but doubling CDR BW is very substantial**
  - These results were originally presented in ghiasi_3dj_01a_2305 before actual 224 Gb/s SerDes demonstration that σ_{RJ} of 10 mUI can be met with 4 MHz CRU
  - There is only marginal benefit increasing CRU BW beyond 4 MHz, next will show actual 224 Gb/s SerDes results!





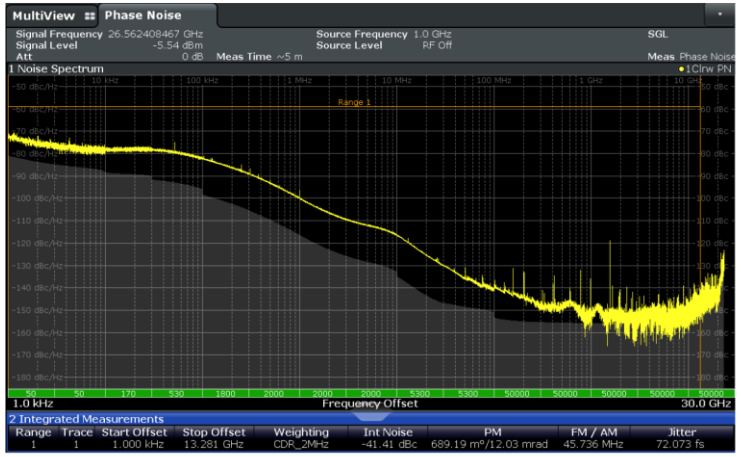




212 Gb/s DSP-Based PAM-4 Transceiver

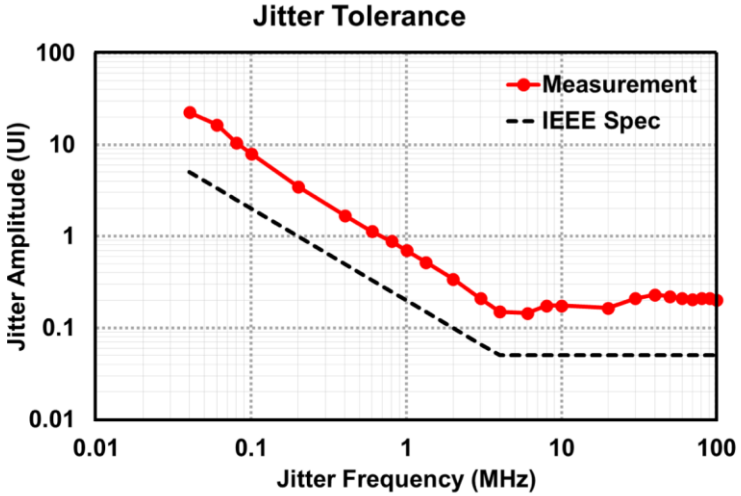
- **J.Q.Wang, et. al, "A 2.69pJ/b 212Gb/s DSP-Based PAM-4 Transceiver for Optical Direct-Detect Application in 5nm FinFET, ISSCC 2024", 7.1**
  - Wang σ_{RJ} of 72 fs reported for 2 MHz 2nd order CRU, σ_{RJ} with 4 MHz 1st order CRU expect to be lower.

TX Measurement: Random Jitter



- FSWP50
- 1100 clock pattern
- RJ = 72fs,rms
- 2M 2nd order CDR
- 1kHz to 13.28GHz

RX Measurement: Jitter Tolerance

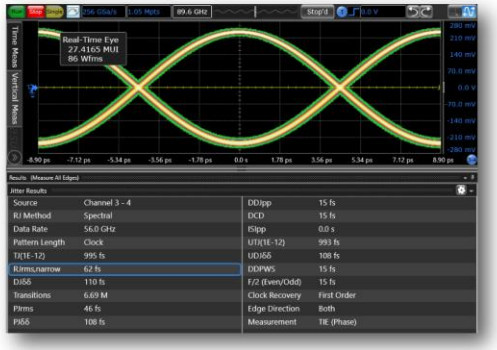


- PRBS test with BERT
- Additional injected jitter
- Pass mask with margin

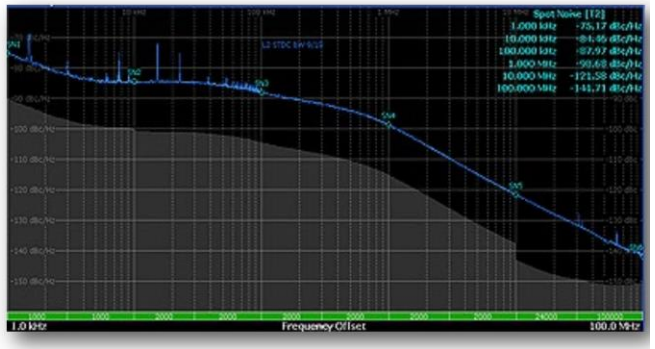
A 224Gb/s sub-pJ/b PAM-4 and PAM-6 DAC-Based Transmitter

- **Marco Cusmai, et. al, "A 224Gb/s sub-pJ/b PAM-4 and PAM-6 DAC-Based Transmitter in 3nm FinFET", ISSCC 2024, 7.2.**

Clock patterns (High frequency path)



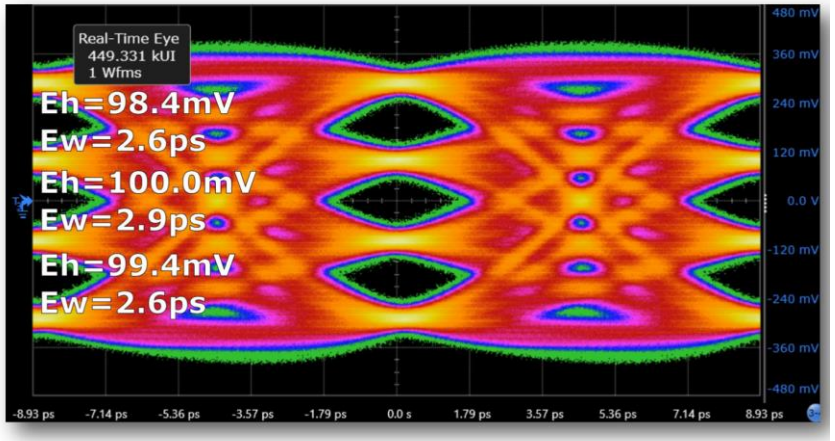
- **56GHz clock pattern**
  - 89.6GHz scope BW
  - 4MHz 1st order CDR
- **RJ=62fs**



- **28GHz clock pattern**
- **Phase noise analyzer (R&S FSWP50)**
- **-99dBc/Hz @1MHz offset from carrier**
- **21.2GHz to 30.0GHz PLL tuning range**

PAM-4 @ 224Gb/s (UI=8.9ps)

SNDR = 36.0dB
$J3u_{03}$ = 55mUI (490fs)
J_{RMS} = 16mUI (140fs)
EOJ = 16mUI (140fs)
RLM = 0.97
Power = 0.92pJ/b

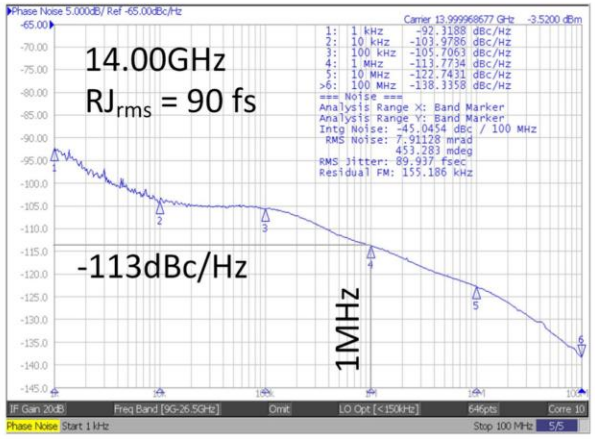


A 224Gb/s 3pJ/b 40dB Insertion Loss Transceiver

- **Dirk Pfaff, et. al., "A 224Gb/s 3pJ/b 40dB Insertion Loss Transceiver in 3nm FinFET CMOS", ISSCC 2024, 7.3.**

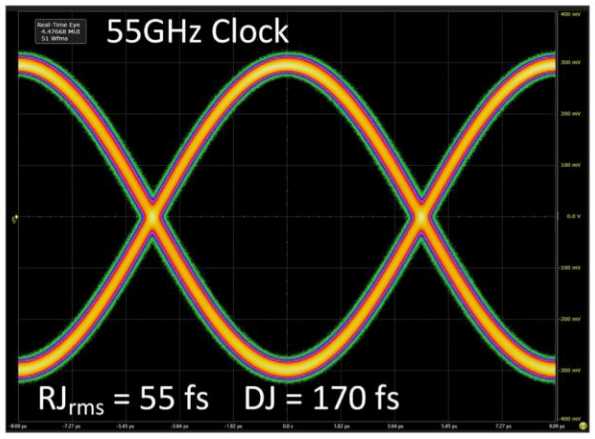
Clock Measurements

1/8 rate clock phase noise:



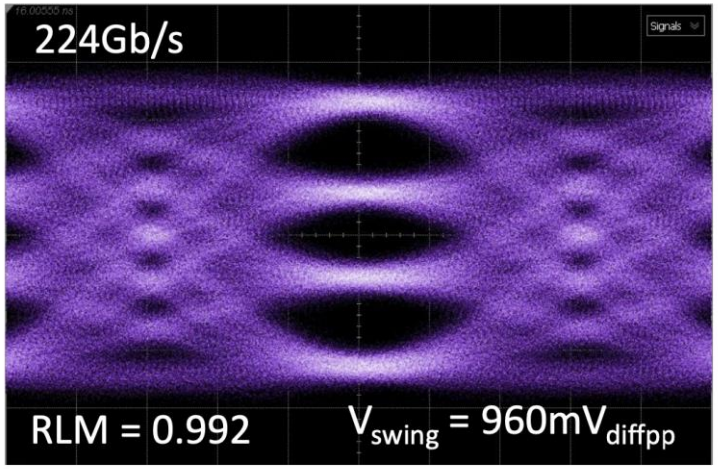
→90fs rms jitter (1kHz … 100MHz)

Full rate TX clock:



55fs rms jitter with 4MHz CDR

Transmitter Measurements



- 4MHz CDR BW (Sampling Scope)
- No TX FFE
- 5.5dB test fixture loss removed

Transmit Jitter and CRU BW

- **sun_3dj_01_2401 proposes to relax the transmit jitter and/or increase the CRU BW to mitigate transmit Rj**
  - Proposal suggest increasing σ_{RJ} from 10 mUI to 15 mUI
  - Also suggested to increase the CRU BW from 4 MHz to 8 MHz
- **3 ISSCC 2024 paper demonstrated 200G SerDes**
  - All 3 papers met transmit σ_{RJ} of 10 mUI
  - All 3 papers assumed CRU BW of 4 MHz
- **Three 224 Gb/s transceiver meets σ_{RJ} of 10 mUI and all 3 assume CRU BW of 4 MHz**
  - Doubling DSP receiver CDR BW to 8 MHz will add significant power and complexity, not to mention existing design are based on 4 MHz
  - The above 3 SerDes all met σ_{RJ} of 10 mUI, at least these SerDes don't need the relaxation
    - Small like ~2 mUI relaxation of σ_{RJ} of should be evaluated on its own merits without touching the CRU BW!

Text to Implement Motion 7 (May-23) for FECo Optical PMDs

- **Add "The clock recovery unit (CRU) has a corner frequency of 4 MHz and a slope of 20 dB/decade. The CRU can be implemented in hardware or software depending on oscilloscope technology" to TDECQ and TECQ definition 180.9.5/180.9.6 and 181.9.5/181.9.6**
- **Also add following figure, but after polarization rotator add two more loops to indicate fiber for TDECQ measurement. For TECQ refer to the same figure but measured without fiber.**

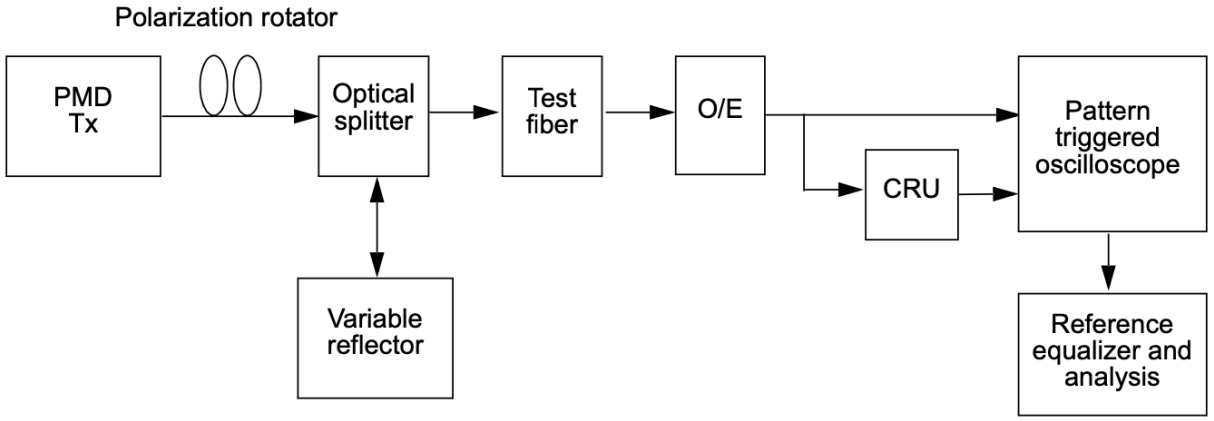


Figure 121–4—TDECQ conformance test block diagram

Text to Implement Motion 7 (May-23) for CR/KR PMDs

- **Add "The reference clock recovery unit (CRU) used in the measurement acts as a high-pass jitter filter with a corner frequency of 4 MHz and a slope of 20 dB/decade." to Linear fit to the measured waveform 179.9.4.1.1 and 180.9.4.1.1**
- **In receiver jitter tolerance to 179.9.5.4 section add "A PHY shall meet the FEC symbol error ratio requirement defined in Table 179–16 for each pair of jitter frequency and peak-to-peak amplitude values listed in Table 179–17 with jitter added to all lanes".**

179-17

Table ~~162~~–17—Receiver jitter tolerance parameters

Parameter	Case A	Case B	Case C	Case D	Case E	Case F	Units
Jitter frequency	0.04	0.4	1.333	4	12	40	MHz
Jitter amplitude (pk-pk)	5	0.5	0.15	0.05	0.05	0.05	UI

CRU BW for FECi PMDs

- **FECo PMDs CRU BW=f_{Baud}/26562.5 or 4 MHz**
- **We need to make a decision on the FECi CRU BW**
  - Option I - CRU BW=f_{Baud}/26562.5 or 4.27 MHz
  - Option II – CRU BW= f_{Baud}/28359.375 or 4 MHz
  - Either of the above option will allow us to make progress and difference of 0.27 MHz is well within the design tolerance
- **The feedback from T&M providers is that the difference is so small and within the precision of the loop tuning and its impact on any measurements probably does not warrant the hassle of having two values**
- **Proposed to adopt 4 MHz for all FECi PMDs.**

Text to Implement for FECi Optical PMDs

- **Add "The clock recovery unit (CRU) has a corner frequency of 4 MHz and a slope of 20 dB/decade. The CRU can be implemented in hardware or software depending on oscilloscope technology" to TDECQ and TECQ definition 182.9.5/182.9.6 and 183.9.5/183.9.6**
- **Also add following figure, but after polarization rotator add two more loops to indicate fiber for TDECQ measurement. For TECQ refer to the same figure but measured without fiber.**

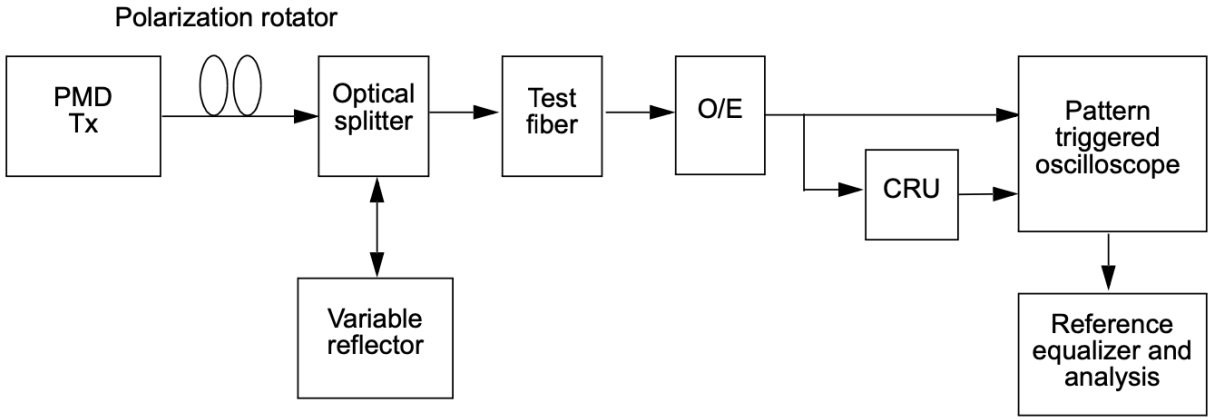


Figure 121–4—TDECQ conformance test block diagram

Summary

- **Three 224 Gb/s SerDes meets with margin σ_{RJ} of 10 mUI with 4 MHz CRU**
  - Considering substantial ADC receiver complexity there is no justification to double the CRU BW
- **Provided text how to implement CRU motion 7 May-23 for FECo PMDs**
- **Provided text how to implement CRU for FECi PMDs currently TBD with 4 MHz**
  - Assuming recommendation to adopt 4 MHz for FECi CRU BW motion passes.