200G/Lane KR Baseline for 802.3dj

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Background

- Progresses had been made in 802.3dj related to KR spec development[1]
  - CRU BW and JTOL corner frequency had been set at 4 MHz
  - DER_0 had been set to 2e−4 for KR and CR
  - die-to-die insertion loss (IL) <= 40 dB at 53.125 GHz had been set for KR and CR
  - COM reference die model and parameters had been set for KR, CR, AUI (C2M/C2C)[2]
  - COM reference package model and parameters (Class A and B) had been set KR and CR[3]
- Several 200G/Lane TCs had been demonstrated and related results had been published [4],[5],[6],[7]
- OIF/CEI-224G-LR-PAM4 spec draft had been developed[8]
- It is the time to start developing the KR baseline for 802.3dj

Methodologies

- Start with the 802.3ck 100G/Lane KR spec [9]
- Use the same test fixture related signal definitions (TP0, TP0V for TX, TP5, TP5V for RX)
- Maintain BAUD independent TX/RX parameters when appropriate
- Frequency/time scale for BAUD dependent TX/RX parameters
- Validated and checked against available TC measurements and silicon/circuit simulations/modeling over PVT and distributions
- Leverage the OIF/CEI-224G-LR-PAM4 latest specification draft[9]
  - Maintain the alignment when appropriate/possible
  - Benefit the datacom, telecom, DC, AI/ML, and ecosystem at large

Scope of the Baseline

- TX parameter specifications
  - no dependence on the reference RX EQ which are under development/to be matured
- RX JTOL parameter specifications
  - no dependence on the reference RX EQ which are under development/to be matured

Proposed TX Spec at TP0v (Part1)

~~Table 163–5~~ –Summary of transmitter specifications at TP0v

Parameter	Reference	Value	Units
Signaling rate, each lane (range)	TBI	~~53.125 ± 50 ppm~~[a] 106.25 ± 50 ppm	GBd
Differential pk-pk voltage (max)[b] Transmitter disabled Transmitter enabled	~~93.8.1.3~~	30 ✓ 1200 ✓	 mV mV
DC common-mode voltage (max)[b]	~~93.8.1.3~~	1 ✓	V
DC common-mode voltage (min)[b]	~~93.8.1.3~~	0.2 ✓	V
Low-frequency peak-to-peak AC common-mode voltage, VCM_{LF} (max)	~~162.9.4.4~~	30 ✓	mV
Signal to AC common-mode noise ratio, *SCMR* (min)	~~163.9.2.6~~	15 ✓	dB
Difference effective return loss, *dERL* (min)	~~163.9.2.2~~	–3 ✓	dB
Common-mode to common-mode return loss, *RLcc* (min)	~~163.9.2.3~~	3.25 ✓	dB
Difference steady-state voltage, dv_f (min)	~~163.9.2.4~~	0 ✓	V
Difference linear fit pulse peak ratio, dR_{peak} (min)	~~163.9.2.5~~	0 ✓	—
Level separation mismatch ratio, R_{LM} (min)	~~162.9.4.2~~	0.95 ✓	—

Proposed TX Spec at TP0v (Part2)

~~Table 163–5~~ TBD –Summary of transmitter specifications at TP0v *(continued)*

Parameter	Reference	Value	Units
Transmitter waveform			
absolute value of step size for all taps (min)	~~162.9.4.1.4~~	~~0.005~~	—
absolute value of step size for all taps (max)	~~162.9.4.1.4~~	~~0.025~~	—
value at minimum state for $c(-3)$ (max)	~~162.9.4.1.5~~	~~0.06~~	—
value at maximum state for $c(-2)$ (min)	~~162.9.4.1.5~~	~~0.12~~ TBD	—
value at minimum state for $c(-1)$ (max) TBD	~~162.9.4.1.5~~	~~0.34~~	—
value at minimum state for $c(0)$ (max)	~~162.9.4.1.5~~	~~0.5~~	—
value at minimum state for $c(1)$ (max)	~~162.9.4.1.5~~	~~0.2~~	—
Signal-to-noise-and-distortion ratio, SNDR (min)	~~162.9.4.6~~	~~32.5~~ TBD	dB
Signal-to-residual-intersymbol-interference ratio, SNR_{ISI} (min)	~~162.9.4.3~~	~~28~~ TBD	dB
Jitter (max)[c]			
J_{RMS}	~~162.9.4.7~~	~~0.023~~ TBD	UI
~~J3u$_{03}$~~ J2.7u$_{03}$	~~162.9.4.7~~	~~0.106~~ TBD	UI
~~J3u~~ J2.7	~~162.9.4.7~~	~~0.115~~ TBD	UI
~~Even-odd~~ jitter, pk-pk	~~162.9.4.7~~	0.025 ✓	UI

[a] For a PMD in the same package as the PCS sublayer. In other cases, the signaling rate is derived from the input to the PMD transmit function provided by the adjacent PMA sublayer.

[b] Measurement uses the method described in 93.8.1.3 with the exception that the PRBS13Q test pattern is used.

[c] ~~J3u~~ J2.7u, J_{RMS}, and even-odd jitter measurements are made with a single transmit equalizer setting selected to compensate for the loss of the transmitter package and TP0 to TP0v test fixture.

*Note that the change of J3u ->J2.7u is due to the DER_0 is now 2e-4, while J3u is for DER_0 of 1e-4.

Proposed TX Spec at TP0v (Part3)

~~163.9.2.1.3~~ Test fixture common-mode to common-mode return loss

TBD

The common-mode to common-mode return loss of the test fixture shall be greater than or equal to 6 dB at all frequencies between 0.2 GHz and ~~40~~ 80 GHz.

~~163.9.2.2~~ Transmitter difference ERL

TBD

The difference ERL of the transmitter at TP0v is computed using the procedure in 163A.3.2.2 with the values in ~~Table 163–7 and Table 163–11~~ TBD TBD, and with the value of T_{fx} equal to twice the delay from TP0 to TP0v.

The difference ERL at TP0v shall be greater than or equal to *dERL* (min) in ~~Table 163–5.~~ TBD

~~Table 163–7~~—Transmitter and receiver ERL parameter values

TBD

Parameter	Symbol	Value	Units
Transition time associated with a pulse	T_r	~~0.01~~ 0.005	ns
Incremental available signal loss factor	β_x	0	GHz
Permitted reflection from a transmission line external to the device under test	ρ_x	0.618	—
Length of the reflection signal	N	~~200~~ 400	UI
Equalizer length associated with reflection signal	N_{bx}	~~21~~ TBD	UI
Tukey window flag	tw	1	—

Proposed TX Spec at TP0v (Part4)

~~163.9.2.3~~ Transmitter common-mode to common-mode return loss

TBD

The common-mode to common-mode return loss shall be greater than or equal to *RLcc* (min) in ~~Table 163–5~~ TBD at all frequencies between 0.2 GHz and ~~40~~ 80 GHz.

~~163.9.2.4~~ Difference steady-state voltage

TBD

The difference steady-state voltage of the transmitter at TP0v is computed using the procedure in ~~163A.3.2.1~~ TBD with N_v = ~~200~~ 400 and other parameter values specified in ~~Table 163–11~~ TBD.

The difference steady-state voltage at TP0v shall meet the specification dv_f (min) in ~~Table 163–5~~ TBD.

~~163.9.2.5~~ Difference linear fit pulse peak ratio

TBD

The difference linear fit pulse peak ratio of the transmitter at TP0v is computed using the procedure in 163A.3.2.1 with parameters specified in ~~Table 163–11~~ TBD.

The difference linear fit pulse peak ratio at TP0v shall meet the specification dR_{peak} (min) in ~~Table 163–5~~ TBD.

Proposed TX Spec at TP0v (Part5)

- Signal to AC common-mode noise ratio is calculated using the measurement method specified in 163.9.2.6 (with the following exception TBDs)

~~163.9.2.6~~ Signal to AC common-mode noise ratio

TBD

Signal to AC common-mode noise ratio, *SCMR*, is calculated using Equation (~~163–1~~).

TBD

$$SCMR = 20\log_{10}\left(\frac{v_{peak}}{VCM_{FB}}\right) \qquad (\text{~~163–1~~})$$

TBD

where

SCMR	is the signal to AC common-mode noise ratio in dB
v_{peak}	is defined in ~~162.9.4.1.2~~
VCM_{FB}	is the full-band peak-to-peak AC common-mode voltage defined by the method specified in ~~162.9.4.4~~ and measured with the transmitter equalization set to "no equalization"

TBD

TBD

The signal to AC common-mode noise ratio shall meet the specification for *SCMR* (min) in ~~Table 163–5.~~

TBD

Proposed RX Spec at TP5v (Part1)

Table ~~163–8~~ Summary of receiver specifications at TP5v

Parameter	Reference	Value	Units
Signaling rate, each lane (range)	~~163.9.3.1~~	~~53.125 ± 100 ppm~~ 106.25 ± 100 ppm	GBd
Difference effective return loss, *dERL* (min)	~~163.9.3.3~~	–3 ✓	dB
Differential-mode to common-mode return loss, *RLcd*	~~163.9.3.4~~	Equation ~~(163–2)~~ TBD	dB
Interference tolerance	~~163.9.3.5~~	Table ~~163–9~~ TBD	—
Jitter tolerance	~~163.9.3.6~~	Table ~~162–17~~ Slide 13	—

Proposed RX Spec at TP5v (Part2)

~~163.9.3.6~~ Receiver jitter tolerance

TBD

Receiver jitter tolerance is verified for each pair of jitter frequency and peak-to-peak amplitude values listed in Table ~~162–17~~. The test setup shown in Figure 93–12, or its equivalent, is used. TP0v (TP5v) replaces TP0a (TP5a) in Annex 93A, Annex 93C, and Annex 120D. The test channel meets the insertion loss requirement for Test 2 in Table ~~163–9~~. The synthesizer frequency is set to the specified jitter frequency and the synthesizer output amplitude is adjusted until the specified peak-to-peak jitter amplitude for that frequency is measured at TP0v. The test procedure is the same as the one described in 163.9.3.5, with the following exceptions:

TBD, see slide 13

TBD

a) No broadband noise is added.

b) The test channel COM, calculated per items 3) through 7) in 93C.2, is at least 3 dB.

c) For the COM parameter calibration described in 93C.2 item 7), the test channel transmitter J_{RMS} and ~~J3u~~ values are measured with the jitter frequency and amplitude set according to Case F from Table ~~162–17~~.

J2.7u

TBD, see slide 13

The receiver under test shall meet the FEC symbol error ratio ~~in Table 163–9~~ for each case in Table ~~162–17~~.

TBD

TBD, see slide 13

Proposed RX Spec at TP5v (Part3)

Table ~~162–17~~ —Receiver jitter tolerance parameters

TBD

Parameter	Case A	Case B	Case C	Case D	Case E	Case F	Units
Jitter frequency	0.04	0.4	1.333	4	12	40	MHz
Jitter amplitude (pk-pk)	5	0.5	0.15	0.05	0.05	0.05	UI

References

[1] https://www.ieee802.org/3/dj/projdoc/KeyMotions_3dj_240125.pdf

[2] https://www.ieee802.org/3/dj/public/24_01/lim_3dj_01_2401.pdf

[3] https://www.ieee802.org/3/dj/public/23_11/lim_3dj_01a_2311.pdf

[4] J. Kim et al, "A 224Gb/s DAC-Based PAM-4 Transmitter with 8-Tap FFE in 10nm CMOS", ISSCC, 2021.

[5] A. Khairi "A 1.4 pJ/b 224 Gb/s- PAM4 SERDES Receiver with 31 dB Loss Compensation ", ISSCC, 2022.

[6] M. Cusmai et al., "A 224Gb/s sub-pJ/b PAM-4 and PAM-6 DAC-Based Transmitter in 3nm FinFET", ISSCC, 2024.

[7] D. Pfaff et al. "A 224Gb/s 3pJ/b 40dB Insertion Loss Transceiver in 3nm FinFET CMOS", ISSCC, 2024.

[8] oif2023.235.02

[9] https://ieeexplore.ieee.org/document/9999414

Thank You!