Update to 200Gbps/Lane Electrical Interface Link Simulation

Tobey P.-R. Li

MediaTek

IEEE P802.3dj Task Force

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Outline

- Background and Introduction
- Update to Electrical Interface Link Simulation
- Further Investigation on CR Host IL Budget
- Considerations on Reliable MLSE Improvement
- Summary

Background and Introduction

- As in motions_3cwdfdj_2401 (Motion #10), TF adopted reference receiver framework of RxFFE + 1-tap DFE along with
  - New MMSE optimization procedure, see healey_3dj_01_2401
  - COM progress update in lusted_3dj_elec_01a_240229
- This presentation updates link performance of 200Gbps/lane electrical interfaces with COM 4.4beta to help progress
  - Channel insertion loss for 200G/lane AUI C2M electrical interface
  - Further study on CR host IL budget
  - Incorporation of reliable MLSE improvement
  - This is NOT a baseline proposal, further parameter adjustment is required with completed COM modeling
- *From COM4.3 to COM 4.4beta*
  - *Fix indexing bugs*
  - *Refinement of floating FFE location search based on FOM optimization*

Channel Test Cases

CR/KR Channel Source	Test Cases
shanbhag_3dj_01_2305	6
kocsis_3dj_02_2305	5
lim_3dj_03_230629	1
lim_3dj_04_230629	1
lim_3dj_07_2309	1
akinwale_3dj_02_2311	4
weaver_3dj_02_2311	12
mellitz_3dj_02_elec_230504	27
weaver_3dj_02_2305	36
shanbhag_3dj_02_2305	4
weaver_3dj_elec_01_230622	4
akinwale_3dj_01_2310	7
Total	108

C2M Channel Source	Test Cases
rabinovich_3df_01_2209	3
rabinovich_3df_02_2209	3
rabinovich_3dj_02_230116	1
rabinovich_3dj_03_230116	1
shanbhag_3dj_03_2305	6
akinwale_3dj_02_2307	28
akinwale_3dj_03_2307	27
akinwale_3dj_04_2307	28
lim_3dj_01_230629	1
lim_3dj_02_230629	1
weaver_3dj_elec_02_230831	32
lim_3dj_06_2309	1
gore_3dj_elec_02_231026	18
karati_3dj_elec_02_240111	60
Total	210

Package Test Cases

z_p select	[1 2]
.START	PKG_LowR_CLASSA
Table 93A–3 parameters	
Parameter	**Setting**
package_tl_gamma0_a1_a2	[0.0005 0.00089 0.0002]
package_tl_tau	0.006141
package_Z_c	[87.5 87.5 ; 95 95 ; 100 100; 100 100]
R_d	[50 50]
z_p (TX)	[12 33 33 33 ; 1.8 1.8 1.8 1.8 ; 0 0 0 0 ; 0 0 0 0]
z_p (NEXT)	[12 33 33 33 ; 1.8 1.8 1.8 1.8 ; 0 0 0 0 ; 0 0 0 0]
z_p (FEXT)	[12 33 33 33 ; 1.8 1.8 1.8 1.8 ; 0 0 0 0 ; 0 0 0 0]
z_p (RX)	[12 33 33 33 ; 1.8 1.8 1.8 1.8 ; 0 0 0 0 ; 0 0 0 0]
C_p	[0.4e-4 0.4e-4]
A_v	[0.413 0.413 0.413 0.413]
A_fe	[0.413 0.413 0.413 0.413]
A_ne	[0.600 0.600 0.600 0.600]
.END	

z_p select	[1 2 3 4]
.START	PKG_HiR_CLASSB
Table 93A–3 parameters	
Parameter	**Setting**
package_tl_gamma0_a1_a2	[0.0005 0.00065 0.000293]
package_tl_tau	0.006141
package_Z_c	[87.5 87.5 ; 95 95 ; 100 100; 78 78]
R_d	[50 50]
z_p (TX)	[8 24 30 45 ; 2 2 2 2; 1.3 1.3 1.3 1.3 ; 1.5 1.5 1.5 1.5]
z_p (NEXT)	[8 24 30 45 ; 2 2 2 2; 1.3 1.3 1.3 1.3 ; 1.5 1.5 1.5 1.5]
z_p (FEXT)	[8 24 30 45 ; 2 2 2 2; 1.3 1.3 1.3 1.3 ; 1.5 1.5 1.5 1.5]
z_p (RX)	[8 24 30 45 ; 2 2 2 2; 1.3 1.3 1.3 1.3 ; 1.5 1.5 1.5 1.5]
C_p	[0.4e-4 0.4e-4]
A_v	[0.413 0.413 0.413 0.413]
A_fe	[0.413 0.413 0.413 0.413]
A_ne	[0.600 0.600 0.600 0.600]
.END	

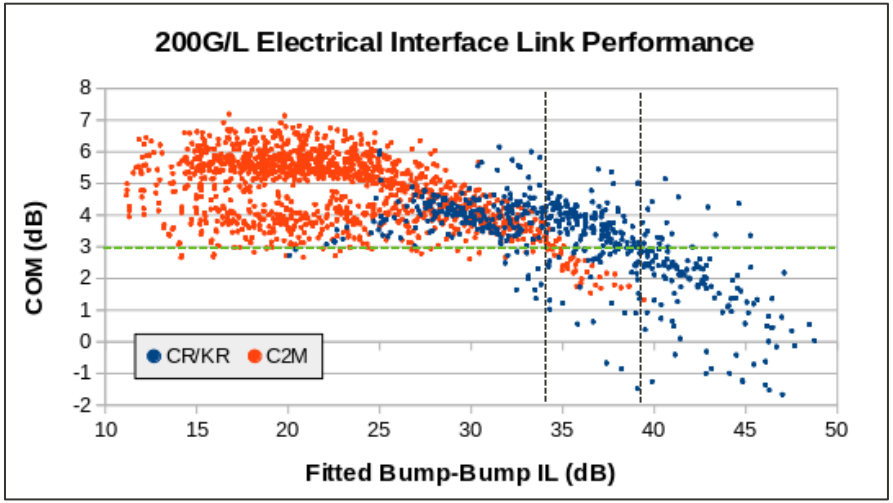
.START	PKG_Module
Table 93A–3 parameters	
Parameter	**Setting**
package_tl_gamma0_a1_a2	[0.0005 0.00089 0.0002]
package_tl_tau	0.006141
package_Z_c	[87.5 87.5 ; 95 95 ; 100 100; 100 100]
R_d	[50 50]
z_p (TX)	[8 8 8 8 ; 0 0 0 0 ; 0 0 0 0 ; 0 0 0 0]
z_p (NEXT)	[8 8 8 8 ; 0 0 0 0 ; 0 0 0 0 ; 0 0 0 0]
z_p (FEXT)	[8 8 8 8 ; 0 0 0 0 ; 0 0 0 0 ; 0 0 0 0]
z_p (RX)	[8 8 8 8 ; 0 0 0 0 ; 0 0 0 0 ; 0 0 0 0]
C_p	[0.4e-4 0.4e-4]
.END	

- **CR & KR simulation**
  - **TX & RX: PKG-A/PKG-B**
- **C2M simulation**
  - **TX: PKG-A/PKG-B**
  - **RX: Module PKG**

Initial Look at Electrical Link Performance

- Reference parameters highlight
  - EQ parameter is NOT a baseline proposal, further adjustment is required with the completed COM modeling
  - See Appendix for detail COM setting

	C2M	CR & KR
DER_0	2.00E-05	2.00E-04
N_b	1	1
b_max (1)	0.75	0.75
ffe_pre_tap_len	5	5
ffe_post_tap_len	10	10
N_bg	1	1
N_bf	4	4
N_f	60	60
eta_0	1.25E-08	6.00E-09
MLSE	0	0

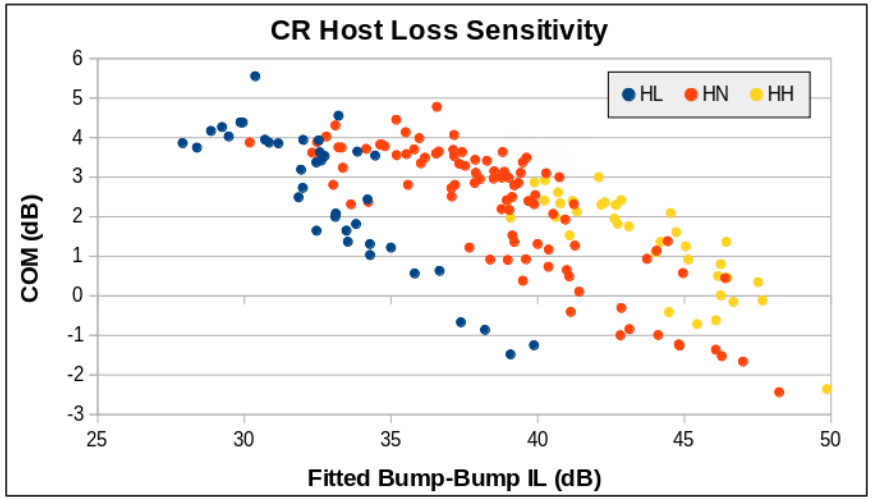


- Additional EQ capability required to provide >1dB COM margin in handling highly reflective channels
- ~5-6dB link budget difference between CR/KR & C2M under the same EQ complexity

Further Investigation on CR Host IL Budget

- **Adopted CR host loss budget**
  - See motions_3cwdfdj_2311 (Motion 11)

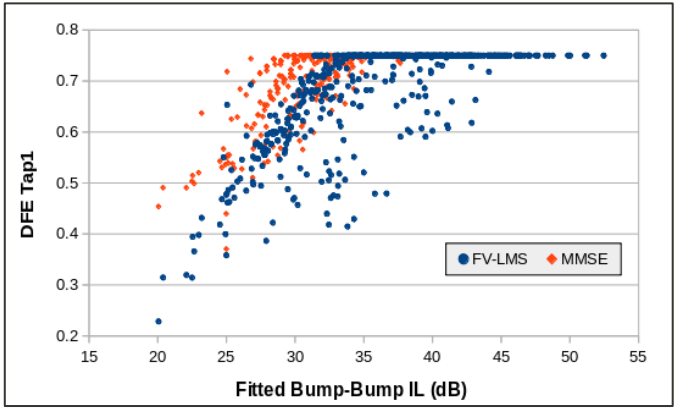
Host Architecture	PKG + Host PCB IL
Host-Low (HL)	6.5 dB
Host-Nominal (HN)	11.5 dB
Host-High (HH)	16.5 dB

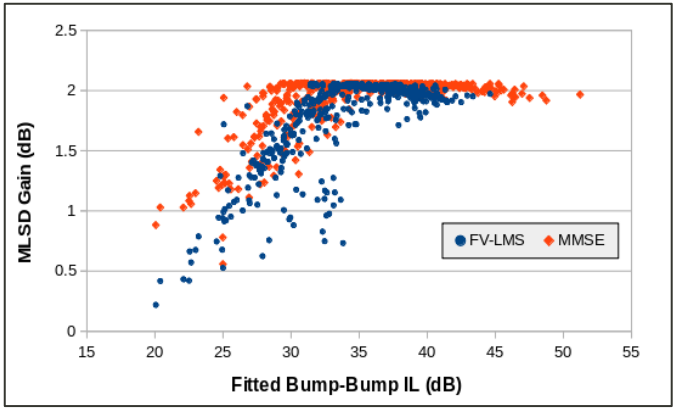


- **COM obviously splits into groups with host loss categories**
  - **Anticipation of very different requirements on reference parameters or spec values**
- **COM analysis and compliance validation shall be done for a subset of cases to enable flexible host architecture**

MLSE in COM: Test Results based on U0

- Adopted MLSE Equation U1.c in shakiba_3dj_01b_2401 slide 11 is WIP in COM
- Key debates on reliable MLSE improvement
  - Theoretic vs implementation gap
  - No implementation penalty to RxFFE in COM
  - MLSE gain is much less for reflection or crosstalk dominated channels
- Considerations of MLSE implementation penalty
  - Higher implementation penalty with increasing insertion loss is observed in real world conditions
  - Don't suggest using a constant MLSE gain or penalty for all channels





Summary

- **This presentation provided the initial look of link performance for 200G/lane electrical interfaces with the latest COM update**
  - **Further adjustment to reference parameters is required with the completed COM modeling and the incorporation of MLSE**
- **IL target for AUI C2M is expected to be >5dB less than CR & KR due to COM penalties associated with higher DER0 and eta_0**
- **Careful development of compliance definition is required for flexible link configurations**
  - **Further works on COM analysis and compliance validation to be completed**

Appendix

COM Configuration

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
PKG_NAME	PKG_LowR_CLASSA PKG_LowR_CLASSA		TX RX
A_v	0.413	V	
A_fe	0.413	V	
A_ne	0.45	V	
z_p select	[1 2]		
L	4		
M	32		
filter and Eq			
f_r	0.58	*fb	
c(0)	0.54		min
c(-1)	[-0.4:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	0		[min:step:max]
c(-4)	0		[min:step:max]
c(1)	0		[min:step:max]
N_b	1	UI	
b_max(1)	0.75		As/dffe1
b_max(2..N_b)	0		As/dfe2..N_b
b_min(1)	0		As/dffe1
b_min(2..N_b)	0	S	As/dfe2..N_b
g_DC	0	dB	[min:step:max]
f_z	42.5	GHz	
f_p1	42.5	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
Butterworth	1	logical	include in fr

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	0	logical
RESULT_DIR	.\results\CRKR_[date]\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	KR_set1_eval_	
COM_CONTRIBUTION	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	4000	logical
TDR_Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	0	
fixture delay time	[0 0]	
Tukey_Window	1	
Noise, jitter		UI
sigma_RJ	0.01	UI
A_DD	0.02	V^2/GHz
eta_0	6.00E-09	dB
SNR_TX	33	
R_LM	0.95	

new
relevent

Table 93A-3 parameters			
Parameter	**Setting**	**Units**	Information
package_tl_gamma0_a1_a2	[5e-4 0.00065 0.0003]		
package_tl_tau	0.006141	ns/mm	
package_Z_c	[92 92 ; 70 70; 80 80; 100 100]	Ohm	
z_p (TX)	[8 24 30 45 ; 1 1 1 1; 1 1 1 1 ; 0.5 0.5 0.5 0.5]	mm	[test cases to run]
z_p (NEXT)	[8 24 30 45 ; 1 1 1 1; 1 1 1 1 ; 0.5 0.5 0.5 0.5]	mm	[test cases]
z_p (FEXT)	[8 24 30 45 ; 1 1 1 1; 1 1 1 1 ; 0.5 0.5 0.5 0.5]	mm	[test cases]
z_p (RX)	[8 24 30 45 ; 1 1 1 1; 1 1 1 1 ; 0.5 0.5 0.5 0.5]	mm	[test cases]
C_p	[0.4e-4 0.4e-4]	nF	[test cases]
Operational			
ERL Pass threshold	10	dB	
COM Pass threshold	3	db	
DER_0	2.00E-04		
T_r	0.00400	ns	
FORCE_TR	1	logical	
PMD_type	C2C		
EW	1		
MLSE	0	logical	
ts_anchor	1		
sample_adjustment	[-16 16]		
Local Search	0		
Filter: Rx FFE			
ffe_pre_tap_len	5	UI	
ffe_post_tap_len	10	UI	
ffe_pre_tap1_max	1		
ffe_post_tap1_max	1		
ffe_tapn_max	1		
FFE_OPT_METHOD	MMSE		FV-LMS or MMSE
num_ui_RXFF_noise	4096		
Floating Tap Control			
N_bg	1	0 1 2 or 3 groups	
N_bf	4	taps per group	
N_f	60	UI span for floating taps	
bmaxg	1	max DFE value for floating taps	
B_float_RSS_MAX	1	rss tail tap limit	
N_tail_start	11	(UI) start of tail taps limit	

Thank you

Questions and Discussions