

Supporting contribution to comments regarding error ratio allocation in optical PMD clauses

Guangcan Mi

Huawei Technologies Co., Ltd

Introduction

- Error Ratio was newly defined for 200Gbps/lane PMDs
- Error Ratio of PMDs are measured with $\text{BER}_{\text{added}}$
- $\text{BER}_{\text{added}}$ serves as a proxy to introduce the worst case influence to error ratio from other parts/physical instantiations of the link, in most cases AUIs.
- Two universal values of $\text{BER}_{\text{added}}$ were introduced to the four IMDD optical PMD clauses, CL 180~183.

| 180.2 Error ratio allocation

A complete PHY is expected to meet the frame loss ratio specifications in 174A.5.

A PMD is expected to meet the block error ratio specifications in 174A.6, measured at a PMA, with $\text{BER}_{\text{added}}$ equal to 6.4×10^{-5} .

A PHY is expected to meet the block error ratio specifications in 174A.6, measured at the PCS, with $\text{BER}_{\text{added}}$ equal to 3.2×10^{-5} .

Error Ratio Allocation – referring to PMA

Current draft

180.2 Error ratio allocation

A complete PHY is expected to meet the frame loss ratio specifications in 174A.5.

A PMD is expected to meet the block error ratio specifications in 174A.6, measured at a PMA, with BER_{added} equal to 6.4×10^{-5} .

A PHY is expected to meet the block error ratio specifications in 174A.6, measured at the PCS, with BER_{added} equal to 3.2×10^{-5} .

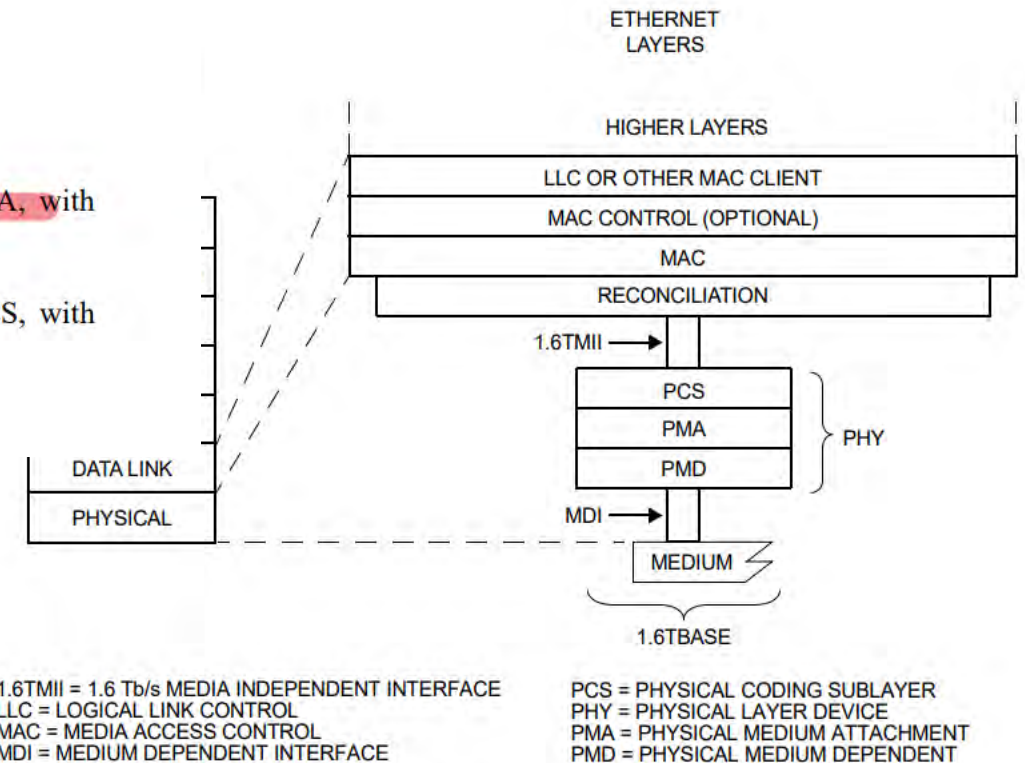


Figure 174-1—Architectural positioning of 1.6 Terabit Ethernet

Possible relative positions of PMA to PMD

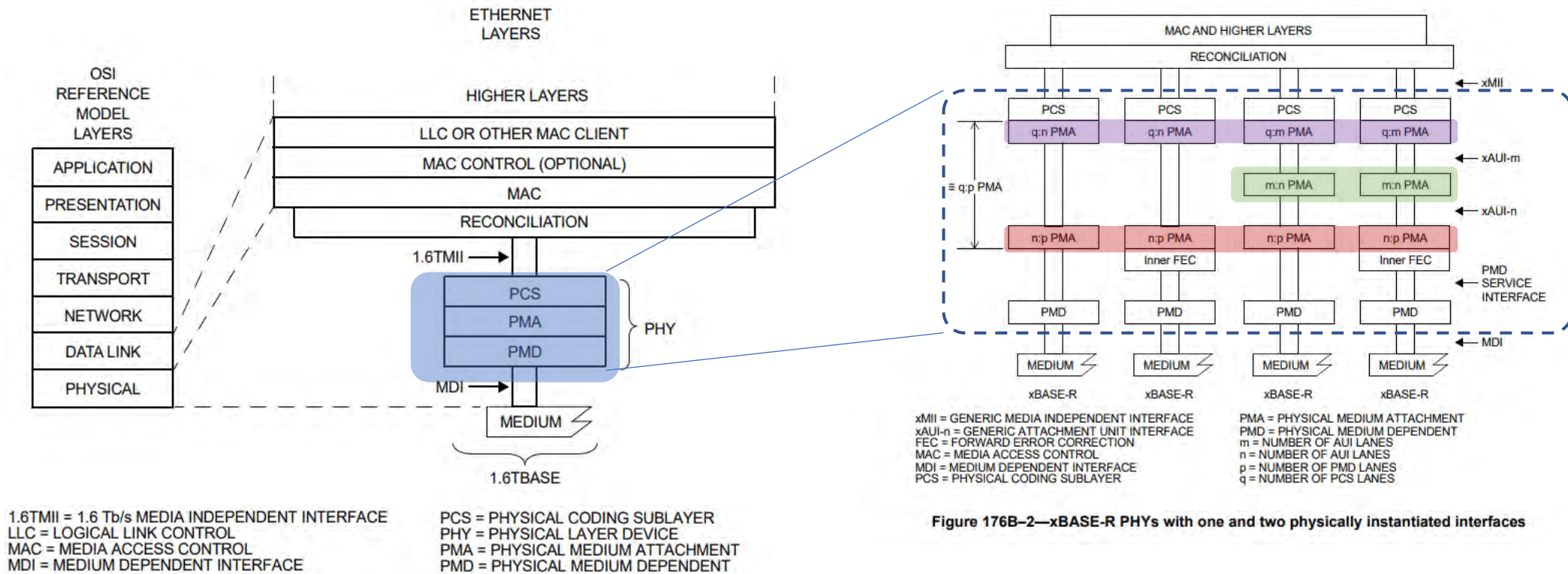


Figure 174-1—Architectural positioning of 1.6 Terabit Ethernet

Figure 176B-2—xBASE-R PHYs with one and two physically instantiated interfaces

1. Immediately before(transmit direction) and after(receive direction) PMD service interface (no AUI included) ← Error ratio
2. In between xAUI-n and xAUI-m (including only the AUI C2Ms)
3. Immediately after PCS (including all AUI interfaces that the data stream will pass)

Proposed change

180.2 Error ratio allocation

A complete PHY is expected to meet the frame loss ratio specifications in 174A.5.

A PMD is expected to meet the block error ratio specifications in 174A.6, **measured at a PMA**, with $\text{BER}_{\text{added}}$ equal to 6.4×10^{-5} .

A PHY is expected to meet the block error ratio specifications in 174A.6, measured at the PCS, with $\text{BER}_{\text{added}}$ equal to 3.2×10^{-5} .

Measured between the two PMAs immediately adjacent to the PMD in both the transmit and receive direction.

Referencing to Figure 176B-2 will be helpful too.

Two ways of $\text{BER}_{\text{added}}$ for optical PMDS

BER_{added} at PMA and PCS

180.2 Error ratio allocation

A complete PHY is expected to meet the frame loss ratio specifications in 174A.5.

A PMD is expected to meet the block error ratio specifications in 174A.6, measured at a PMA, with BER_{added} equal to 6.4×10^{-5} .

A PHY is expected to meet the block error ratio specifications in 174A.6, measured at the PCS, with BER_{added} equal to 3.2×10^{-5} .

Editor's note: A BER target based upon the required block error ratio for the purpose of TDECQ and other optical measurements is needed. Contributions on this subject are encouraged.

Table 174A-1—Error ratio allocations for optical PHYs

Sublayer or interface	Frame loss ratio for entire PHY	Codeword error ratio for entire PHY	BER for entire PHY (BER _{total})	BER per sublayer in a PHY
xAUI-n C2C	6×10^{-11}	1.45×10^{-11}	2.92×10^{-4}	0.08×10^{-4}
xAUI-n C2M				0.24×10^{-4}
PMD-to-PMD				2.28×10^{-4}
xAUI-n C2M				0.24×10^{-4}
xAUI-n C2C				0.08×10^{-4}

PMA: BER_{added} = xAUI-n C2C + xAUI-n C2M + xAUI-n C2M + xAUI-n C2C ← Clarified with the previous section

PCS: BER_{added} = xAUI-n C2C + xAUI-n C2M ← Guessed from the number

Possibilities of Error ratio measured at PCS

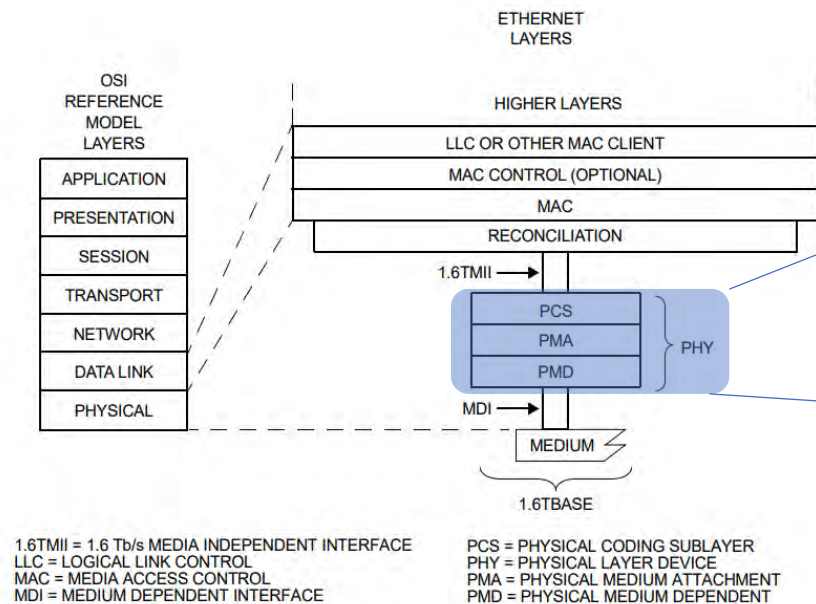


Figure 174-1—Architectural positioning of 1.6 Terabit Ethernet

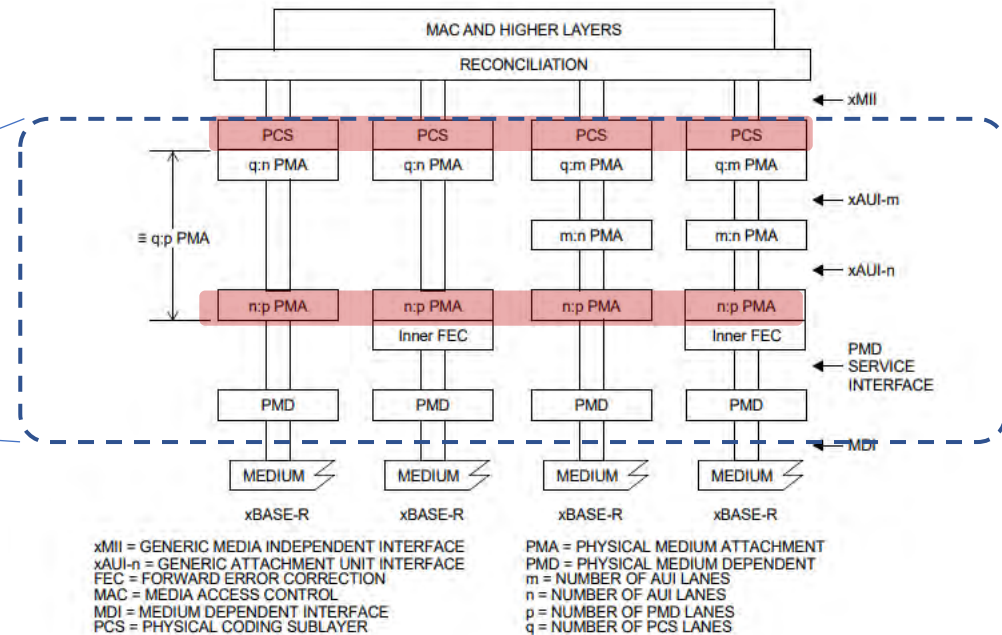


Figure 176B-2—xBASE-R PHYs with one and two physically instantiated interfaces

Error Ratio considered at PCS is measured with contribution of AUIs, with two possible variations on where transmit starts:

Clarification?

Scrambled Idle transmitted from	AUI instantiation passed when Received at PCS
PMA immediately above the PMD service interface	Max. 2 AUI instantiation, depending on test fixtures.
PCS	Max. 4 AUI instantiation. Depending on test fixtures.

Influencing the result

- **Inconsistency, subject to hardware:** Switch testbed/BERT that will be used for module validation could have different implementation of electrical channel/AUI.
- **Optimistic:** Count in the error ratio contribution of AUI implemented in the test fixture, though the physical implementation of AUI interface(s) may not observe the worst case contribution to error ratio, i.e., BER_{added}
- **Pessimistic:** It is also possible to disregard the error ratio contribution of any AUI that may have been incorporated in the measurement setup, but does put a more stringent requirement on the PMD.

For the task force's consideration and discuss

Author's view: pessimistic option may be the easier choice to unify all variations of test fixture and equipments.

Summary

- Clarification in the draft is suggested regarding error ratio allocation for IMDD optical PMDs.

Back up

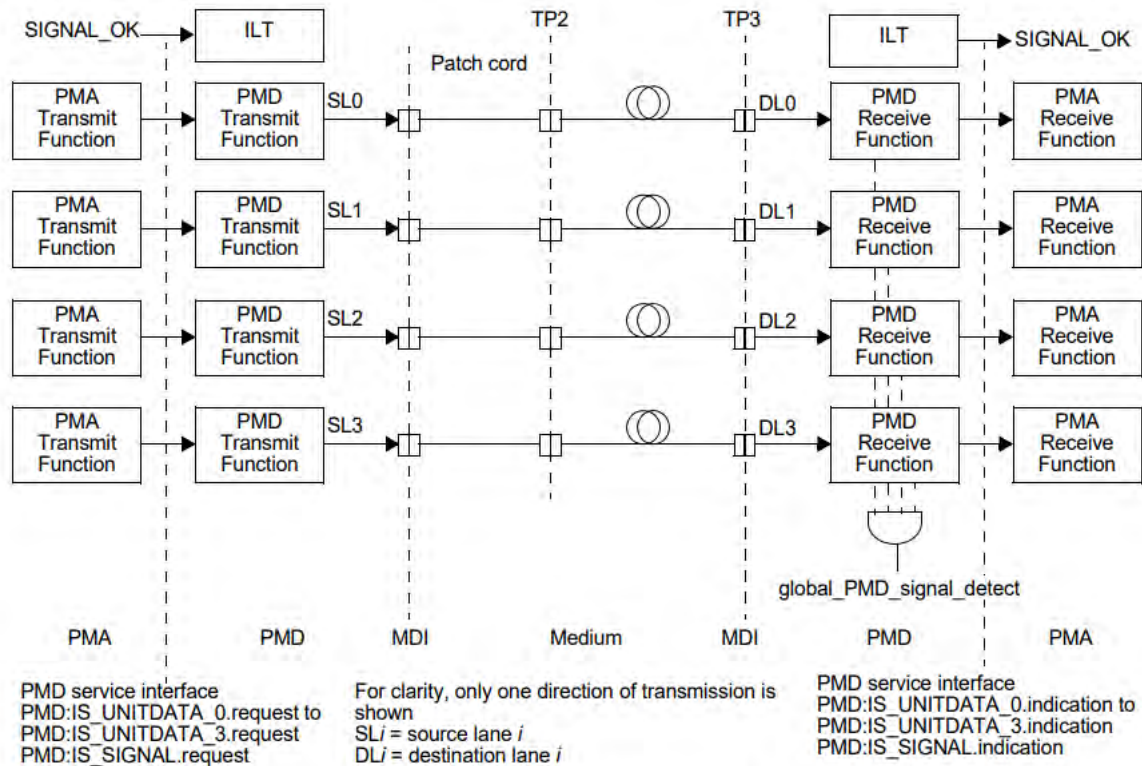
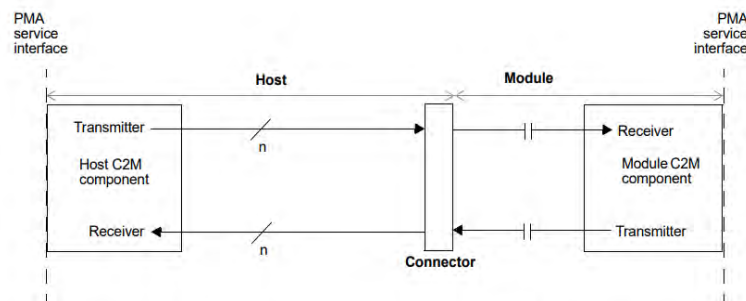
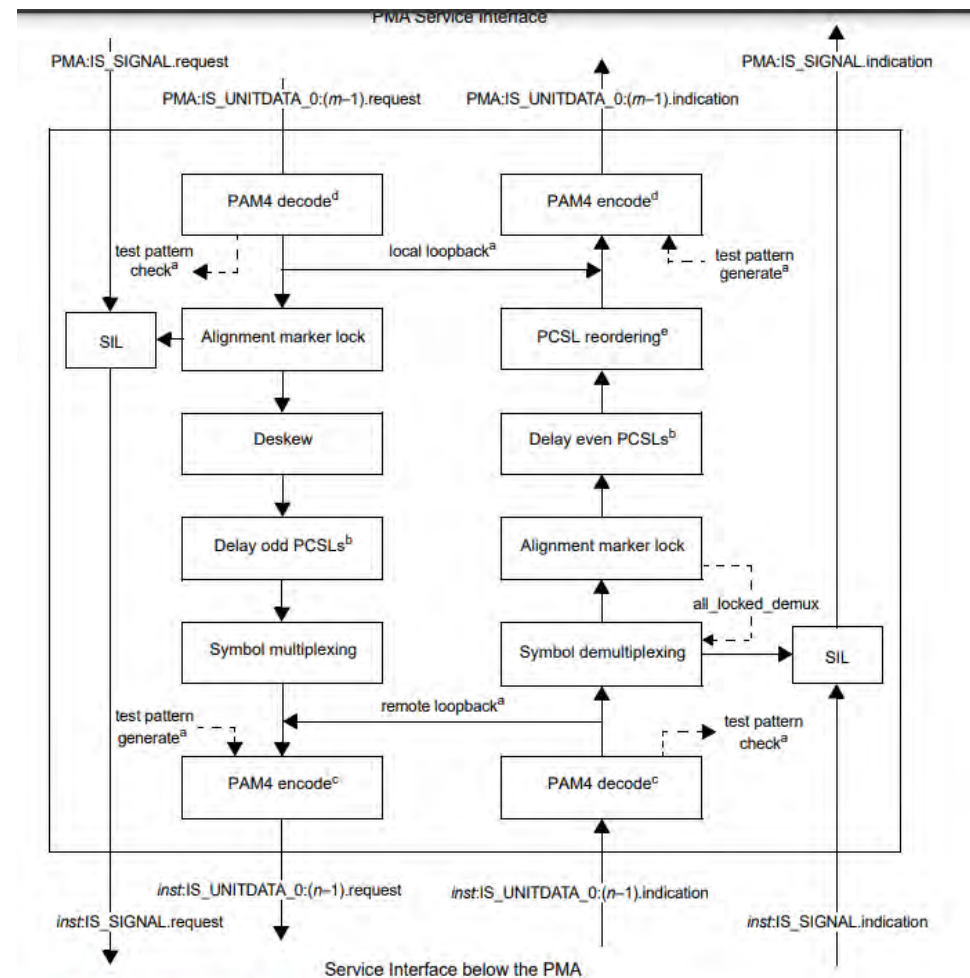


Figure 180-2—Block diagram for 800GBASE-DR4 transmit/receive paths



NOTE—The number of lanes *n* is 1 for 200GAUI-1, 2 for 400GAUI-2, 4 for 800 GAUI-4, and 8 for 1.6TAUI-8.

Figure 176D-2—Components of a 200 Gb/s per lane AUI-C2M



inst: PMA or PMD or FEC or AUI
SIL: Signal indication logic

- ^a Optional
- ^b If 200GBASE-R, 400GBASE-R or 800GBASE-R
- ^c If the sublayer below the PMA is an AUI or PMD
- ^d If the sublayer above the PMA is a 1.6TAUI-16
- ^e If the sublayer above the PMA is an 800GBASE-R BM-PMA

m = 8 (200GBASE-R), 16 (400GBASE-R), 32 (800GBASE-R), or 16 (1.6TBASE-R)
n = 1 (200GBASE-R), 2 (400GBASE-R), 4 (800GBASE-R), or 8 (1.6TBASE-R)

Figure 176-2—200GBASE-R 8:1, 400GBASE-R 16:2, 800GBASE-R 32:4, 1.6TBASE-R 16:8 PMAs functional block diagram

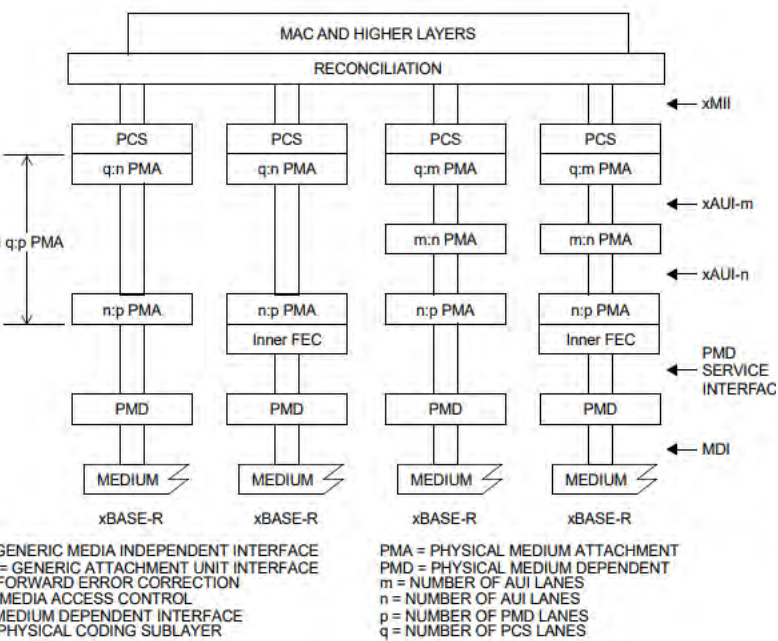


Figure 176B-2—xBASE-R PHYs with one and two physically instantiated interfaces

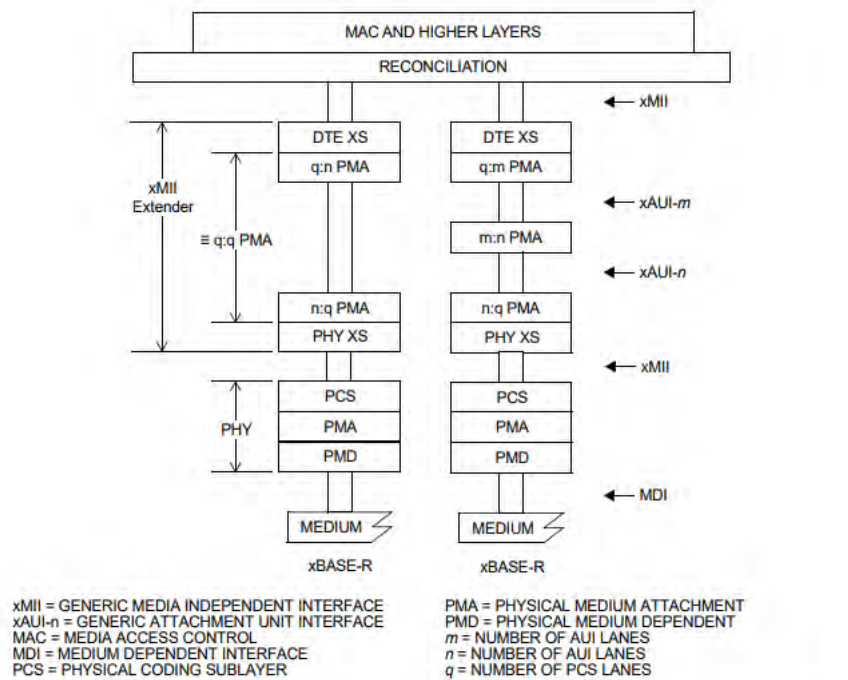


Figure 176B-3—xBASE Physical Layer implementations with an xMII Extender with one and two physically instantiated interfaces

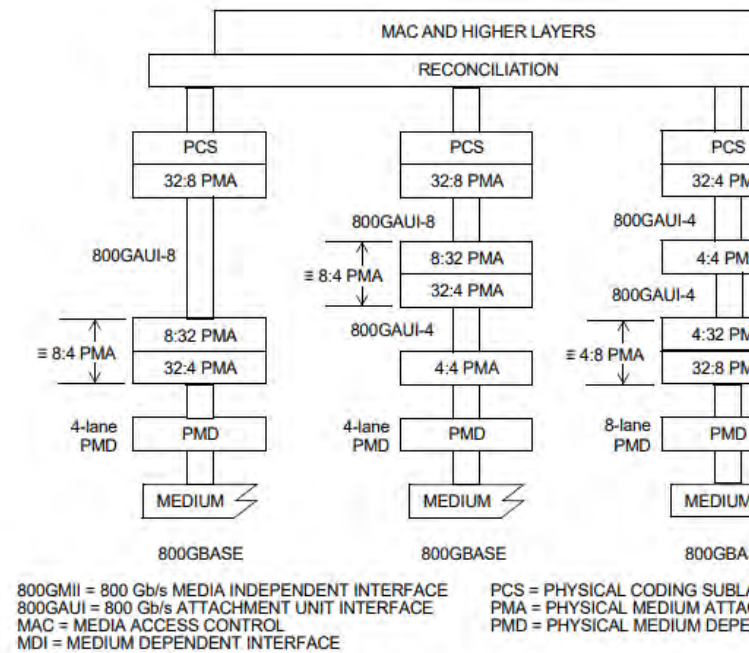


Figure 176B-4—800GBASE-R PHYs with back to back PMA