Revisiting MPI Penalty for Optical PMDs

Ali Ghiasi - Ghiasi Quantum/Marvell

IEEE 802.3dj Meeting
New Orleans

May 10, 2025

Supporters

- John Johnson – Broadcom
- Gary Nicoll – Cisco
- Vipul Bhatt – Coherent
- Chris Cole – Coherent
- Haifeng Liu – HG Genuine
- Mike Dudek – Marvell
- Mark Kimber – Semtech.

Overview

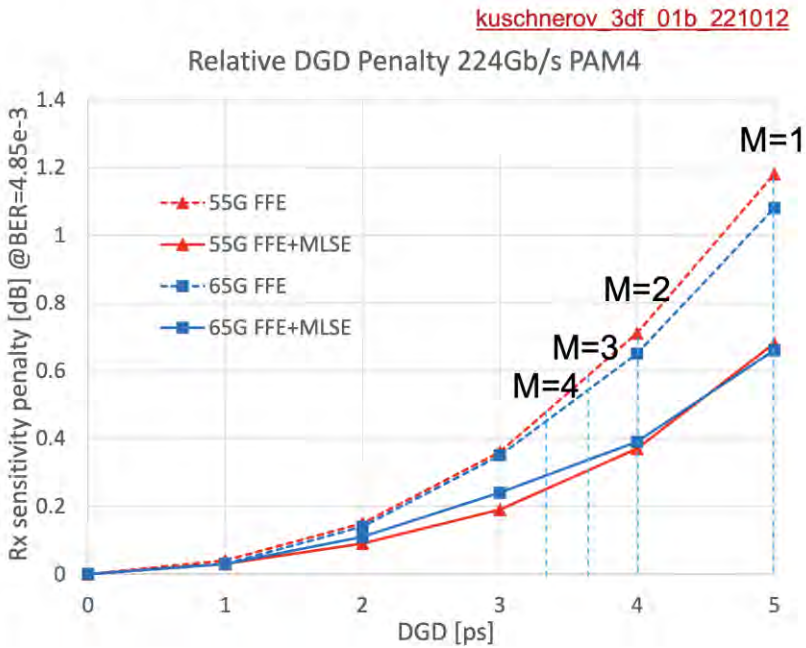
- Background on DGD penalty
- Background on MPI penalties
- Correcting MPI spreadsheet for PAM4
- Revisiting cable plants
- Underlaying MPI assumptions
- Few MPI analysis
- Summary.

DGD Penalty for Clauses 180-183

- **kuschnerov_3dj_optx_01_230829 show worst case DGD penalty of 0.7 dB for clause 183 800GBASE-LR4 PMD for max DGD of 4 ps**
  - 800GBASE-FR4 with max DGD of 2.3 ps has ~0.18 dB penalty
  - 800GBASE-FR4/DRx-2 with max DGD of 2.3 ps has ~0.18 dB penalty
  - 800GBASE-FR4-500/DRx with max DGD of 2.24 ps has ~0.18 dB penalty
- **For PMDs listing combined DGD/MPI penalty the MPI value should be added to the above values of DGDs.**

DGD penalty for varying number of segments M

- The original single segment (M=1) PMD penalty was based on a FFE+MLSE receiver (0.7dB)
- Assuming multiple segments, a linear equalizer would be sufficient to achieve acceptable performance
- Given the available data and pending further discussion by the industry M=4 seems to be a reasonable assumption
- M=4 can achieve a penalty of ≤0.5dB with an linear FFE equalizer

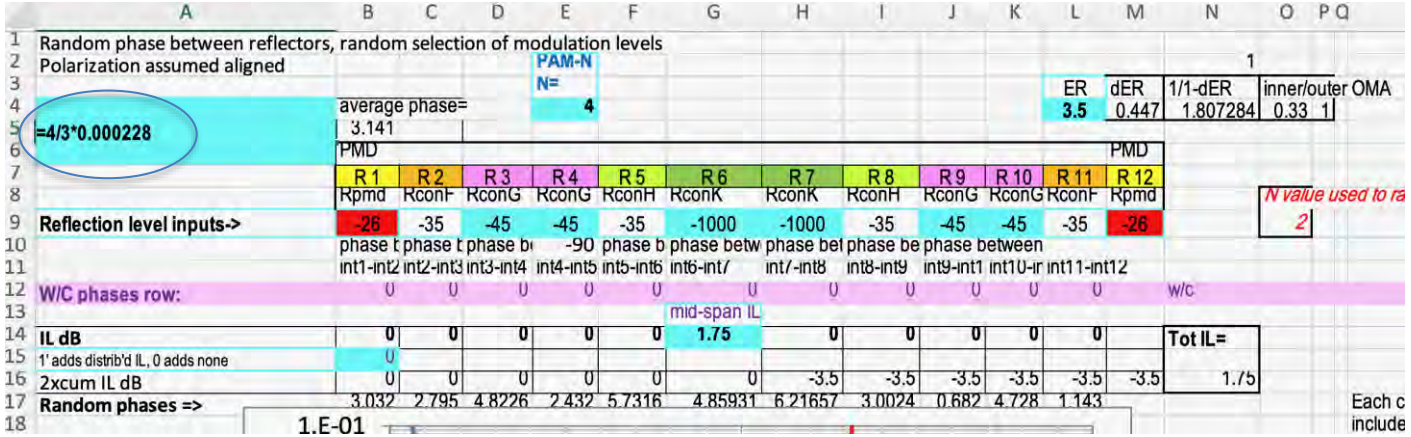


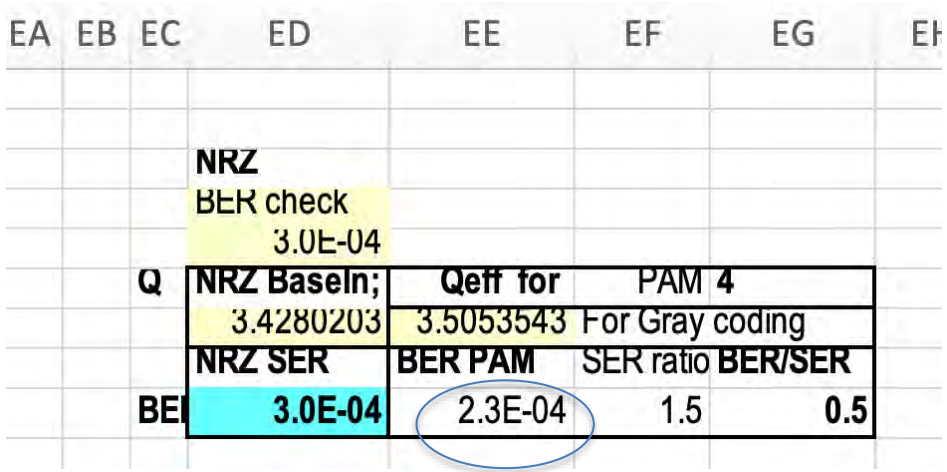
Revisiting the MPI/DGD Penalties

- **MPI penalty based on statistical model proposed by King_01a_01116_smf developed in 802.3bs has been adopted for MPI penalty estimation**
  - 802.3bs MPI analysis was based on assumption in liu_3bs_01a_0316
  - 802.3cd MPI analysis and how to reconcile PC and APC connectors penalties was based on traverso_3cd_01_0317
- **ghiasi_3dj_02_2501 raised concern regarding fixed allocation of MPI penalties**
  - 180.7.3 has allocation of 0.1 dB MPI/DGD penalty to support DR double links with 6 discrete reflectance at @-45 dB discrete reflectance channel IL=3 dB
  - 181.7.3 has allocation of 0.5 dB MPI/DGD penalty to support 800GBASE-FR4-500 double link with 4 discrete reflectance @-35 and 4 discrete reflectance @-45 dB channel IL=3.5 dB
  - 182.7.3 has allocation of 0.4 dB MPI/DGD penalty to support DR-2 double links with 4 discrete reflectance at @-35 dB and 4 discrete reflectance @-45 dB channel IL=4 dB
  - 183.7.3 has allocation of 0.4 dB MPI/DGD penalty to support 800GBASE-FR4 double-link with 4 MPO @-45 dB and 4 LC@-35 dB discrete reflectance and channel ILmax=4 dB
- **johnson_3dj_adhoc_01_250220 additional background on the history of MPI penalty and there may be good reason to revisit some of the underlaying assumptions**
- **Reconciling PC and APC MPI penalties is top priority for 802.3dj**
  - Its also time to revisit underlaying MPI assumptions which applies to all clauses.

Correcting Input BER for PAM4 in King Spreadsheet

- **The intention of J. King likely was to input NRZ BER into cell A5 but we have been inputting PAM4 BER into cell A5**
  - Cell E4 based on on PAMx converts the cell A5 NRZ BER into PAMx BER in cell EE(
  - To use J. King spreadsheet for PAM4 convert the PAM4 BER to NRZ BER by x4/3, see below.

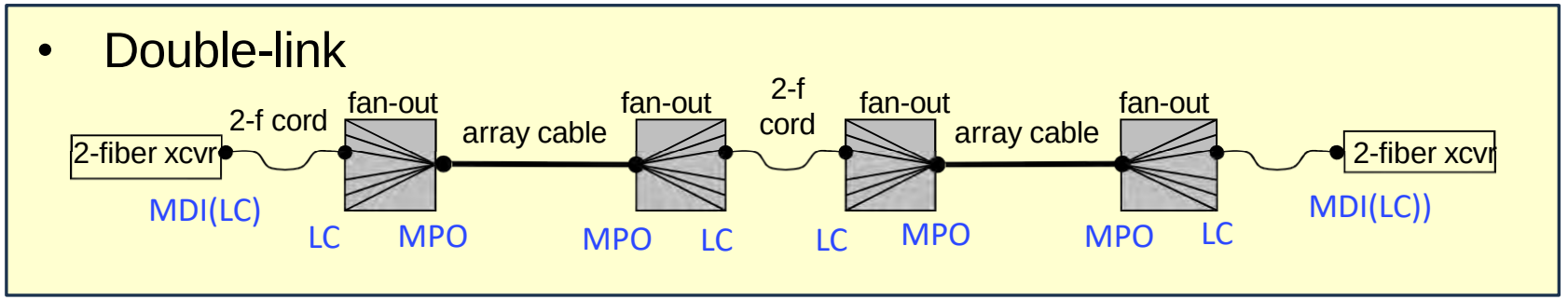




Cable Plants

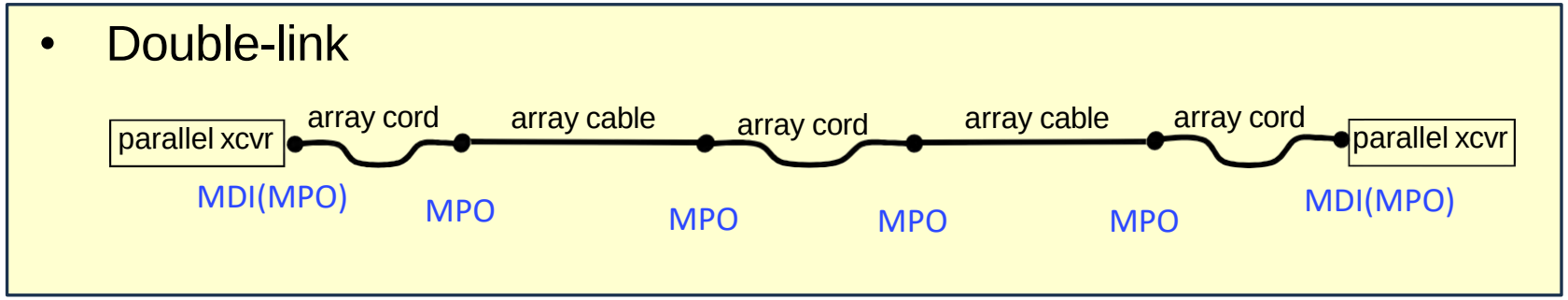
- **Cable plant model per kolesar_3bs_01_0514 double and triple link and nicholl_3bs_01a_0316 for MPI calculations**
  - Are these acceptable cable plant assumptions for 802.3dj optical PMDs?

200GBASE-DR
200GBASE-DR-2
800GBASE-FR4-500
800GBASE-FR4



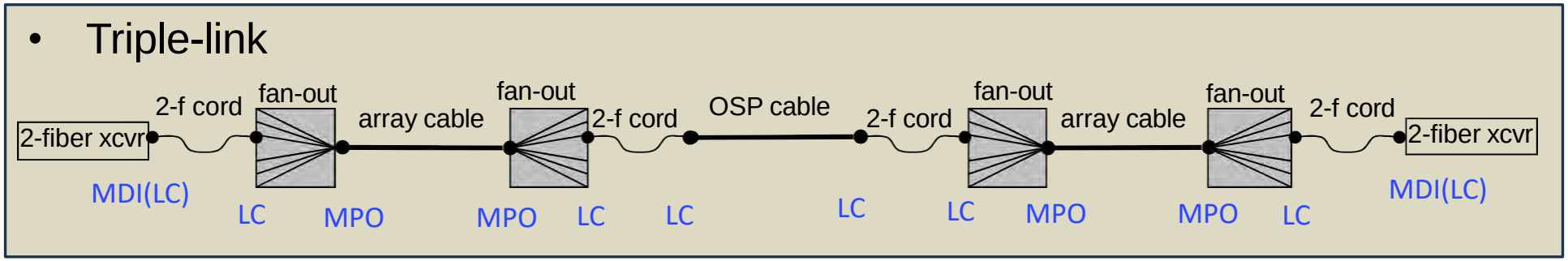
6 LC
+ 4 MPOs

400GBASE-DR2
400GBASE-DR2-2
800GBASE-DR4
800GBASE-DR2-4
1.6TGBASE-DR8
1.6TGBASE-DR8-2



6 MPO

800GBASE-LR4



8 LC
+ 4 MPO

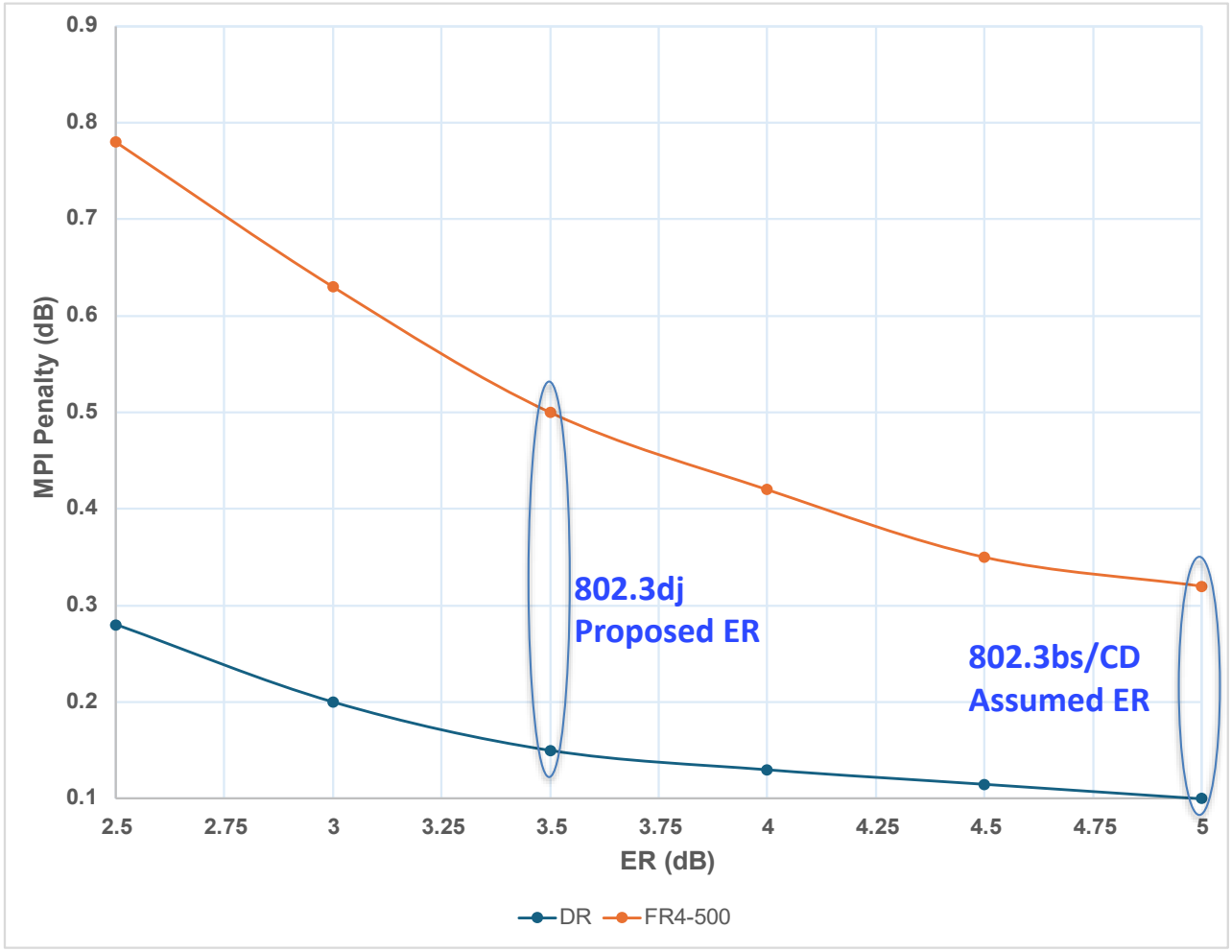
Underlaying MPI Penalty Assumptions

- **Underlaying assumptions in the 802.3bs/cd**
  - Cable plant follow double or triple link model
  - Max loss at the end of cable plant
  - BER inadvertently end up to be 4/3*2.4E-4
  - LC reflectance -35 dB
  - MPO reflectance -45 dB
  - ER=5 dB
  - BER 2E-4
  - MPI penalty extrapolated to 1E-6

- **Proposed assumptions for 802.3dj**
  - Cable plant follow double or triple link model
  - Placing 1/2 of the loss in middle of cable
  - LC reflectance -35 dB
  - MPO reflectance -45 dB
  - ER=3.5 dB (min allowed) to better support 200G SiP
  - BER 2.28E-4 for CL180 and 182, BER 4.8E-3 for CL182 and 183
  - MPI penalty extrapolation for now keep at 1E-6 but when cross-penalty due to TDECQ eye-clousure is included then penalty extrapolation can be redcued to 1E-5 based on improved SMF channel model as in rodes_3dj_01a_2401.

MPI Penalty as Function of ER

- **CL 180 DR and CL 181 FR4-500 MPI penalty as function of ER for double llink configurations as on page 7**
  - MPI penalties for extinction ratio from 5.0 dB to 2.5 dB based on the input that 200G SiP MZM typically operate closer to 3.5 dB
    - Original analysis in 802.3bs liu_3bs_01a_0316 assumed ER of 5 dB with the full channel IL at TP3 input
    - This analysis assumes ½ of loss placed at mid-span
    - Slight MPI penalty increase due to lower channel loss is offsetted by correcting PAM4 BER in King Spreadsheet.



Best Method to Reconcile MPI Penalty for Mixed MPO/LC PMDs

- **traverso_3cd_01_0317 proposed method can reconcile MPI penalty in mixed mode PMDs such as for 200GBASE-DR and 00GBASE-DR-2**
  - Row 0 with 0 >-45 dB and ≤-35 dB reflectance is the MPI for double link MPO cable plant
  - Row 0 with 0 >-45 dB and ≤-35 dB reflectance is used for MPI allocation of double link LC cable plant but cable plant loss are reduced with additional number of discrete reflectance's (LC) >-45 and ≤-35 dB
- **Extending clause 180 DR MPI-loss trade off can be applied to DR-2, FR4-500, FR4, and LR4 as suggested Johnson_3dj_01_2505.**

MPI Penalty Calculation Table from Traverso

MPI Penalty (dB)		Number of discrete reflectances > -55 dB and ≤ -45 dB								
		0	1	2	3	4	5	6	7	8
Number of discrete reflectances > -45 dB and ≤ -35 dB	0	0	0.02	0.03	0.04	0.05	0.06	0.07	0.08	0.10
	1	0.05	0.06	0.05	0.09	0.11	0.12	0.11	0.15	0.12
	2	0.1	0.12	0.13	0.16	0.19	0.2	0.22	0.23	0.22
	3	0.18	0.18	0.2	0.2	0.24	0.3	0.3	0.32	*
	4	0.26	0.27	0.32	0.34	0.36	0.4	0.41	*	*
	5	0.32	0.33	0.38	0.4	0.44	0.48	*	*	*
	6	0.45	0.48	0.51	0.54	0.57	*	*	*	*

x.yz = these values exceed the proposed MPI penalty limit – see slide 3

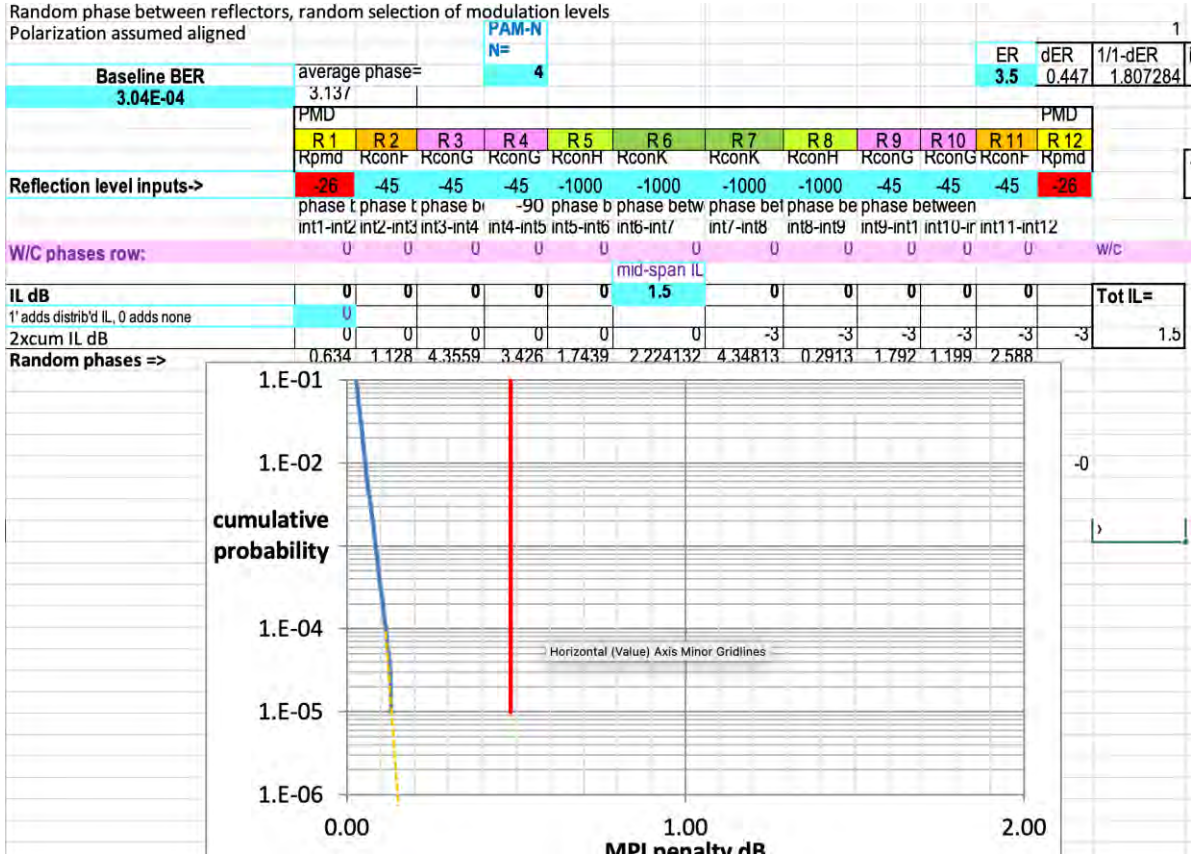
Table 180–12—Maximum channel insertion loss versus number of discrete reflectances

Maximum channel insertion loss (dB)		Number of discrete reflectances > –55 dB and ≤ –45 dB								
		0	1	2	3	4	5	6	7	8
Number of discrete reflectances > –45 dB and ≤ –35 dB	0	3	3	3	3	3	3	3	3	3
	1	3	3	3	3	3	3	3	3	3
	2	3	3	3	2.9	2.9	2.9	2.9	2.9	2.9
	3	2.9	2.9	2.9	2.9	2.9	2.8	2.8	2.8	—[a]
	4	2.8	2.8	2.8	2.8	2.7	2.7	2.7	—[a]	—[a]
	5	2.8	2.8	2.7	2.7	2.7	2.6	—[a]	—[a]	—[a]
	6	2.6	2.6	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]

[a] The indicated combination of reflectances does not provide a supported maximum channel insertion loss.

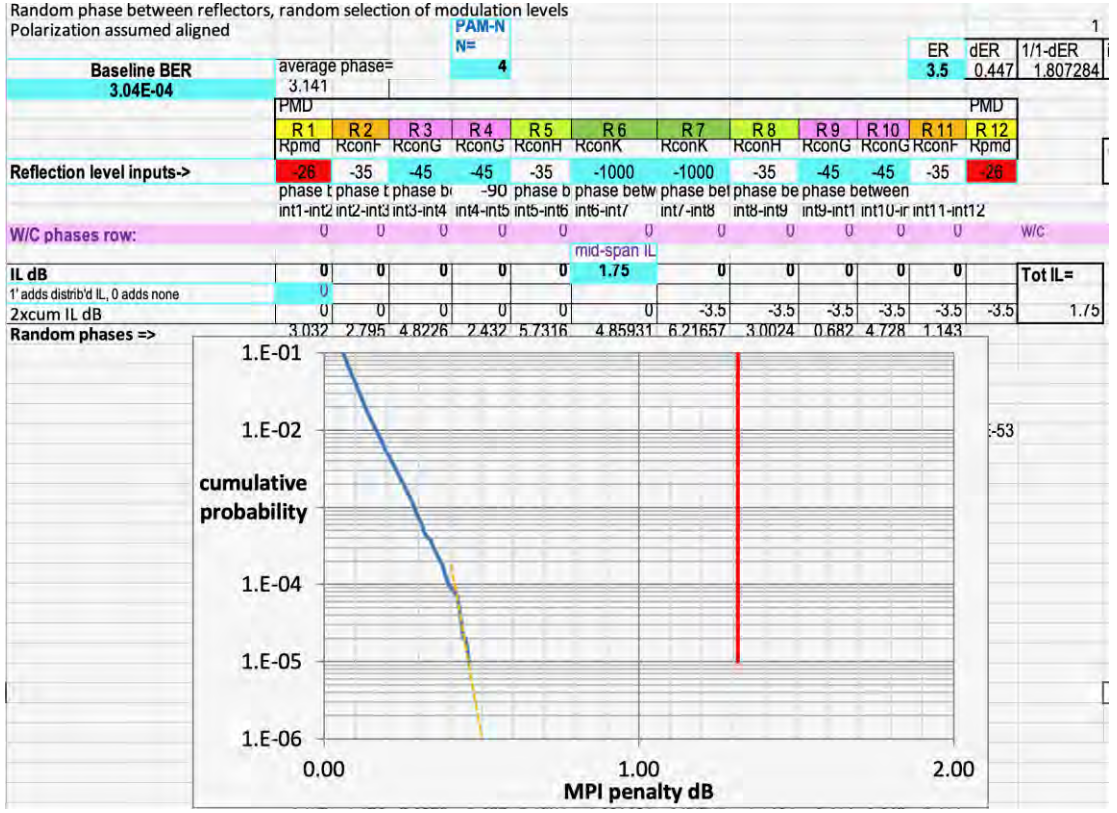
Clause 180 DR Link MPI Penalty

- **Double link with 6 MPO connectors**
  - MPI penalty is ~0.15 dB at confidence 1E-6 after correcting for PAM4 BER and placing half the loss in the middle of the link.



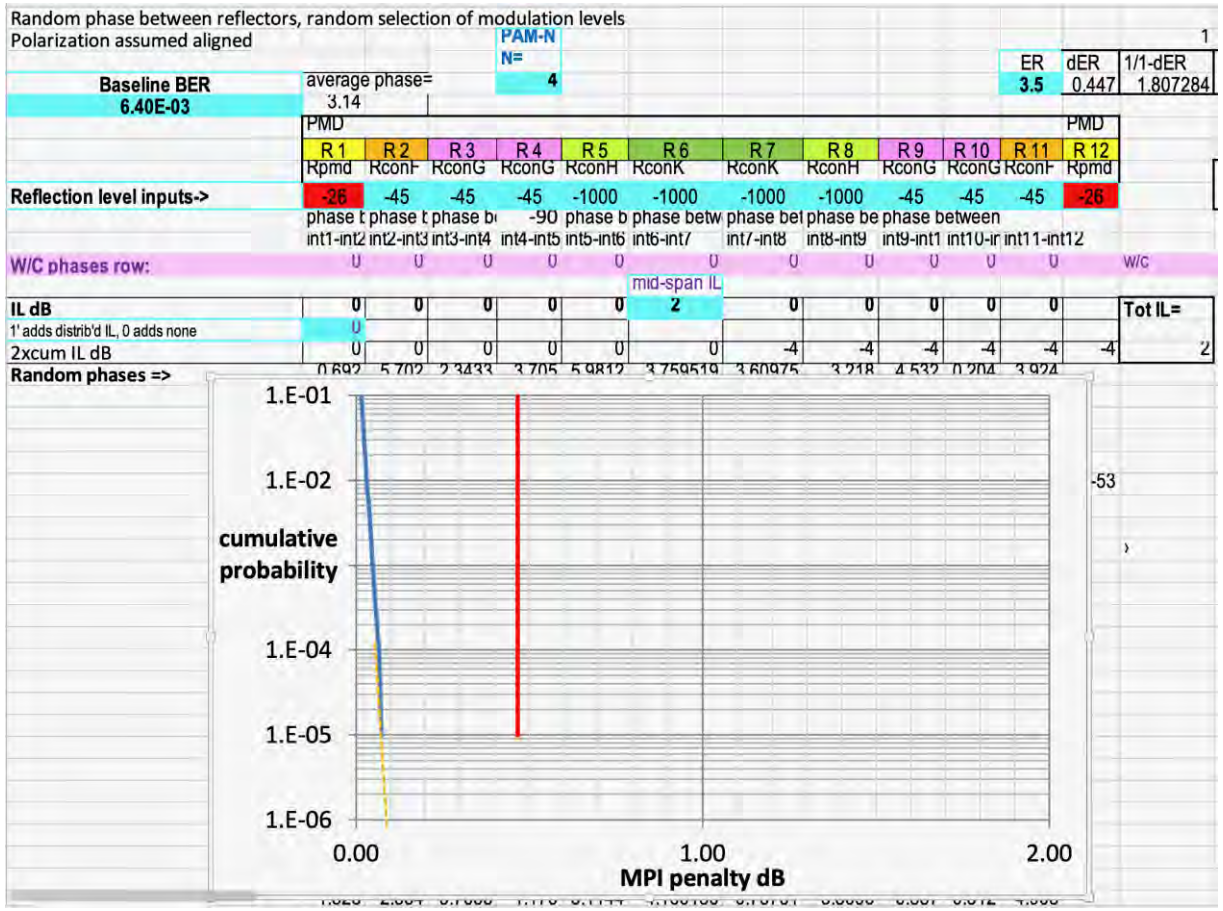
Clause 181 FR4-500 Link MPI Penalty

- **Double link with 4 LC and 4 MPO**
  - MPI penalty is ~0.5 dB at confidence 1E-6 after correcting for PAM4 BER and placing half the loss in the middle of the link.



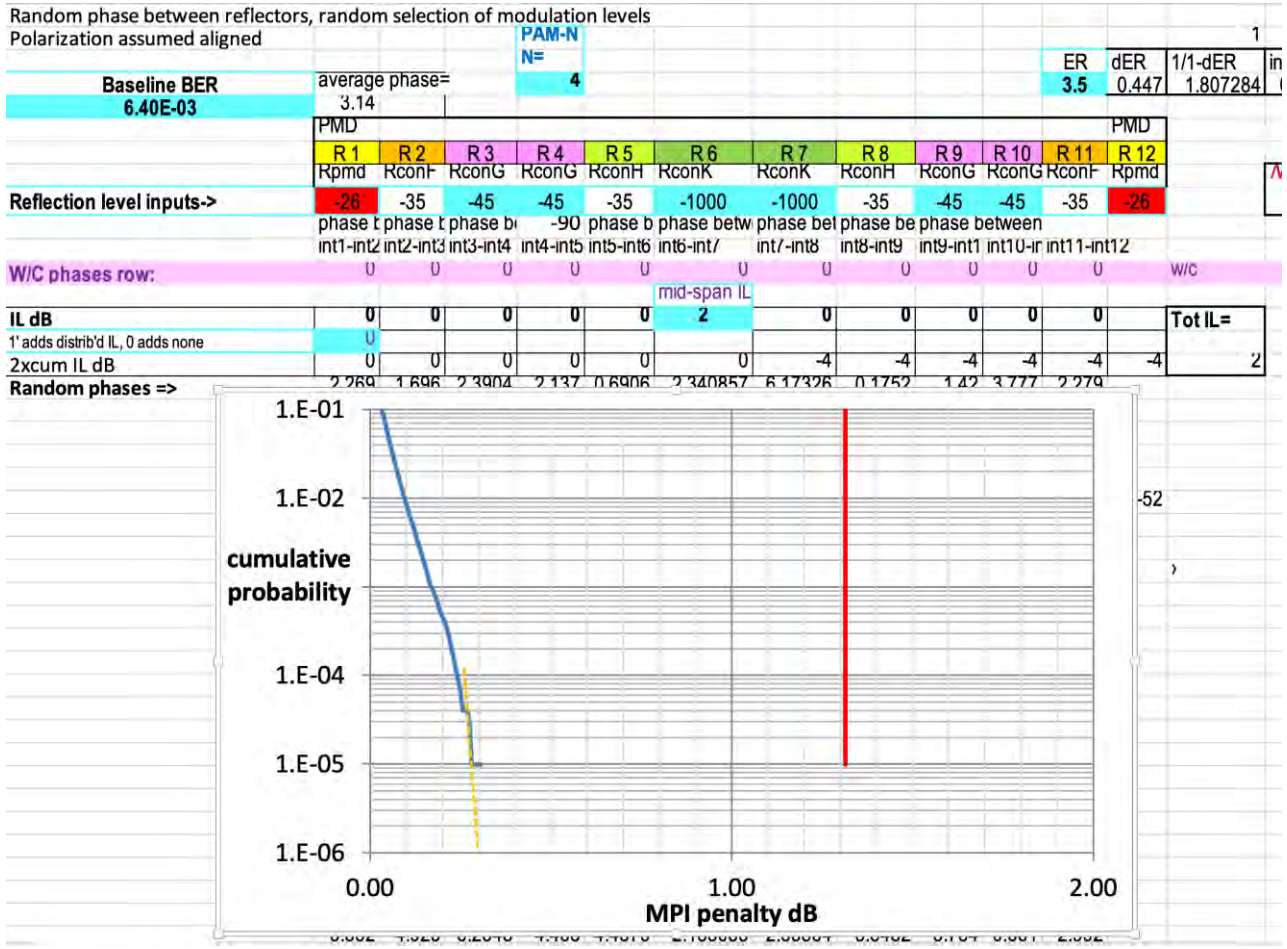
Clause 182 DR-2 MPI Penalty

- **Double link with 4 LC and 4 MPO**
  - MPI penalty is ~0.09 dB at confidence 1E-6 after correcting for PAM4 BER and placing half the loss in the middle of the link.



Clause 183 FR4 MPI Penalty

- **For Double link 4 LC and 4 MPO connectors**
  - MPI penalty is ~0.3 dB at confidence 1E-6 after correcting for PAM4 BER and placing half the loss in the middle of the link.



Summary of MPI/DGD Penalties

- **MPI/DGD penalty must be sufficient to support expected double or triple link configuration.**

Clause	PMD	MPI Penalty DJ D1.5	DGD Penalty DJ D1.5	MPI Penalty Calculation	DGD Penalty Estimate	Proposed MPI Penalty	Propsoed DGD Penalty
180	DR	0.1 dB*		0.15 dB	0.18 dB	0.33 dB*	
181	FR4-500	0.5 dB*		0.5 dB	0.18 dB	0.68 dB*	
182	DR-2	0.4 dB*		0.09 dB	0.18 dB	0.27 dB*	
183	FR4	0.5 dB*		0.3 dB	0.18 dB	0.48 dB*	
183	LR4	0.4 dB	0.7 dB	0.4 dB	0.7 dB	NC	NC
* These PMDs have combined MPI/DGD penalties							

Summary

- **The MPI/DGD penalties must be sufficient to support the underlying double or tipple link configurations**
  - Current combined MPI+DGD penalties of 0.1 dB for CL180 PMDs is insufficient to support double link with 6 MPOs
  - Current combined MPI+DGD penalties of 0.1 dB for CL181 PMDs is insufficient to support double link with 4 MPOs and 4 LCs
  - Current combined MPI+DGD penalties of 0.4 dB for CL182 PMDs is 0.13 dB excess allocation to support double link with 6 MPOs
  - Current combined MPI+DGD penalties of 0.5 dB for CL183 800GBASE-FR4 PMDs is about the right allocation to support double link with 4 MPOs and 4 LCs
  - Current combined MPI+DGD penalties of 0.4/0.7 dB for CL183 800GBASE-LR4 PMDs is about the right allocation to support triple configuration with 6 LC and 4 MPOs
- **Trading off MPI penalty vs channel IL as in Table 180-12 allow supporting greater set of channel configuration but the MPI/DGD penalty must be sufficient to support the basic link configuration**
- **Current MPI penalty doesn't account cross-penalty where low transition (low ISI) reflected pulse interfere with high transition (high ISI TDECQ ~ 3 dB)**
  - In worst case the MPI penalty may double – such even frequency would be low and data dependent
  - This needs more study as doubling MPI penalty would be excessive and costly!

Thank You!