Updated test vectors for 177A

Comment #294, #453

Xiang He, Xuebo Wang

Huawei

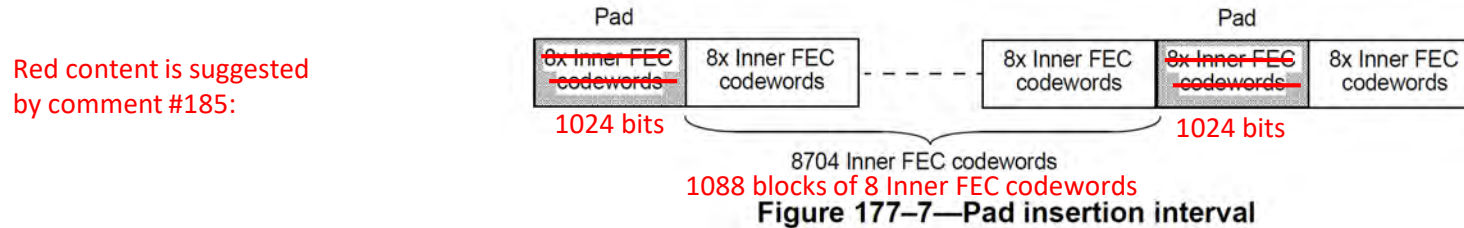# Background

- Test vectors for Clause 177 Inner FEC was added in D1.0 (see levy_3dj_01b_2401.pdf).

- PRBS13 scrambler was added to pad bits in D1.2, to prevent degradation of the transmitted signal (comment #471 against D1.1 by Matt).

- The test vectors need to be updated after the scrambler is added.
  - Comment # 294 and 453.

CI **177A**	SC **177A**		P **765**	L **21**	# 294

Brown, Matt — Alphawave Semi

Comment Type **TR** — *Comment Status* **D** — (Logic) Test vector

The referenced test vectors do not include scrambling of pad bits as specified in 177.4.7.2 as the requirement scrambling was added in a later draft.

SuggestedRemedy

Provide a new test vector set which includes scrambling of the pad bits.

Proposed Response — *Response Status* **W**

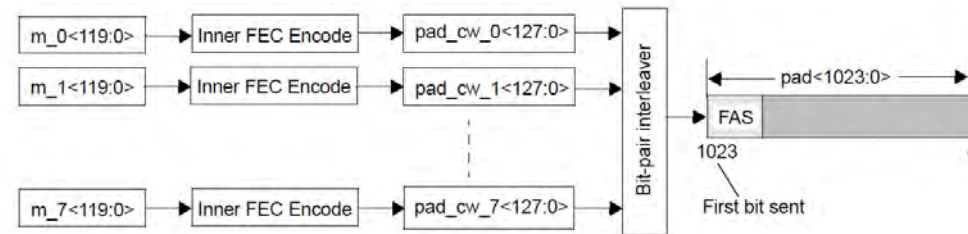PROPOSED ACCEPT IN PRINCIPLE.
Resolve using the response to comment #453.

CI **177A**	SC **177A**		P **765**	L **1**	# 453

He, Xiang — Huawei

Comment Type **TR** — *Comment Status* **D** — (Logic) Test vector

The test vectors have not been updated since scrambler was added to the padding bits. Annex 177A should be updated to reflect the change.

SuggestedRemedy

A presentation with zipped files will be provided.

Proposed Response — *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
Pending review of the following presentation and CRG discussion.
<URL>/he_x_3dj_01_2507.pdf.

Pad structure revisit

- Each pad is 1024-bit long, and is inserted once every 8704 Inner FEC codewords.

Red content is suggested by comment #185:

Figure 177–7—Pad insertion interval

- The 1024-bit pad is consist of 8 (128,120) Inner FEC codewords, and bit-pair interleaved just like the normal payload to share the unified processing on Tx and Rx.
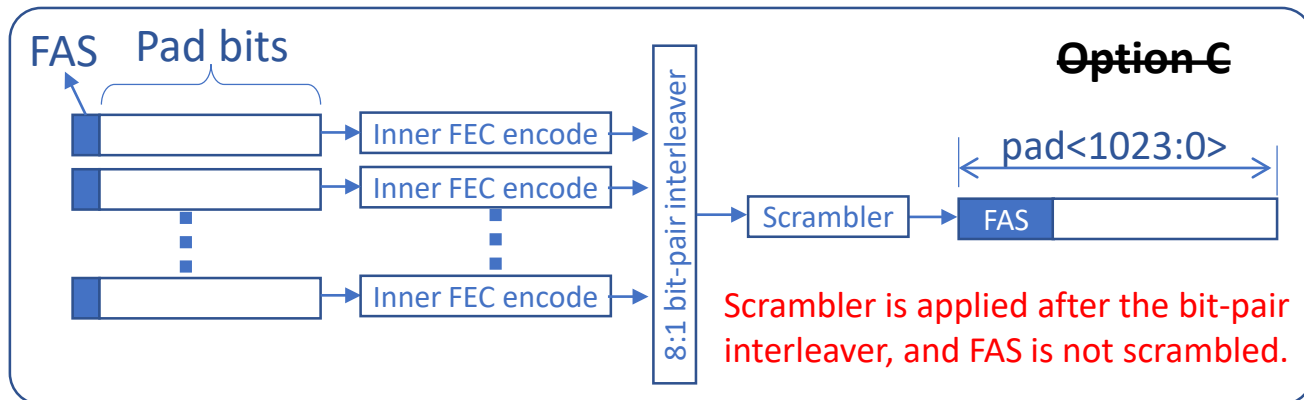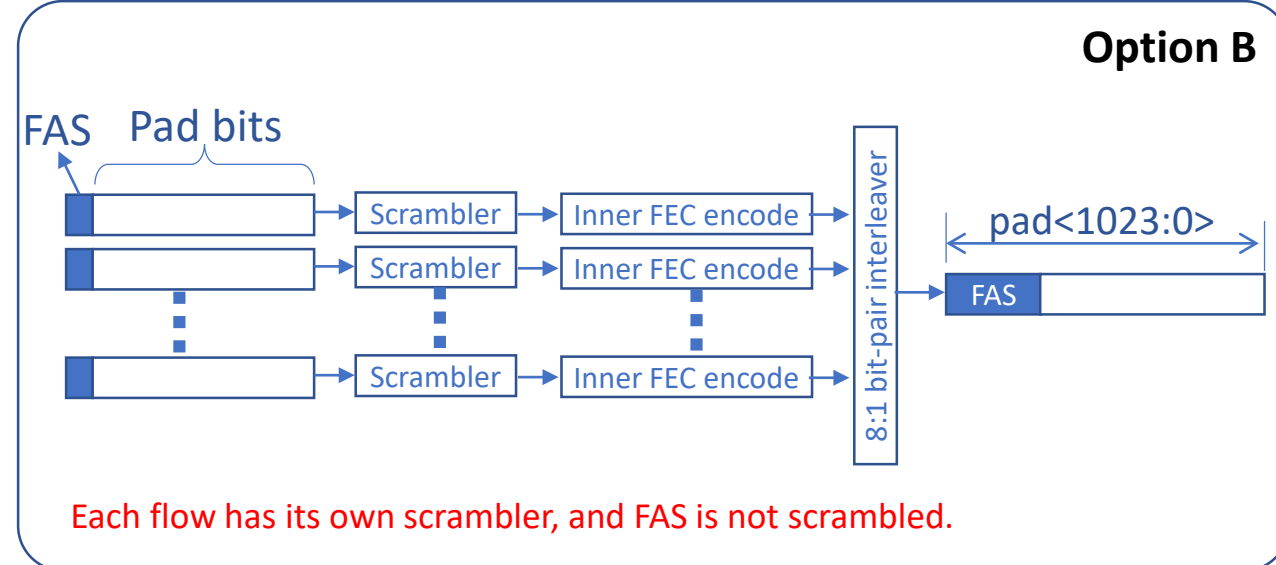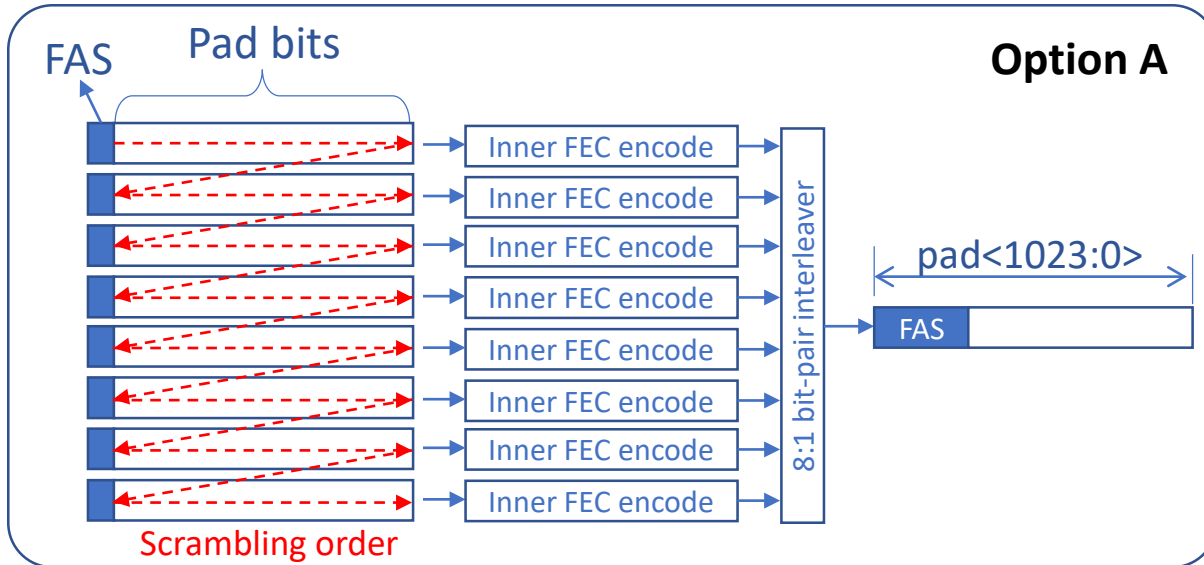

Figure 177–8—Pad codewords mapping

- Within each of the 8 "pad codewords", there are 6 bits of FAS, 114 pad bits, and 8 bits parity. The pad bits are scrambled with a PRBS13 self-synchronizing scrambler.

Table 177–5—Pad format

	Pad frame alignment sequence pad_cw_i<127:122>, m_i<119:114>	Pad bits, pad_cw_i<121:8>, m_i<113:0>	Parity pad_cw_i<7:0> p_i<7:0>
pad_cw_0	01 01 10	See 177.4.7.2	Calculated based on pad_cw_0<127:8>

Misunderstandings on the scrambler

- During discussion how the vectors are generated, we found there were three understandings on how the scrambler is done among different individuals.

Option A: Scrambling order

Option B: Each flow has its own scrambler, and FAS is not scrambled.

~~Option C~~: Scrambler is applied after the bit-pair interleaver, and FAS is not scrambled.

- Option C is wrong because pad is not following the same process as normal data (payload).

- Both option A and B can serve the purpose.
  - Option A was the original idea when PRBS13 was proposed, and a match has been confirmed by Nir Levy.
  - Option B is more intuitive and easier to implement.

Updated test vectors

- Text files can be found at: https://www.ieee802.org/3/dj/public/25_07/he_x_3dj_xxx_2507.7z
    - It was generated using option A in slide 4.
- The test points are following the same definition as in D2.0.
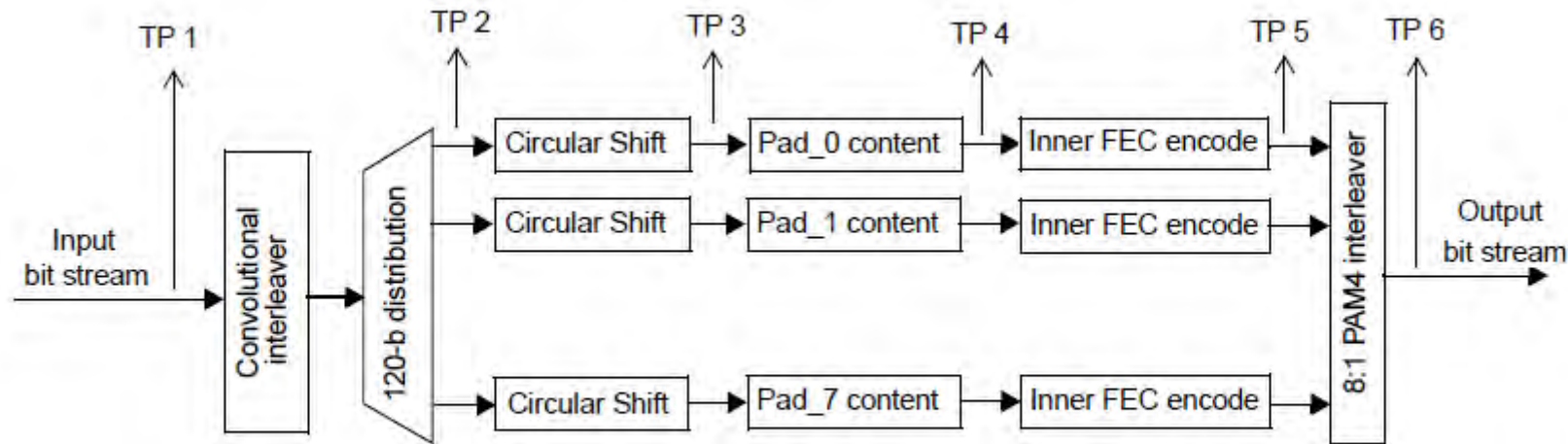- Depending on how comment #110 is resolved, TP4 and TP5 may be removed.

Figure 177A–1—Test points for test vectors

Thank you!

IEEE P802.3dj Task Force