Regarding using block error ratio as performance metric

Related Comments: 394, 395,396, 401,404,411

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Pre-requiste: per lane methodology

181.9.12 Receiver sensitivity

The receiver sensitivity (OMA_{outer}) of each lane shall be within the limits given in Table 181–6 if measured using a test pattern specified for receiver sensitivity in Table 181–12.

180.9.12 Receiver sensitivity

The receiver sensitivity (OMA_{outer}) of each lane shall be within the limits given in Table 180–8 if measured using a test pattern for receiver sensitivity in Table 180–14. The conformance test signal at TP3 meets the requirements for a transmitter followed by an attenuator.

167.8.2 Multi-lane testing considerations

Receiver sensitivity and stressed receiver sensitivity are defined for an interface at the BER specified in 167.1.1. The interface BER is the average of the BERs of the receive lanes when they are stressed. Measurements with Pattern 3 (PRBS31Q) allow lane-by-lane BER measurements. Measurement with Pattern 5 (scrambled idle encoded by RS-FEC) gives the interface BER if all lanes are stressed at the same time.

If each lane is stressed in turn, the BER is diluted by the unstressed lanes, and the BER for that stressed lane alone is found, e.g., by multiplying by four for 400GBASE-SR4 if the unstressed lanes have low BER. In stressed receiver sensitivity measurements, unstressed lanes may be created by setting the power at the

124.8.9.2 Receiver sensitivity for 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2

The receiver sensitivity (OMA_{outer}) for 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2 shall be within the limits given in Table 124–7 if measured using a test pattern for receiver sensitivity in Table 124–10. The conformance test signal at TP3 meets the requirements for a 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2 transmitter followed by an attenuator.

The TECQ of the conformance test signal is measured according to 124.8.5, except that the test fiber is not used. The measured value of TECQ is then used to calculate the limit for receiver sensitivity (OMA_{outer}) as specified in Table 124–7 for 400GBASE-DR4-2, 800GBASE-DR8, and 800GBASE-DR8-2.

	Rx Sens. definition
400GBASE-FR4/LR4 200G/L SMF optical PMDs	Required @ each lane
400GBASE-DR4 800GBASE-DR8 Series	Didn't clearly specify
400GBASE-SR4/800GBASE-SR8	Specifically called out for multi-lane testing, Rx. Sens defined as 400GE and 800GE PMD interface, whose BER is the average of BERs of all lanes.

Pre-requiste: per lane methodology

	Rx Sens. definition
400GBASE-FR4/LR4, 200G/L SMF optical PMDs	Required @ each lane
400GBASE-DR4, 800GBASE-DR8 Series	Didn’t clearly specify
400GBASE-SR4/800GBASE-SR8	Specifically called out for multi-lane testing, Rx. Sens defined as 400GE and 800GE PMD.

Best suited for Rx. Sens compliance testing

174A.8.1.6 Block error ratio method for all lanes using PMA-based measurements

This test method permits measurement of the performance of all physical lanes in a PMD or xAUI-n as a group using error checkers and counters in the PMA. If this test passes, then PHY or xMII Extender will meet the expected codeword error ratio.

174A.8.1.7 Block error ratio method for a single lane using PMA-based measurements

This test method permits measurement of the performance of each physical lane in a PMD or xAUI-n with *p* lanes using error checkers and counters in the PMA. If this test passes for all lanes, then PHY or xMII Extender will meet the expected codeword error ratio.

174A.10.1 Block error ratio method using PCS-based measurements

This test method permits measurement of the performance of all physical lanes in a PHY as a group using FEC error counters in the PCS. If this test passes, then PHY will meet the expected codeword error ratio.

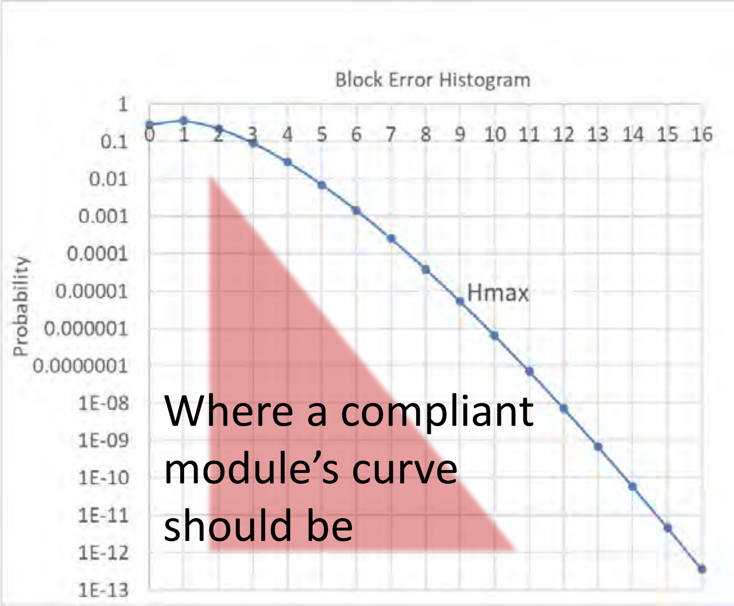
Time consumption = cost of production

Pre-requisite: Receiver Sensitivity and all other parameters of optics is defined as per lane, instead of as a *p-lane* PHY.

Blocks per second: 200G bit /5440/4 → **Time to hit 1 count**: 1/(Hmax(i)*200Gbit /5440/4)

Time required for	0.2min	2.6min	31mins	6.4hours	>1day
Bin x to hit 1 count	12	13	14	15	16p

- For real devices, much longer time will be required to get readable bin count. To reach bin 15, it would be e.g. ~1day.
- To have good confidence of the reading, the error count in each bin is expect to be >10. So another factor of x10 of required time
- It is therefore, impractical to ***measure*** the **full** Histogram, not only in production, also in the design stage and qualification.
- So it will be necessary to make statistical projection, the issue is how
  - What we have been doing with BER, i.e. using a result of finite time to predict/represent the behaviour. The issue of BER is the threshold being overly optimistic, and the assumption of total randomness.



" *The value of test_block_total_count_i should be sufficiently large to reliably verify that the expected block error ratio is met, either by direct measurement or statistical projection. The projection should provide an accurate prediction of the value of Hm(i)(k) that would be observed over longer-term testing or at least provide an upper bound on the value.* "

How does that Translate into testing time and cost

Pre-requisite: Receiver Sensitivity and all other parameters of optics is defined as per lane, instead of as a *p-lane* PHY.

Test Station for Rx Sens./Stressed Rx. Sens.

- BERT if you want to test at PCS
- Golden/Typical Module as the Transmitter
- Sampling Scope(qualifying input signal), can be shared to some extend.
- MCB (not cheap)
- Firmware of module DSP to allow reading of Block Error if want to test at PMA

Time needed to check the Rx. Sens. point:

- Assume collect 2mins of data for each 200Gbps lane
- Consider volume shipping at 10k port /month
- For 800G port, 2min*4*10k ~ 55days*station.
- For 1.6T port, 2min*8*10k~111day*station.
- Only measuring at one single OMA, not examining variations.
- 2min is a wishful assumption, probability not enough.
- If we do a 15-min test to make the total block *sufficient* large, that result in >385day*station for 800GE and >777day*station for 1.6TE

This is why vendors and end users have been using the BER as the proxy test, which requires ~2 seconds per data point

Putting the text into practice

- The block error histogram provides the non-ideal characteristic of a DUT. The block error ratio provides a scientifically correct method of quantifying the link performance. However, it is impossible to conduct in practice.
- The industry can't afford to wait for a real fully measured data anytime the word "volume" is considered.
- Statistical projection is what really matters. But it can have many variables, such as collection time, fitting parameters, etc, which will lead to different result.
- An informative section on the statistical projection method is crucial for the industry and 802.3dj
  - If we leave the spec as is, we end up with end users and customers creating their own interpretation of the spec, and come to different conclusions of good and bad. Isn't this exactly the interop issue we are trying to solve?
- The data showed in he_m_3dj_01a_2507 brings hope in building a projection method with a reasonable collection time.

The current specification of Rx. Sens.

Receiver sensitivity (OMA_{outer}), each lane[c] (max) for TECQ < 0.9 dB for 0.9 dB ≤ TECQ ≤ SECQ	 –3.4 –4.3 + TECQ	dBm
Stressed receiver sensitivity (OMA_{outer}), each lane[c] (max)	–0.9	dBm

[c] Measured with conformance test signal at TP3 (see 180.8) for the block error ratio specified in 180.2.
[d] These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.
[e] No aggressors needed for 200GBASE-DR1 in a single lane device.

180.2 Error ratio allocation

A complete PHY is expected to meet the frame loss ratio specifications in 174A.5.

With a compliant input signal, a PMD receiver is expected to meet the block error ratio of 1.45×10^{-11} (see 174A.5), measured at the PMA adjacent to the PMD using the method described in 174A.8, with BER_{added} equal to 6.4×10^{-5}.

With a compliant input signal, a PHY receiver is expected to meet the block error ratio of 1.45×10^{-11} (see 174A.5), measured at the PCS using the method described in 174A.10, with BER_{added} equal to 3.2×10^{-5}.

In a later section, we have

174A.12 Summary of error ratio allocations

Allocation of frame loss ratio, codeword error ratio, and BER (assuming uncorrelated bit errors) are summarized in Table 174A–1 through Table 174A–3.

Table 174A–1—Error ratio allocations for optical PHYs with no FEC sublayer or with an Inner FEC sublayer

ISL	Frame loss ratio for entire PCS-to-PCS link	Codeword error ratio for entire PCS-to-PCS link	BER for entire PCS-to-PCS link (BER_{total})	BER per ISL [a]
xAUI-n C2C[b]				0.08×10^{-4}
xAUI-n C2M				0.24×10^{-4}
PMD-to-PMD	6×10^{-11}	1.45×10^{-11}	2.92×10^{-4}	2.28×10^{-4}
xAUI-n C2M				0.24×10^{-4}
xAUI-n C2C[b]				0.08×10^{-4}

[a] Measured at the PMA closest to the PMD or AUI component and after Inner FEC decoding, if present, except measured at the Inner FEC for 800GBASE-LR1.
[b] If the PMD is a type defined in Clause 180, Clause 181, Clause 182, Clause 183, or Clause 185, and xAUI-n C2C is a type defined in Annex 120D (i.e., 50 Gb/s per lane) or Annex 120F (i.e., 100 Gb/s per lane), the xAUI-n C2C is expected to meet the BER allocations in this table.

Suggestion:
A complete PHY is expected to meet the frame loss ratio specifications in 174A.5, with each interface in the PHY meeting the error ratio allocations specified in Table 174A-1.