MPI Penalty for Optical PMDs

(Comments 342, 344, 346)

Ali Ghiasi - Ghiasi Quantum/Marvell

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Overview

- Background on DGD penalty
- Background on MPI penalties
- Underlaying MPI assumptions
- Summary of DGD/MPI penalties
- Updated link budget
- Summary.

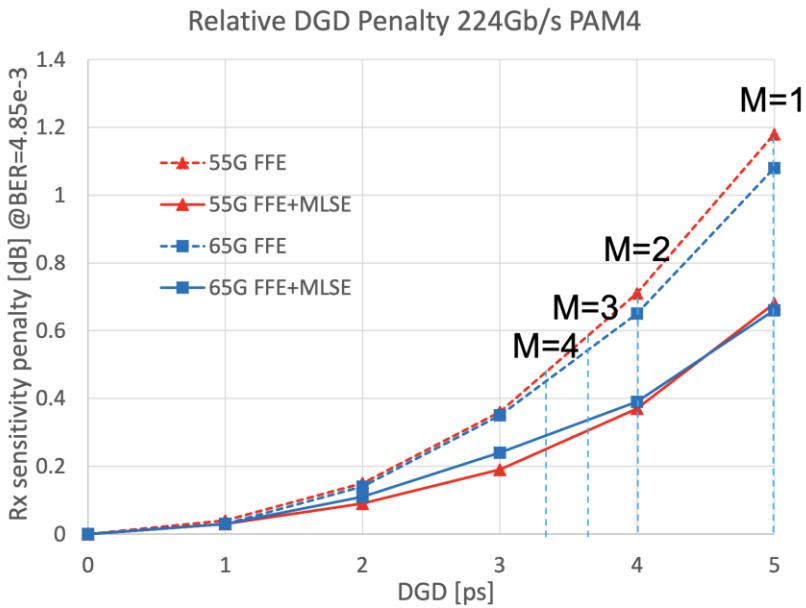
DGD Penalty for Clauses 180-183

- **kuschnerov_3dj_optx_01_230829 show worst case DGD penalty of 0.7 dB for clause 183 800GBASE-LR4 PMD for max DGD of 4 ps**
  - 800GBASE-FR4 with max DGD of 2.3 ps has ~0.18 dB penalty
  - 800GBASE-FR4/DRx-2 with max DGD of 2.3 ps has ~0.18 dB penalty
  - 800GBASE-FR4-500/DRx with max DGD of 2.24 ps has ~0.18 dB penalty
- **For PMDs listing combined DGD/MPI penalty the MPI value should be added to the above values of DGDs.**

DGD penalty for varying number of segments M

- The original single segment (M=1) PMD penalty was based on a FFE+MLSE receiver (0.7dB)
- Assuming multiple segments, a linear equalizer would be sufficient to achieve acceptable performance
- Given the available data and pending further discussion by the industry M=4 seems to be a reasonable assumption
- M=4 can achieve a penalty of ≤0.5dB with an linear FFE equalizer

kuschnerov_3df_01b_221012



Revisiting the MPI/DGD Penalties

- **MPI penalty based on statistical model proposed by King_01a_01116_smf developed in 802.3bs has been adopted for MPI penalty estimation**
  - 802.3bs MPI analysis was based on assumption in liu_3bs_01a_0316
  - 802.3cd MPI analysis and how to reconcile PC and APC connectors penalties was based on traverso_3cd_01_0317
- **ghiasi_3dj_02_2501 raised concern regarding fixed allocation of MPI penalties**
  - 180.7.3 has allocation of 0.1 dB MPI/DGD penalty to support DR double links with 6 discrete reflectance at @-45 dB discrete reflectance channel IL=3 dB
  - 181.7.3 has allocation of 0.5 dB MPI/DGD penalty to support 800GBASE-FR4-500 double link with 4 discrete reflectance @-35 and 4 discrete reflectance @-45 dB channel IL=3.5 dB
  - 182.7.3 has allocation of 0.4 dB MPI/DGD penalty to support DR-2 double links with 4 discrete reflectance at @-35 dB and 4 discrete reflectance @-45 dB channel IL=4 dB
  - 183.7.3 has allocation of 0.4 dB MPI/DGD penalty to support 800GBASE-FR4 double-link with 4 MPO @-45 dB and 4 LC@-35 dB discrete reflectance and channel ILmax=4 dB
- **johnson_3dj_adhoc_01_250220 additional background on the history of MPI penalty and there may be good reason to revisit some of the underlaying assumptions**
- **For some of MPI penalty underlaying details, see ghiasi_3dj_01b_2505.**

Underlaying MPI Penalty Assumptions

- **Underlaying assumptions in the 802.3bs/cd**
  - Cable plant follow double or triple link model
  - Max loss at the end of cable plant
  - Cell A5 in J. King spreadsheet require inputting PAM2 BER but inadvertently PAM4 BER was used in this cell for bs/cd MPI estimates, for correct MPI calculation convert PAM4 BER by 4/3 in cell A5 to convert back to NRZ
  - LC reflectance -35 dB
  - MPO reflectance -45 dB
  - ER=5 dB
  - BER 2E-4
  - MPI penalty extrapolated to 1E-6

- **Proposed assumptions for 802.3dj**
  - Cable plant follow double or triple link model
  - Placing 1/2 of the loss in middle of cable
  - LC reflectance -35 dB
  - MPO reflectance -45 dB
  - ER=3.5 dB (min allowed) to better support 200G SiP
  - BER 2.28E-4 for CL180 and 182, BER 4.8E-3 for CL182 and 183
  - MPI penalty extrapolation for now keep at 1E-6 but when cross-penalty due to TDECQ eye-closure is included then penalty extrapolation can be reduced to 1E-5 based on improved SMF channel model as in rodes_3dj_01a_2401.

Best Method to Reconcile MPI Penalty for Mixed MPO/LC PMDs

- **traverso_3cd_01_0317 proposed method can reconcile MPI penalty in mixed mode PMDs such as for 200GBASE-DR and 00GBASE-DR-2**
  - Row 0 with 0 >-45 dB and ≤-35 dB reflectance is the MPI for double link MPO cable plant
  - Row 0 with 0 >-45 dB and ≤-35 dB reflectance is used for MPI allocation of double link LC cable plant but cable plant loss are reduced with additional number of discrete reflectance's (LC) >-45 and ≤-35 dB
- **Extending clause 180 DR MPI-loss trade off can be applied to DR-2, FR4-500, FR4, and LR4 as suggested in Johnson_3dj_01_2505.**

MPI Penalty Calculation Table from Traverso

MPI Penalty (dB)		Number of discrete reflectances > -55 dB and ≤ -45 dB								
		0	1	2	3	4	5	6	7	8
Number of discrete reflectances > -45 dB and ≤ -35 dB	0	0	0.02	0.03	0.04	0.05	0.06	0.07	0.08	0.10
	1	0.05	0.06	0.05	0.09	0.11	0.12	0.11	0.15	0.12
	2	0.1	0.12	0.13	0.16	0.19	0.2	0.22	0.23	0.22
	3	0.18	0.18	0.2	0.2	0.24	0.3	0.3	0.32	*
	4	0.26	0.27	0.32	0.34	0.36	0.4	0.41	*	*
	5	0.32	0.33	0.38	0.4	0.44	0.48	*	*	*
	6	0.45	0.48	0.51	0.54	0.57	*	*	*	*

x.yz = these values exceed the proposed MPI penalty limit – see slide 3

Table 180–12—Maximum channel insertion loss versus number of discrete reflectances

Maximum channel insertion loss (dB)		Number of discrete reflectances > –55 dB and ≤ –45 dB								
		0	1	2	3	4	5	6	7	8
Number of discrete reflectances > –45 dB and ≤ –35 dB	0	3	3	3	3	3	3	3	3	3
	1	3	3	3	3	3	3	3	3	3
	2	3	3	3	2.9	2.9	2.9	2.9	2.9	2.9
	3	2.9	2.9	2.9	2.9	2.9	2.8	2.8	2.8	—[a]
	4	2.8	2.8	2.8	2.8	2.7	2.7	2.7	—[a]	—[a]
	5	2.8	2.8	2.7	2.7	2.7	2.6	—[a]	—[a]	—[a]
	6	2.6	2.6	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]	—[a]

[a] The indicated combination of reflectances does not provide a supported maximum channel insertion loss.

Summary of MPI/DGD Penalties

- **MPI/DGD penalty must be sufficient to support expected double or triple link configuration.**

Clause	PMD	MPI Penalty DJ D1.5	DGD Penalty DJ D1.5	MPI Penalty Calculation	DGD Penalty Estimate	Total MPI/DGD Penalties	
180	DR	0.1 dB*		0.15 dB	0.18 dB	0.3 dB*	
181	FR4-500	0.5 dB*		0.5 dB	0.18 dB	0.7 dB*	
182	DR-2	0.4 dB*		0.09 dB	0.18 dB	0.3 dB*	
183	FR4	0.5 dB*		0.3 dB	0.18 dB	0.5 dB*	
183	LR4	0.4 dB	0.7 dB	0.4 dB	0.7 dB	NC	NC

* Rounded combined MPI/DGD penalties.

TX/RX Specifications Adjustment as Result of MPI/DGD Penalties

	Clause 180 DRn		Clause 181 FR4-500		Clause 182 DRn-2	
PMD Parameters	DJ D2.0	This proposal Comment 342	DJ D2.0	This proposal Comment 344	DJ D2.0	This proposal Comment 346
Illustrative link budget		Δ=+0.2 dB		Δ=+0.2 dB		Δ=-0.1 dB
Power budget (for max TDECQ)	6.5	6.7	7.4	7.6	7.8	7.7
Allocation for penalties (for max TDECQ)	3.5	3.7	3.9	4.1	3.8	3.7
Transmitter characteristics						
Average launch power, each lane (min)	-3.3	-3.1	-2.2	-2.0	-3.3	-3.1
Outer Optical Modulation Amplitude (OMAouter), each lane (min) for max(TECQ, TDECQ) < 0.9 dB for 0.9 dB < max(TECQ, TDECQ) < 3.4 dB	 -0.3 -1.2+TDECQ	 -0.1 -1.0+TDECQ	 0.8 -0.1+TDECQ	 1.0 0.1+TDECQ	 -0.3 -1.2+TDECQ	 -0.1 -1.0+TDECQ
Receiver characteristics						
Average receive power, each lane (min)	-6.3	-6.1	-5.7	-5.5	-7.3	-7.1
Receiver sensitivity (OMAouter), each lane (max) for TECQ < 0.9 dB for 0.9 dB < TECQ < SECQ					 -4.7 -5.6+TDEC	 -4.4 -5.3+TDEC
Stressed receiver sensitivity (OMAouter), each lane (max)					-2.2	-1.9

Summary

- **The MPI/DGD penalties must be sufficient to support the underlying double or tipple link configurations**
  - CL180 combined DGD/MPI to support double link with 6 MPOs must increase from current 0.1 dB to 0.3 dB
  - CL181 PMDs combined DGD/MPI to support double link with 4 MPOs and 4 LCs must increase from current 0.5 dB to 0.7 dB
  - CL182 PMDs combined DGD/MPI to support double link with 6 MPOs needs to decrease from 0.4 dB to 0.3 dB
  - Current combined MPI+DGD penalties of 0.5 dB for CL183 800GBASE-FR4 PMDs is about the right allocation to support double link with 4 MPOs and 4 LCs
  - Current combined MPI+DGD penalties of 0.4/0.7 dB for CL183 800GBASE-LR4 PMDs is about the right allocation to support triple configuration with 6 LC and 4 MPOs
- **Analysis is consistent in johnson_3dj_01a_2505 except for Clause 181 DGD/MPI penalty of 0.68 dB was rounded down to 0.6 dB by Johnson**
- **Trading off MPI penalty vs channel IL as in Table 180-12 allow supporting greater set of channel configurations but the MPI/DGD penalty must be sufficient to support the basic link configuration**
- **Current MPI penalty doesn't account cross-penalty where low transition (low ISI) reflected pulse interfere with high transition (high ISI TDECQ ~ 3 dB)**
  - Potentially may double the penalty on high ISI pulses!

Thank You!