Supporting Materials for 803.2dj D2.0 Comment #466

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Cl **178B** *SC* **178B.5.1** *P* **788** *L* **21** # 466

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Comment Type **TR** *Comment Status* **D** *(Common) ILT timers*

Having an unspecified time limit for rx_ready assertion (from entry to TRAIN_LOCAL) makes for unpredicatable link up behaviors. A time limit from the point at which TRAIN_LOCAL is entered to entry to TRAIN_REMOTE will improve predictability of operation which will facilitate predicatble device behaviors.

SuggestedRemedy

Presentation for a solution to be provided.

ILT timeouts

For legacy rates LinkTraining was defined for a single link segment from PMD to PMD. The standard specified a time limit this process was allotted (copper). All implementers (component and systems) could look to the standard to set their behaviors based on that value for their copper interconnects.

With ILT path-startup we need to constrain certain time limits on processes to enable multi-vendor interop to work with all parties using the standard to define their behavior, rather than in field debugging of “what” the other guy requires.

Adaptation time limit

In clause 73 and 136 the Link Training process begins when the PMD starts to the drive the link and it equalizes the link segment between the two PMDs. A time limit is set for this which establishes how soon the PCS data begins to flow at a “good” BER between the PMDs. This constraint is used by both SerDes providers and users to know how much time they’re to allot towards this process which typically the dominate time in establishing the path.

Does setting a limit cause a ILT restart

Setting a constraint for this does not mean the entire ILT path-start up must begin anew. The isl_ready for the interface will not be asserted which means the remote_rts of the dependent link segment will remain false.

Thus a link-segment that incurs an adaptation timeout would end up in the FAIL state for some (or all) the physical lanes. Those particular lanes could be debugged/restarted.

Proposal

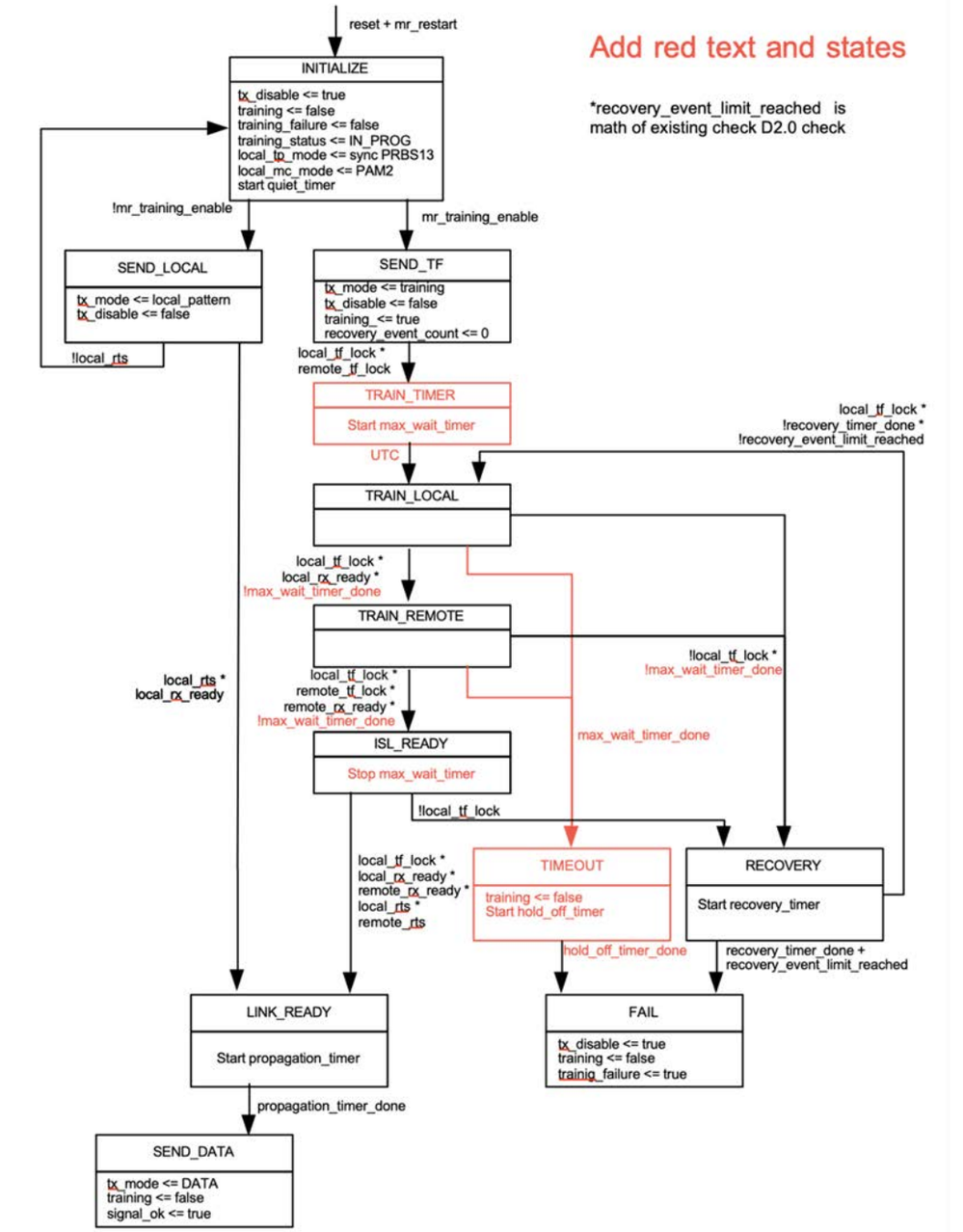
Add in a state to start a hard timeout timer between ST and TRAIN_LOCAL.

Add the TIMEOUT state that sends Training frames for an addition period of time before squelching.

Stop the timer when entering the ISL_READY state.

Timer duration is register controlled with defaults of 12s for all DJ users of 178B but when set to 0, does not generate a done event.

FSM update


reset + mr_restart
INITIALIZE
tx_disable <= true
training <= false
training_failure <= false
training_status <= IN_PROG
local_tp_mode <= sync PRBS13
local_mc_mode <= PAM2
start quiet_timer
Add red text and states
*recovery_event_limit_reached is math of existing check D2.0 check
!mr_training_enable
mr_training_enable
SEND_LOCAL
tx_mode <= local_pattern
tx_disable <= false
!local_rts
SEND_TF
tx_mode <= training
tx_disable <= false
training_<= true
recovery_event_count <= 0
local_tf_lock *
remote_tf_lock
TRAIN_TIMER
Start max_wait_timer
UTC
local_tf_lock *
!recovery_timer_done *
!recovery_event_limit_reached
TRAIN_LOCAL
local_tf_lock *
local_rx_ready *
!max_wait_timer_done
TRAIN_REMOTE
local_rts *
local_rx_ready
local_tf_lock *
remote_tf_lock *
remote_rx_ready *
!max_wait_timer_done
!local_tf_lock *
!max_wait_timer_done
max_wait_timer_done
ISL_READY
Stop max_wait_timer
!local_tf_lock
local_tf_lock *
local_rx_ready *
remote_rx_ready *
local_rts *
remote_rts
TIMEOUT
training <= false
Start hold_off_timer
RECOVERY
Start recovery_timer
hold_off_timer_done
recovery_timer_done +
recovery_event_limit_reached
LINK_READY
Start propagation_timer
FAIL
tx_disable <= true
training <= false
trainig_failure <= true
propagation_timer_done
SEND_DATA
tx_mode <= DATA
training <= false
signal_ok <= true

max wait timer

178B.14.3.3

max_wait_timer

This timer is started when the training control state machine enters the TRAIN_TIMER state (see Fig 178B-8). The terminal count of this timer is max_wait_timer_duration variable * 1ms (see Table 178B-6). The default duration is specified by the the AUI component or PMD. To facilitate debug when the max_wait_timer_duration is set to 0 the timer duration is infinite and max_wait_time_done always remains false.

45.x.x.x.x ILT max_wait_timer_duration

16b MDIO register that holds the maximum duration for adapting the equalization of the link when transmitting the training pattern during ILT specified in Annex 178B. Add to Table 178B-6 mapping table.

hold_off_timer

178B.14.3.3

hold_off_timer

This timer is started when the PMD control state diagram enters the TIMEOUT QUIET state. The terminal count of holdoff_timer is 80 ms ± 2%.