Cable Assembly TP1-TP4 Insertion Loss (Comment #358)

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Week of Sept 15, 2025

TE Connectivity

EVERY CONNECTION COUNTS

Supporters

Agenda

- Introduction
- Cable Assembly Insertion Loss Data
- Insertion Loss Budgets & Host Impact
- Proposed Changes

Introduction

Comment #358

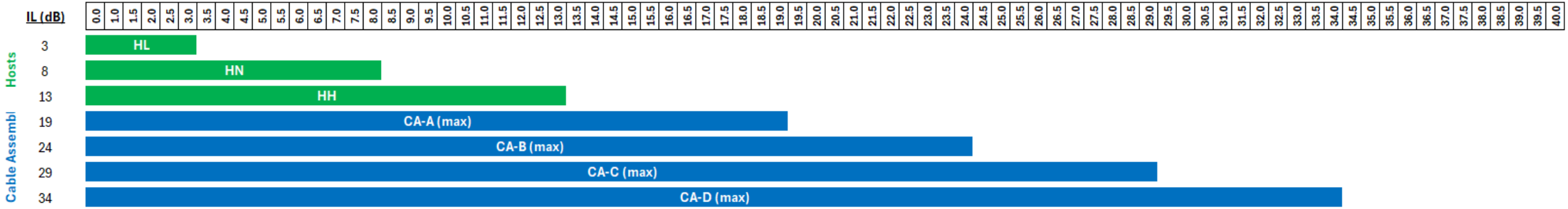
Cable assembly TP1-TP4 insertion loss specifications prove challenging to meet when accounting for all sources of variation, specifically for the CA-A and CA-B cable assembly classes. A more manufacturable specification needs an additional 1 dB insertion loss to be allocated to the cable assembly for CA-A and CA-B.

Suggested Remedy

- Reduce the insertion loss allocation for all three host classes (HL/HN/HH) by 0.5 dB (Table 179A-1).
- Increase the TP1-TP4 cable assembly insertion loss (Table 179-14) for CA-A from 19 dB to 20 dB, and for CA-B from 24 dB to 25 dB.
- Change the partial host PCB trace lengths in Table 179-19 to provide the host loss reduction
  - (see slides 10-11 for full implementation details)

Cable Assembly & Partial Host Loss

Current Draft 2.1



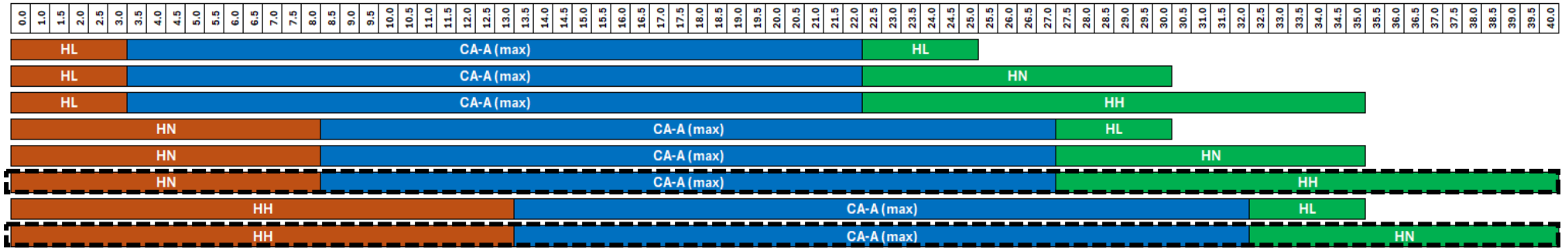
- 3 host classes. HL = 3 dB, HN = 8 dB, HH = 13 dB (maximum)
  - These are partial host losses. The full host loss includes an additional 5.95 dB that includes the reference packages and additional host PCB trace.
  - Full host loss: HL/HN/HH = 8.95/13.95/18.95 dB (maximum)
- 4 Cable Assy classes: CA-A = 19 dB, CA-B = 24 dB, CA-C = 29 dB, CA-D = 34 dB (maximum)
- The 40 dB total budget (die to die) constrains the allowed combinations of hosts and cable assemblies.

Current TP1-TP4 Loss Budgets

Draft 2.1

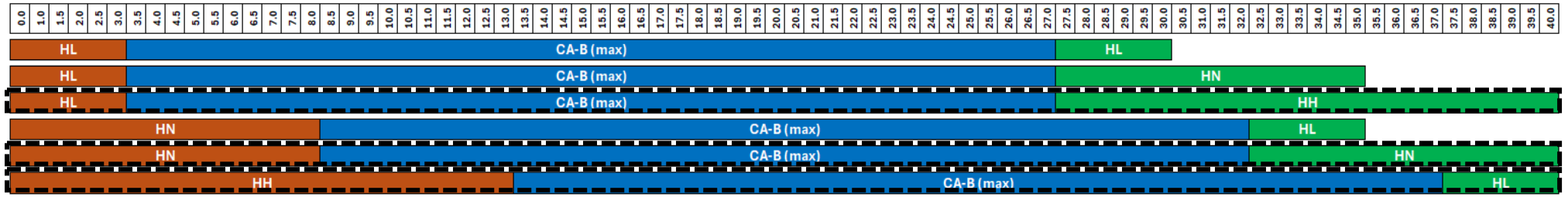
CA-A

Host	CA	Host	IL (dB)
HL	A	HL	25
HL	A	HN	30
HL	A	HH	35
HN	A	HL	30
HN	A	HN	35
HN	A	HH	**40**
HH	A	HL	35
HH	A	HN	**40**



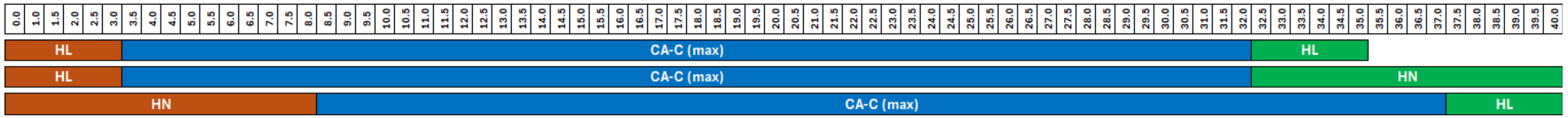
CA-B

Host	CA	Host	IL (dB)
HL	B	HL	30
HL	B	HN	35
HL	B	HH	**40**
HN	B	HL	35
HN	B	HN	**40**
HH	B	HL	**40**



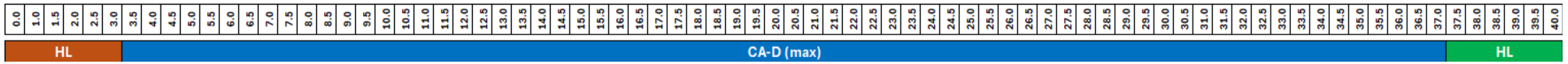
CA-C

Host	CA	Host	IL (dB)
HL	C	HL	35
HL	C	HN	**40**
HN	C	HL	**40**



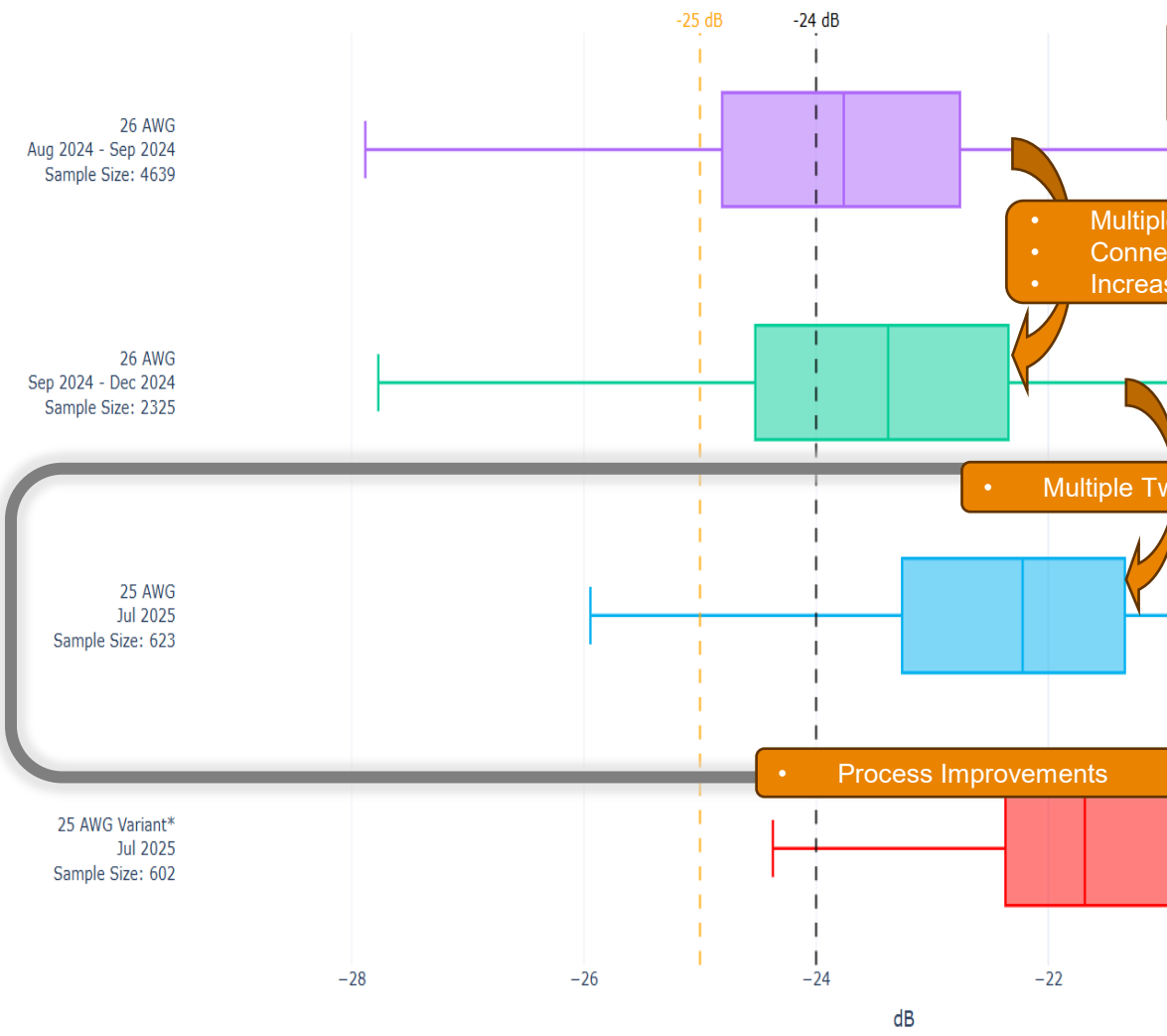
CA-D

Host	CA	Host	IL (dB)
HL	D	HL	**40**



Limiting case

1.0m 26AWG & 1.0m 25AWG DAC, S_{DD21} @ 53.12GHz



Initial Pre-Production Builds

Assembly yield (24dB limit)	**0%**
Lane yield (24dB limit)	56%

- Multiple Paddle Card Design Updates
- Connector/Fixture Improvements
- Increasing Process Automation

Assembly yield (24dB limit)	**3%**
Lane yield (24dB limit)	64%

- Multiple Twinax Improvements

Current Product that meets robustness standards in Industry

Assembly Yield (24dB limit)	**15%**
Lane Yield (24dB limit)	90%
Assembly yield (25dB limit)	**62%**
Lane yield (25dB limit)	97%

- Process Improvements

***Introduces critical process changes that degrade robustness & product quality**
Unacceptable Product

Assembly Yield (24dB limit)	**82%**
Lane Yield (24dB limit)	98%
Assembly yield (25dB limit)	**87%**
Lane yield (25dB limit)	99%

Aug 2024
Sep 2024
Dec 2024
Jul 2025

At the time CA-x budgets were set, there was insufficient cable assembly build experience

Proposed Loss Budget Reallocation

- Needs: Reduce combined host loss by 1 dB.
- Analysis

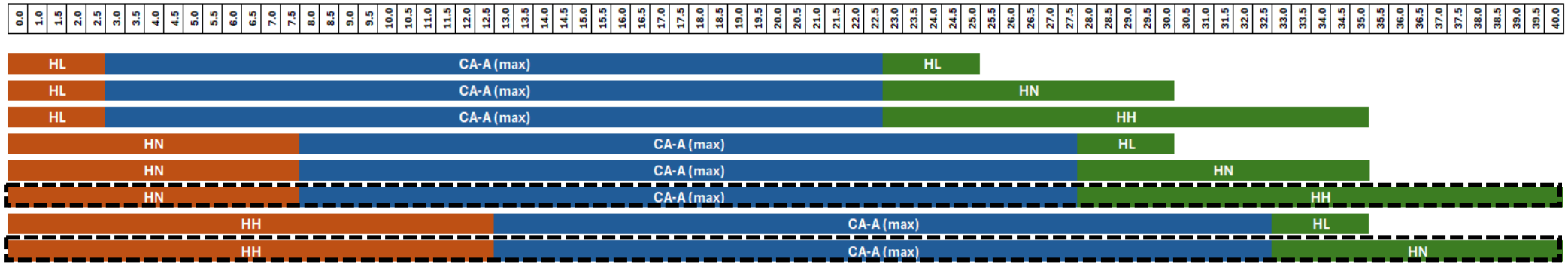
Cable Assembly	Host Combination	Proposal
CA-A	HN+HN	Reduce HN by 0.5 dB
CA-B	HN+HH	Reduce HH by 0.5 dB
	HL+HH	Reduce HL by 0.5 dB

- Proposed partial host & CA insertion loss:
  - HL = 2.5 dB, HN = 7.5 dB, HH = 12.5 dB
  - CA-A = 20 dB, CA-B = 25 dB, CA-C = 29 dB, CA-D = 34 dB
- Host physical design impact: Assume all reduction from host PCB (no change to pkg).
  - 0.5 dB IL reduction ~10 mm trace length reduction on each host
  - Depends on dielectric material, surface roughness and stackup/trace geometry

TP1-TP4 Loss Budgets with Proposed Changes

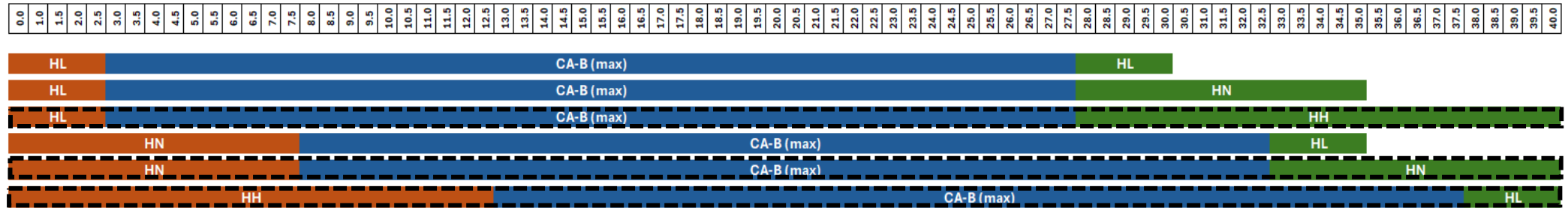
CA-A

Host	CA	Host	IL (dB)
HL	A	HL	25
HL	A	HN	30
HL	A	HH	35
HN	A	HN	30
HN	A	HN	35
HN	A	HH	**40**
HH	A	HL	35
HH	A	HN	**40**



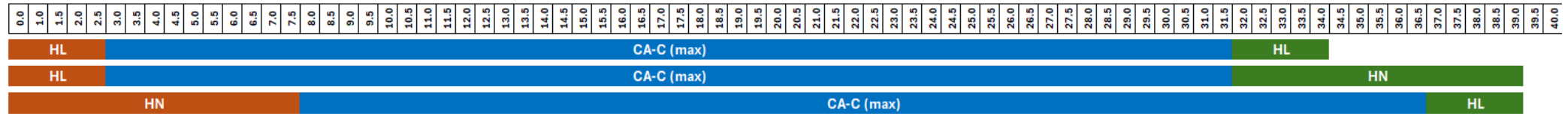
CA-B

Host	CA	Host	IL (dB)
HL	B	HL	30
HL	B	HN	35
HL	B	HH	**40**
HN	B	HL	35
HN	B	HN	**40**
HL	B	HL	**40**



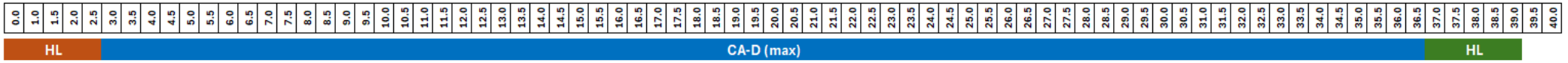
CA-C

Host	CA	Host	IL (dB)
HL	C	0	34
HL	C	HN	39
HN	C	HL	39



CA-D

Host	CA	Host	IL (dB)
HL	D	HL	39



Limiting case

Proposed Changes

179.11

Table 179–14—Cable assembly characteristics summary

Description	Reference	Value	Unit
Insertion loss at 53.125 GHz, *ILdd* (max)	179.11.2		
CA-A		~~19~~ 20	dB
CA-B		~~24~~ 25	dB
CA-C		29	dB
CA-D		34	dB

179.11.7.1

Table 179–18—Partial host channel model parameters per Host class

Parameter	Host class			Units
	HL	HN	HH	
Package class	A	B	B	—
Package transmission line 1 length, z_p (1)	8	15	45	mm
Partial host PCB transmission line length, z_p (h)	~~9~~ 2	~~70~~ 61	~~60~~ 51	mm

NOTE—For each host class, the sum of the differential insertion loss (ILdd) at 53.125 GHz of the partial host channel (excluding the device termination) and the reference mated test fixtures (see Equation (179B–5) and Figure 179A–1) is equal to the recommended maximum host channel insertion loss in 179A.4 for that host class.

179A.4

Table 179A–1—Recommended differential insertion loss limits at 53.125 GHz

Host class	Host channels		TP0d to TP2 or TP3 to TP5d	
	Range (dB)		Max (dB)	
Host-Low (HL)	4.45 to ~~8.95~~	8.45	~~12.75~~	12.25
Host-Nominal (HN)	4.45 to ~~13.95~~	13.45	~~17.75~~	17.25
Host-High (HH)	4.45 to ~~18.95~~	18.45	~~22.75~~	22.25

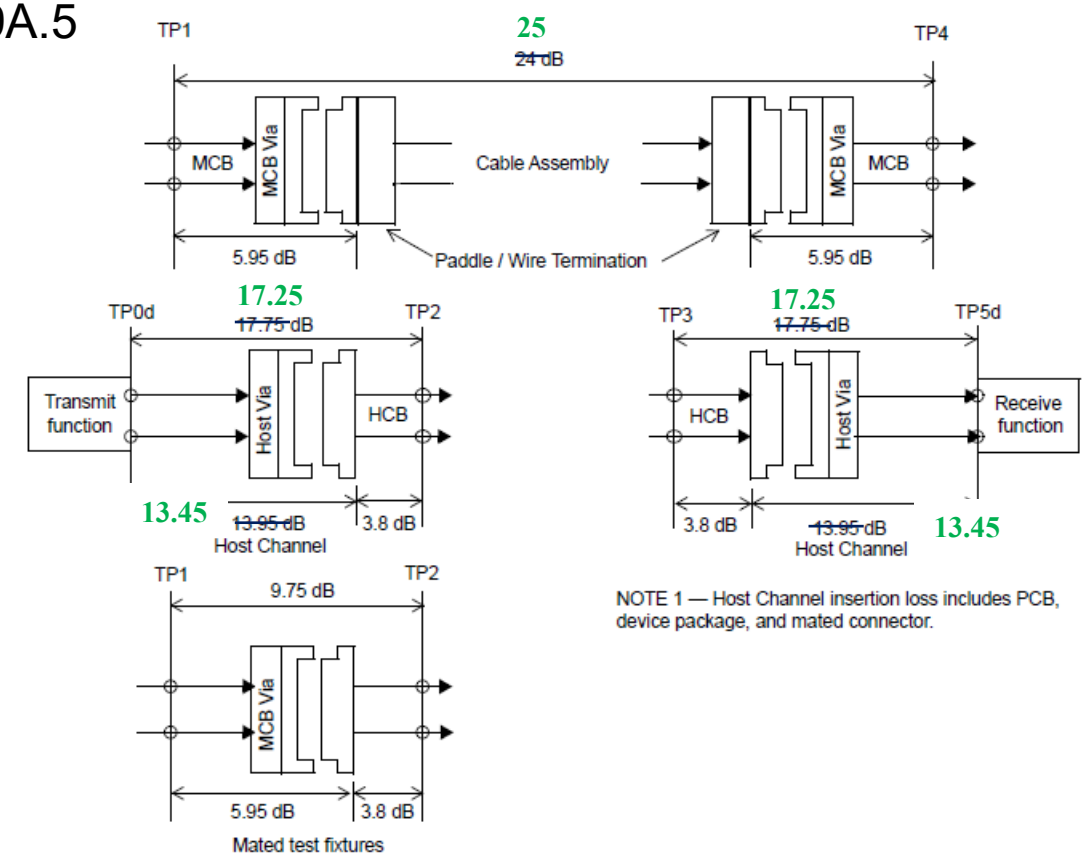
179A.5

Table 179A–2—Maximum Insertion loss budget values at 53.125 GHz

Link Configuration	$ILdd_{CA,max}$ (dB)	$ILdd_{TP0d\text{-}TP2,max}$ (dB)	$ILdd_{TP3\text{-}TP5d,max}$ (dB)	$ILdd_{MTFref}$ (dB)	$ILdd_{Ch,max}$ (dB)
HH to HN	~~19~~ 20 (CA-A)	~~22.75~~ 22.25	~~17.75~~ 17.25	9.75	40
HH to HL	~~24~~ 25 (CA-B)	~~22.75~~ 22.25	~~12.75~~ 12.25	9.75	40
HN to HN	~~24~~ 25 (CA-B)	~~17.75~~ 17.25	~~17.75~~ 17.25	9.75	40
HN to HL	29 (CA-C)	~~17.75~~ 17.25	~~12.75~~ 17.25	9.75	40
HL to HL	34 (CA-D)	~~12.75~~ 12.25	~~12.75~~ 12.25	9.75	40

Proposed Changes

179A.5



NOTE 1 — Host Channel insertion loss includes PCB, device package, and mated connector.

NOTE 2 — The MCB and HCB ILdd allocations include the RF connector (up to the RF connector reference plane).

MCB = Module Compliance Board, 179B.3
HCB = Host Compliance Board, 179B.2
MCB Via = transition via to MDI connector on an MCB
Host Via = transition via to MDI connector on a Host Channel
Paddle/Wire Termination = transition structure(s) in a Cable Assembly not present on an HCB

Figure 179A–1—Host-Nominal to Host-Nominal, Cable assembly, and test fixture insertion loss at 53.125 GHz

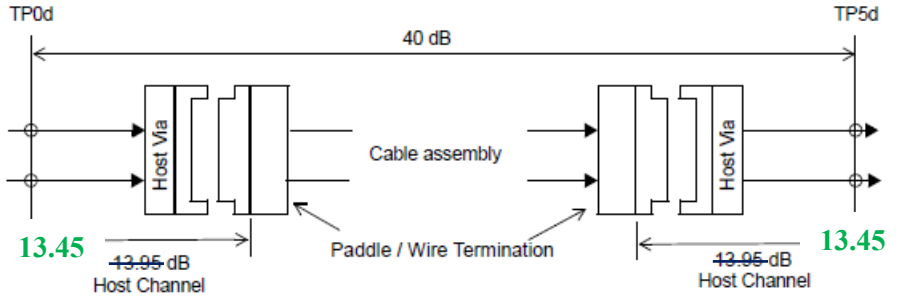


Figure 179A–2—HN-to-HN Channel Max (TP0d-TP5d) at 53.125 GHz

Channel Max (TP0d-TP5d) lldd = 40 dB @ 53.125 GHz = (25+17.25+17.25)-(2*9.75)
Channel Max (TP0d-TP5d) lldd = 40 dB @ 53.125 GHz = (2*13.45)+13.1

Summary

Proposal to make the cable assembly insertion loss specifications more robust and manufacturable:

- add 1 dB to the TP1-TP4 insertion loss specifications for the CA-A and CA-B cable assembly classes.
- remove 0.5 dB from the host loss specifications for the HL/HN/HH host classes
  - with commensurate reductions in partial host insertion loss & PCB trace lengths

Appendices

Die-Die Insertion Loss Budget Remains within 40 dB

TX Host	CA	RX Host	Partial TX Host	CA (TP1-TP4)	Partial RX Host	Total
HL	CA-A	HL	2.5	20	2.5	25
HL	CA-A	HN	2.5	20	7.5	30
HL	CA-A	HH	2.5	20	12.5	35
HN	CA-A	HL	7.5	20	2.5	30
HN	CA-A	HN	7.5	20	7.5	35
HN	CA-A	HH	7.5	20	12.5	40
HH	CA-A	HL	12.5	20	2.5	35
HH	CA-A	HN	12.5	20	7.5	40
HL	CA-B	HL	2.5	25	2.5	30
HL	CA-B	HN	2.5	25	7.5	35
HL	CA-B	HH	2.5	25	12.5	40
HN	CA-B	HL	7.5	25	2.5	35
HN	CA-B	HN	7.5	25	7.5	40
HH	CA-B	HL	12.5	25	2.5	40
HL	CA-C	HL	2.5	29	2.5	34
HL	CA-C	HN	2.5	29	7.5	39
HN	CA-C	HL	7.5	29	2.5	39
HL	CA-D	HL	2.5	34	2.5	39

No change to Total ILdd

Total Ildd decreases by -1 dB

Detailed Loss Budgets (TP1-TP4)

Cable Assembly IL (dB)

		TP1-TP4
Current	CA-A	19
	CA-B	24
	CA-C	29
	CA-D	34
Proposed	CA-A	20
	CA-B	25
	CA-C	29
	CA-D	34

Partial Host IL (dB)

		Pkg	PCB	Total
Current	HL	2.3	0.7	3.0
	HN	4.0	4.0	8.0
	HH	9.7	3.3	13.0
Proposed	HL	2.3	0.2	2.5
	HN	4.0	3.5	7.5
	HH	9.7	2.8	12.5

Loss Budgets

	TX Host	HL	HL	HL	HN	HN	HN	HH	HH	HL	HL	HL	HN	HN	HH	HL	HL	HN	HL
	Cable Assembly	CA-A	CA-A	CA-A	CA-A	CA-A	CA-A	CA-A	CA-A	CA-B	CA-B	CA-B	CA-B	CA-B	CA-B	CA-C	CA-C	CA-C	CA-D
	RX Host	HL	HN	HH	HL	HN	HH	HL	HN	HL	HN	HH	HL	HN	HL	HL	HN	HL	HL
Current	TX Package	2.3	2.3	2.3	4.0	4.0	4.0	9.7	9.7	2.3	2.3	2.3	4.0	4.0	9.7	2.3	2.3	4.0	2.3
	TX partial PCB	0.7	0.7	0.7	4.0	4.0	4.0	3.3	3.3	0.7	0.7	0.7	4.0	4.0	3.3	0.7	0.7	4.0	0.7
	CA (TP1-TP4)	19.0	19.0	19.0	19.0	19.0	19.0	19.0	19.0	24.0	24.0	24.0	24.0	24.0	24.0	29.0	29.0	29.0	34.0
	RX partial PCB	0.7	4.0	3.3	0.7	4.0	3.3	0.7	4.0	0.7	4.0	3.3	0.7	4.0	0.7	0.7	4.0	0.7	0.7
	RX Package	2.3	4.0	9.7	2.3	4.0	9.7	2.3	4.0	2.3	4.0	9.7	2.3	4.0	2.3	2.3	4.0	2.3	2.3
	Total	25.0	30.0	35.0	30.0	35.0	**40.0**	35.0	**40.0**	30.0	35.0	**40.0**	35.0	**40.0**	**40.0**	35.0	**40.0**	**40.0**	**40.0**

	TX Host	HL	HL	HL	HN	HN	HN	HH	HH	HL	HL	HL	HN	HN	HH	HL	HL	HN	HL
	Cable Assembly	CA-A	CA-A	CA-A	CA-A	CA-A	CA-A	CA-A	CA-A	CA-B	CA-B	CA-B	CA-B	CA-B	CA-B	CA-C	CA-C	CA-C	CA-D
	RX Host	HL	HN	HH	HL	HN	HH	HL	HN	HL	HN	HH	HL	HN	HL	HL	HN	HL	HL
Proposed	TX Package	2.3	2.3	2.3	4.0	4.0	4.0	9.7	9.7	2.3	2.3	2.3	4.0	4.0	9.7	2.3	2.3	4.0	2.3
	TX partial PCB	0.2	0.2	0.2	3.5	3.5	3.5	2.8	2.8	0.2	0.2	0.2	3.5	3.5	2.8	0.2	0.2	3.5	0.2
	CA (TP1-TP4)	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0	25.0	25.0	25.0	25.0	25.0	25.0	29.0	29.0	29.0	34.0
	RX partial PCB	0.2	3.5	2.8	0.2	3.5	2.8	0.2	3.5	0.2	3.5	2.8	0.2	3.5	0.2	0.2	3.5	0.2	0.2
	RX Package	2.3	4.0	9.7	2.3	4.0	9.7	2.3	4.0	2.3	4.0	9.7	2.3	4.0	2.3	2.3	4.0	2.3	2.3
	Total	25.0	30.0	35.0	30.0	35.0	**40.0**	35.0	**40.0**	30.0	35.0	**40.0**	35.0	**40.0**	**40.0**	34.0	39.0	39.0	39.0

Δ	Total	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	0.0	-1.0	-1.0	-1.0	-1.0

- Proposed values with blue/green text are increased/decreased from current values.
  - CA-A, CA-B increase by 1 dB
  - TX/RX partial PCB for HL/HN/HH decrease by 0.5 dB (each)
- Limiting cases (40 dB total insertion loss) are highlighted in **bold purple**.