Capturing Jitter Penalty with TDECQ and FRx

(Comments 124, 125, 126, 127, 128)

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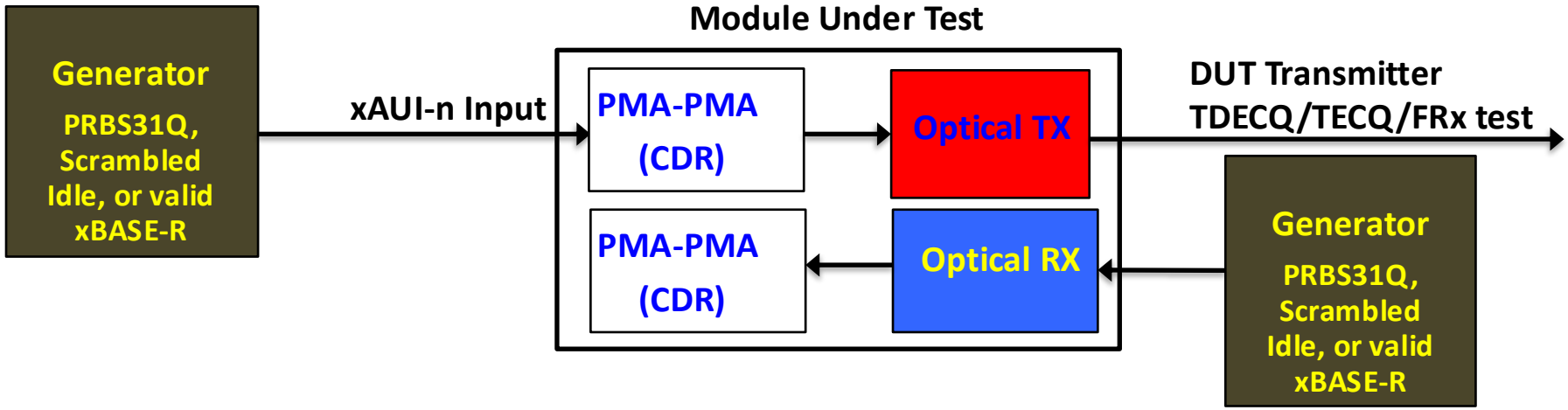
Background

- **Prior to DJ project TDECQ was defined with local SSPRQ pattern from the module ignoring jitter through the module and without counter propagating crosstalk traffic**
  - In D1.4 when xAUI-n is accessible the clock source for SSPRQ test pattern is derived from xAUI-n input
  - Also added in D1.4 was asynchronous crosstalk test pattern to optical receive input
- **Changes made in D1.4 were in the right direction**
  - Unless the test include the worst case xAUI-n input jitter TDECQ and Functional Receiver FRx will not capture problematic transmitter with high jitter
  - An xAUI-n driven from a clean generator will not transfer any jitter from xAUI-n input to TP2!

Current TDECQ/FRx Jitter Shortcoming

- **Current DJ draft short coming is that xAUI-n may be a benign generator, therefore TDECQ/TECQ/FRx measurement will not include any host contributed jitter transfer!**
  - Both clause 120G and 176D xAUI-n have CDR corner frequency of 4 MHz.



Current TDECQ/FRx Jitter Shortcoming

- **Clause 120E 100G xAUI-n and clause 176D 200G xAUI-n have identical jitter tolerance corner frequencies except clause 176D has additional jitter frequencies**
  - Jitter in table 120G.3.4.3 or 176D-12 when applied to an x-AUI-n to 200G PMA can result following output jitters
    - Integrated output jitter in case of 100G 2:1 PMA will double to *0.1 UI* with 4 MHz CDR
    - Integrated output jitter in case of 200G 1:1 PMA can be *0.05 UI* with 4 MHz CDR
  - Considering a typical eye opening of just ~0.2 U at TP2 the addition of 0.05/0.1 UI can add significant penalty to reported TDECQ/TECQ/FRx!

Table 120E–6—Applied sinusoidal jitter

Parameter	Case A	Case B	Case C	Case D	Case E	Units
Jitter frequency	0.04	1.333	4	12	40	MHz
Jitter amplitude	5	0.15	0.05	0.05	0.05	UI

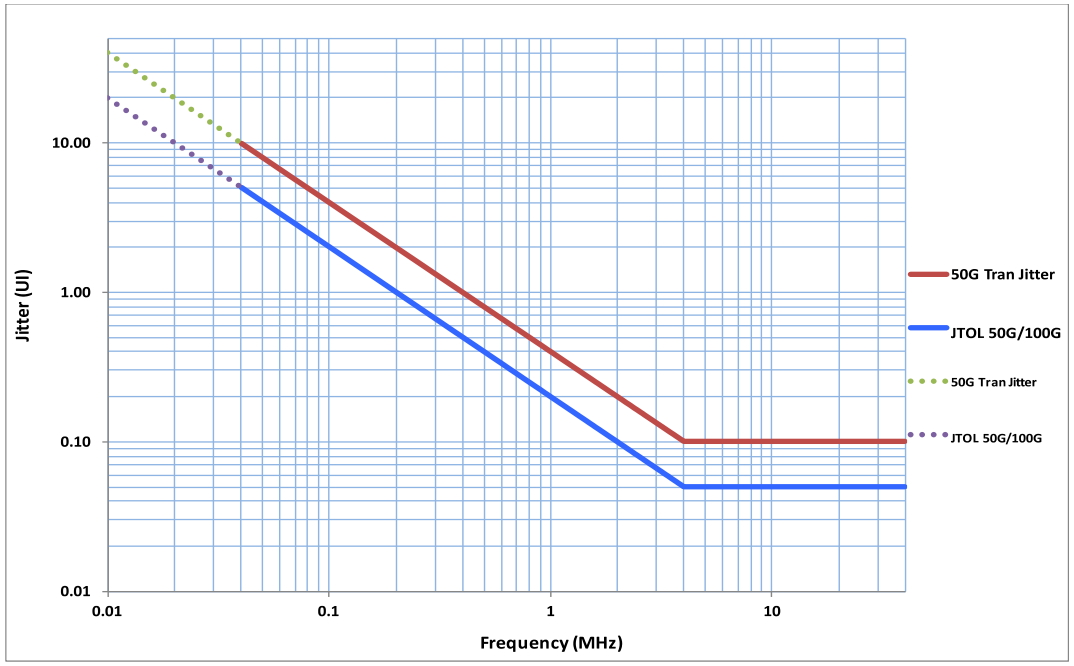
Table 176D–12—Receiver jitter tolerance parameters

Parameter	Case A	Case B	Case C	Case D	Case E	Case F	Case G	Units
Jitter frequency	0.04	0.1333	0.4	1.333	4	12	40	MHz
Jitter amplitude (peak-to-peak)	5	1.5	0.5	0.15	0.05	0.05	0.05	UI

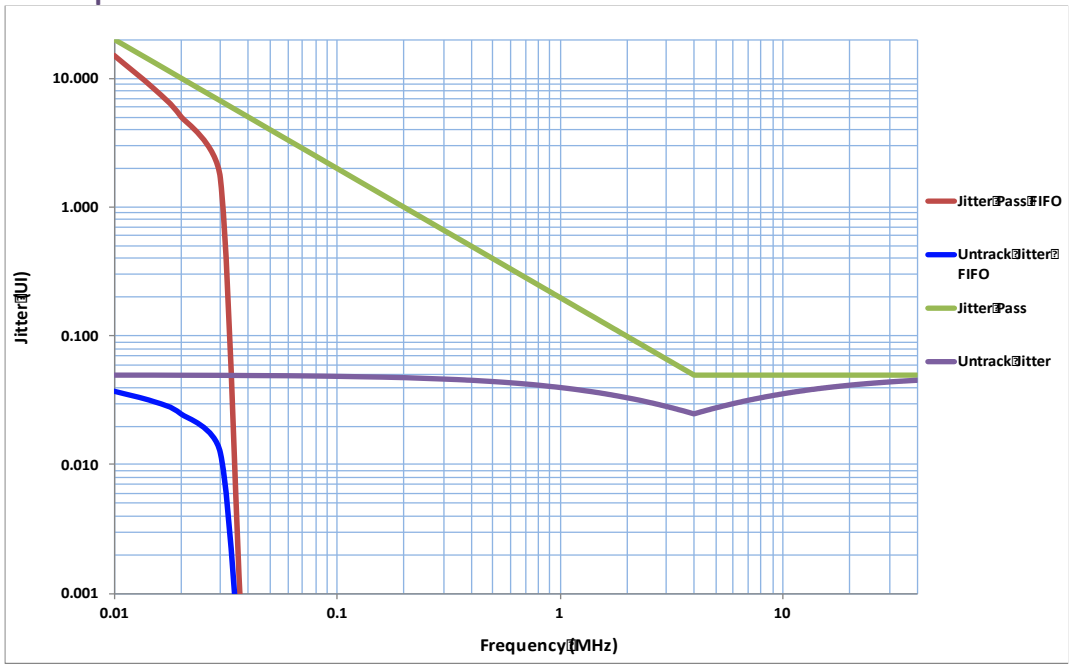
PMA-PMA Jitter Transfer and Penalty

- **PMA-PMA implementations such as BW, peaking, and FIFO has significant impact on jitter transfer**
  - With benign signal applied to xAUI-n penalties to jitter from xAUI-n and jitter peaking are masked from TDECQ/FRx
  - For detail of jitter transfer graphs below see ghiasi_3cd_01_0118 .

Red Line for case of 2:1 Mux Jitter Doubling
Blue 1:1 PMA-PMA Jitter Transfer



Red Line for case of 2:1 Mux Jitter Transfer with FIFO
Orange 1:1 PMA-PMA Jitter Transfer
Purple Untrack Jitter for 2:1 PMA with FIFO

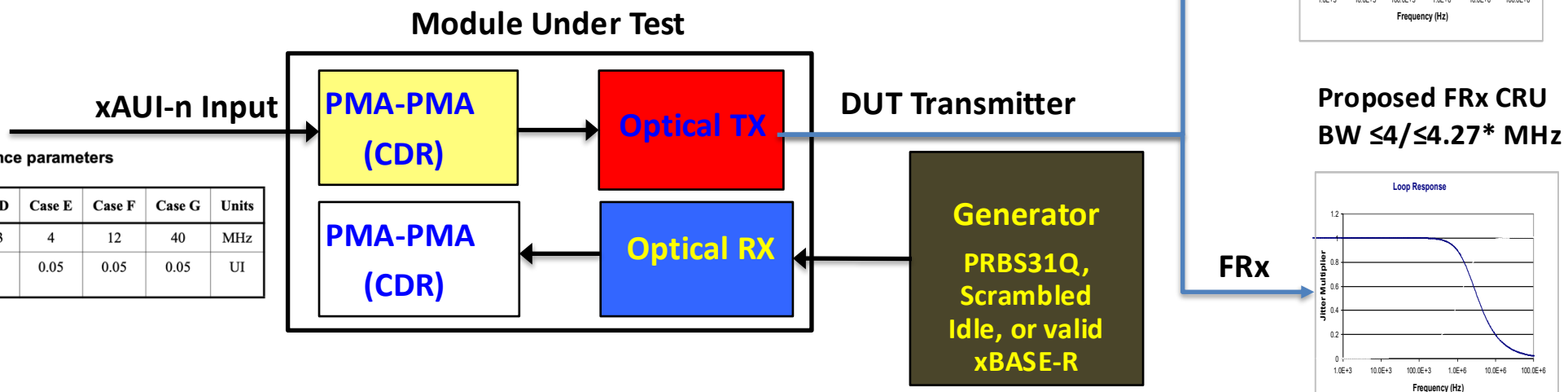


Current TDECQ/FRx Jitter Shortcoming

- **Module under test TECQ/TDECQ and FRx results are depended on how well DUT test setup captures worst case allowed jitter**
  - The highlighted module PMA-PMA may have variety of responses such as:
    - May have BW <4 MHz
    - May have BW >4 MHz
    - May have few dB's of jitter peaking
    - In case of 2:1 PMA integrated jitter may double
    - May include FIFO where xAUI-n jitter is attenuated
  - Dependeding on the module PMA implementation TECQ/TDECQ/FRx may have sensitivity to one or more of the JTOL test frequences!

Table 176D–12—Receiver jitter tolerance parameters

Parameter	Case A	Case B	Case C	Case D	Case E	Case F	Case G	Units
Jitter frequency	0.04	0.1333	0.4	1.333	4	12	40	MHz
Jitter amplitude (peak-to-peak)	5	1.5	0.5	0.15	0.05	0.05	0.05	UI



* CRU BW for clauses 180/181 is 4 MHz and for clauses 182/183 4.27 MHz.

Proposed Remedy See comments 124, 125, 126, 127, 128

- **Add following sentence to include JTOL test condition to 180.9.6, 180.9.9, 181.9.6, 182.9.6, 183.9.6**
  - For those cases there is a xAUI-n chip-to-module (C2M) interface TDECQ must be met with Module stressed input condition in 176D.8.14 for 200 Gb/s AUI and in 120G.3.4.3 for 100 Gb/s AUI
- **The proposed remedy did not want to require testing at all 8 JTOL test frequencies**
  - Generally, for a given DUT PMA/Module one of the JTOL frequencies may result in maximum penalty at TP2
  - Manufacture may choose to test at one frequency or may determine even testing without the JTOL condition present for a specific PMA-PMA device there is negligible jitter transfer penalty .

Summary

- **In D1.4 the task force for first time added requirement that TDECQ clock is derived from x-AUI-n PMA and added counter propagating optical crosstalk for the DUT module**
  - A significant step in the right direction
- **The Task Force has been investigating how to best capture jitter penalties for the past 1.5 years**
  - Unless worst case jitter transfer is captured during TDECQ and FRx tests a major hole remains in the specifications
- **The DUT x-AUI-n need to operate with JTOL conditions for TDECQ and FRx to capture the penalty associated with worst case jitter that is allowed in the system!**

Thank You!