

Aligning specifications to module insertion loss allocation

(comments #58 and #60)

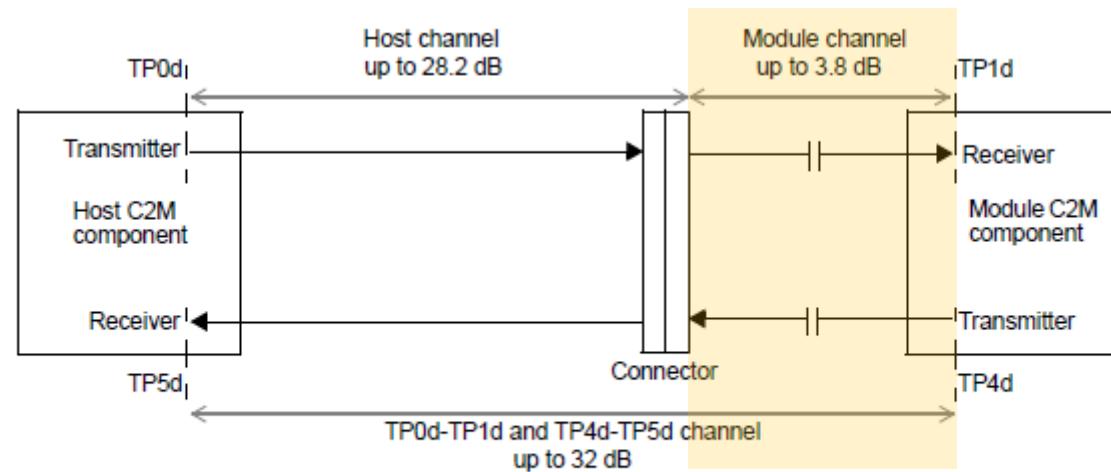
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IEEE P802.3dj Task Force

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Chip-to-module reference insertion loss budget

- The D2.3 reference insertion loss budget allocates 3.8 dB to the module
- This allocation is from the mating point of the MDI connector to TP1d or TP4d (it includes the module device package)
- Note that the reference insertion loss of a host compliance board is also 3.8 dB
- Some module specifications in D2.3 are not consistent with this insertion loss allocation



NOTE—For loss budgeting purposes, the host channel loss is from TP0d to the center of the edge connector of the module.

Figure 176D-6—Reference insertion loss budget at 53.125 GHz

D2.3 interference tolerance test calibration

176D.8.13.2 Test channel calibration

The COM of the test channel is calculated using the method defined in Annex 178A and the parameters of 176D.7.2, with the following considerations:

- a) For the host test, the test channel is measured between the Tx and Rx test references shown in Figure 176D-7b, and COM is calculated using the partial host channel, device package, and device termination models in Table 176D-6 for the receiver S-parameter model.
- b) For the module test, the test channel is measured between the Tx and Rx test references shown in Figure 176D-8b, and COM is calculated using the module device package and device termination models in Table 176D-6 for the receiver S-parameter model. Calculation is performed for both case 1 and case 2 of the package transmission line 1 length, and the value of COM is taken as the lower of the two calculated values.

Table 176D-11—Interference tolerance test parameters

Parameter	Host test	Module test L (low loss) ^a	Module test H (high loss)	Units
Test channel insertion loss at 53.125 GHz	9 ± 2	9 ± 2	32 ± 0.5	dB

Table 176D-6—Host and module model parameters (continued)

Parameter	Symbol	Value	Units
Device package model, module			
Transmission line parameter γ_0	γ_0	5×10^{-4}	1/mm
Transmission line parameter a_1	a_1	8.9×10^{-4}	ns ^{1/2} /mm
Transmission line parameter a_2	a_2	2×10^{-4}	ns/mm
Transmission line parameter τ	τ	6.141×10^{-3}	ns/mm
Transmission line 1 length, case 1	$z_p^{(1)}$	4	mm
Transmission line 1 length, case 2	$z_p^{(1)}$	10	mm
Transmission line 1 characteristic impedance	$Z_c^{(1)}$	87.5	Ω
Transmission line 2 length	$z_p^{(2)}$	1.8	mm
Transmission line 2 characteristic impedance	$Z_c^{(2)}$	92.5	Ω
Single-ended package capacitance at package-to-board interface	C_p	40×10^{-6}	nF

Host input calibration

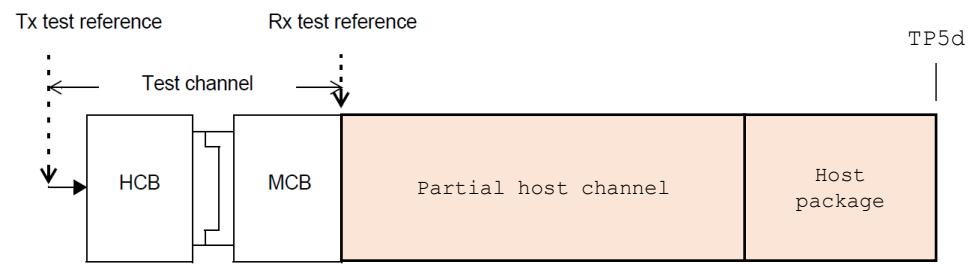
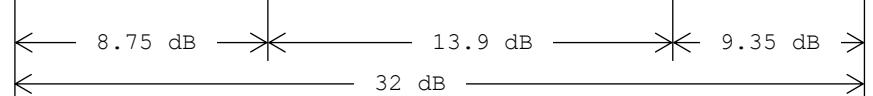
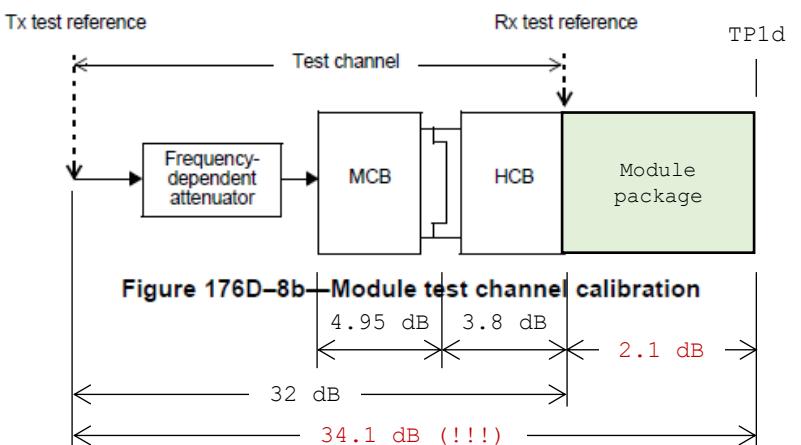


Figure 176D-7b—Host test channel calibration



Module input calibration



Assumed module loss is too high!

Correction to interference tolerance test calibration

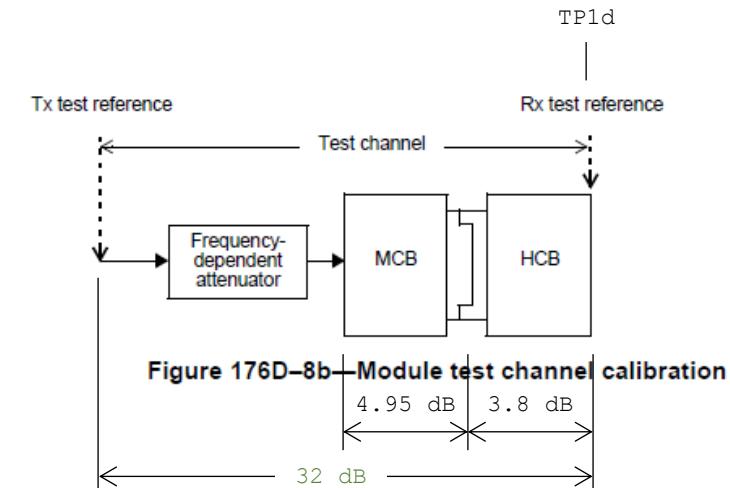
176D.8.13.2 Test channel calibration

The COM of the test channel is calculated using the method defined in Annex 178A and the parameters of 176D.7.2, with the following considerations:

- For the host test, the test channel is measured between the Tx and Rx test references shown in Figure 176D-7b, and COM is calculated using the partial host channel, device package, and device termination models in Table 176D-6 for the receiver S-parameter model.
- For the module test, the test channel is measured between the Tx and Rx test references shown in Figure 176D-8b, and COM is calculated using the ~~module device package and device termination models~~ in Table 176D-6 for the receiver S-parameter model. ~~Calculation is performed for both case 1 and case 2 of the package transmission line 1 length, and the value of COM is taken as the lower of the two calculated values.~~

Table 176D-11—Interference tolerance test parameters

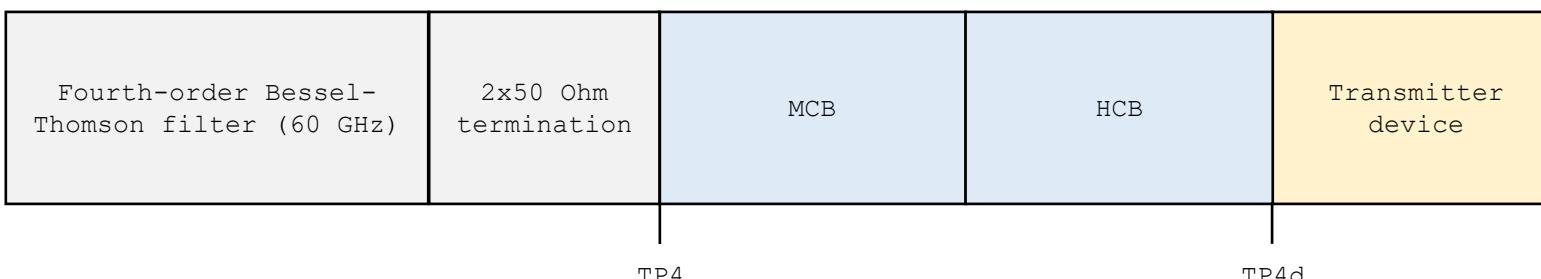
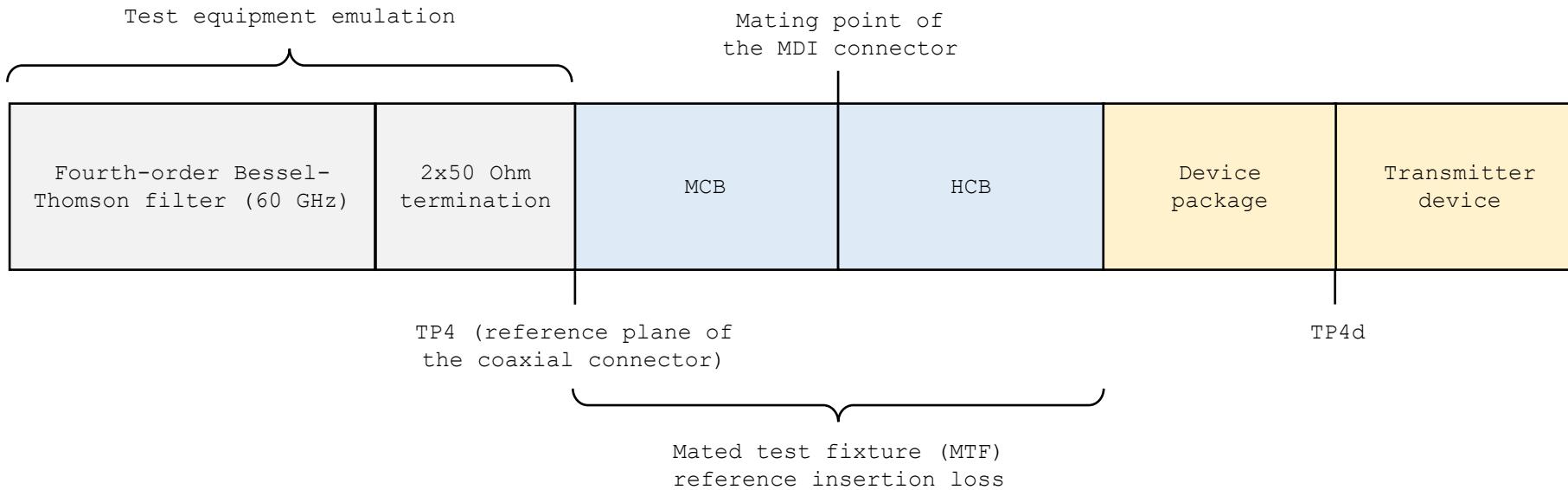
Parameter	Host test	Module test L (low loss) ^a	Module test H (high loss)	Units
Test channel insertion loss at 53.125 GHz	9 ± 2	9 ± 2	32 ± 0.5	dB



Module output R_{peak} and v_f

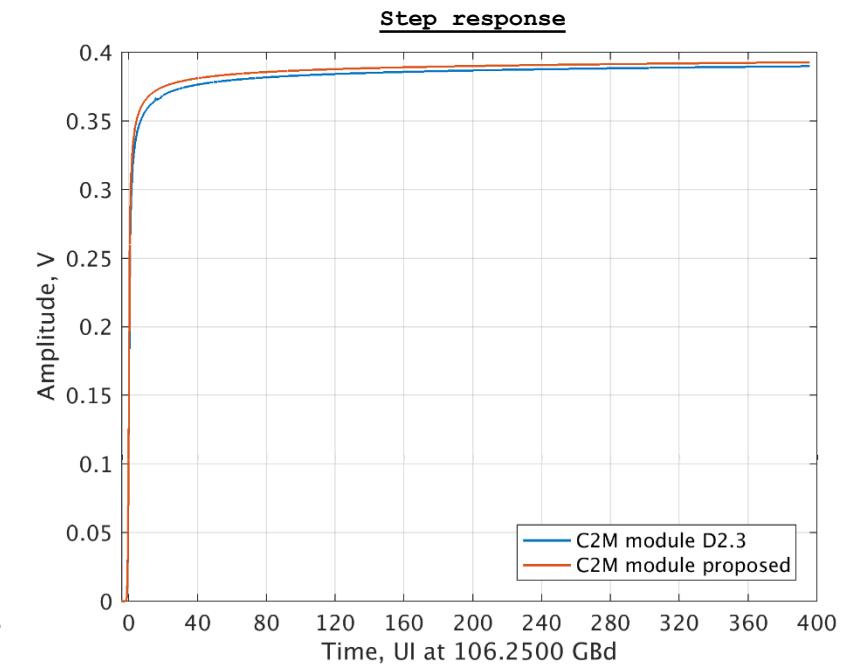
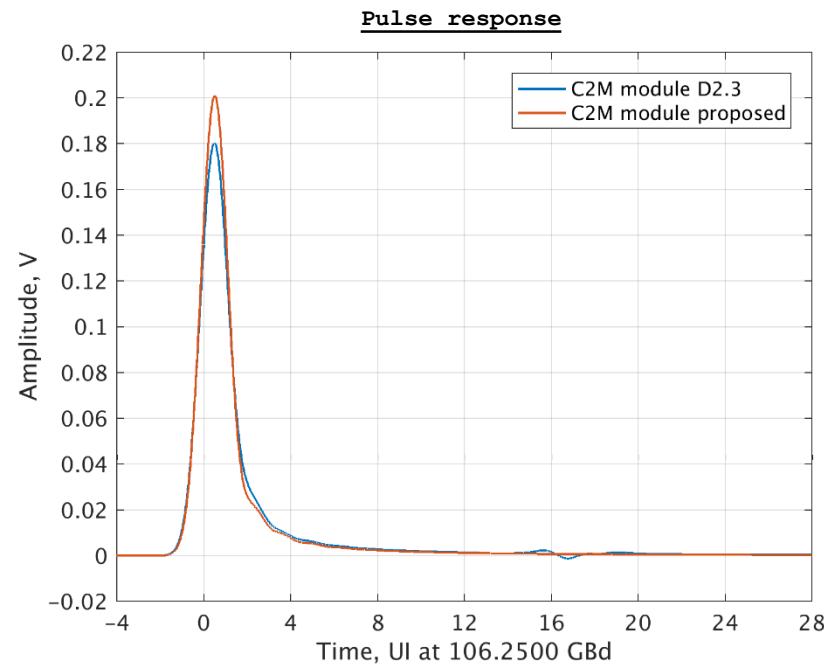
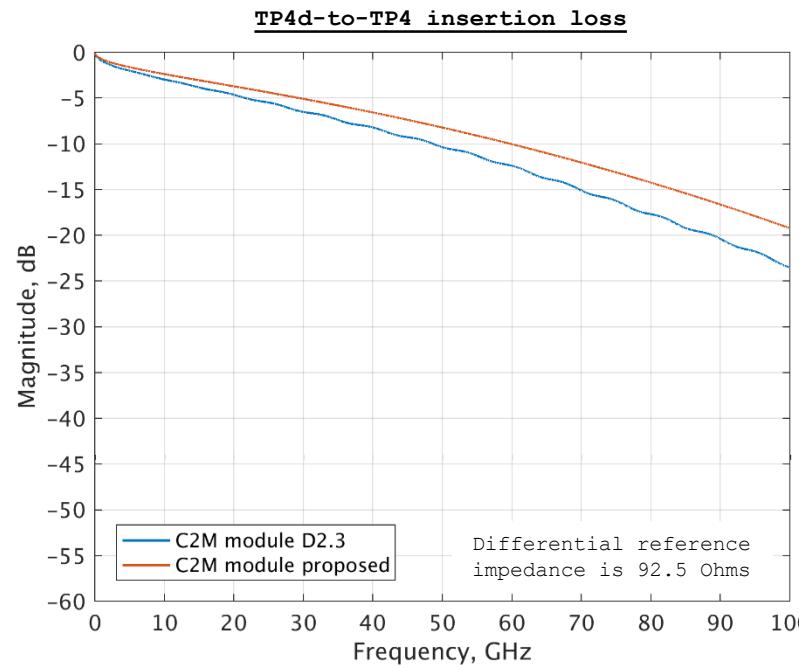
- In [healey_3dj_01a_2511](#), module output specification limits were derived from the Channel Operating Margin (COM) model of a module transmitter and the mated test fixture reference insertion loss
- Limits were computed with a module device package model in addition to the host compliance board
- This was consistent with the interference tolerance test calibration but not consistent with the module loss allocation
- If the interference tolerance test calibration is corrected, then the module output specification limits should also be revisited

Model of a module transmitter



Note that the transmitter device model includes the device termination model and the input rise time filter

Specification limits recalculated using the corrected model



Case	Package		Insertion loss, dB			p_{max} , v	v_f , v	R_{peak}
	Class	Length, mm	Mated test fixture	TP4d-to-TP4				
C2M module, D2.3	A	10	8.75	10.82		0.179	0.389	0.46
C2M module, proposed	n/a	n/a	8.75	8.75		0.2	0.392	0.51

Corrected specification limits

Recommendations

- Remove module device package model from module interference and jitter tolerance test calibration
- Update module output R_{peak} and v_f limits to be consistent with its insertion loss allocation