176.10 - Path data delay for time synchronization

Andras de Koos – Microchip Technology

IEEE 802.3dj Task Force

The path data delay calculation instructions in 176.10 are incomplete

The path data delay is meant to reflect a PHY layer's in-to-out delay. But when the delay through the PHY layer is not constant, we need a convention so that each end of the PTP link is consistent.

As explained in Clause 90, each PHY layer should report its path data delay as the delay of the bit that has the longest delay on Tx and shortest delay on Rx (guaranteed to be the same bit). The text in the new PHY clauses seeks to spell out which bit this is.

Current text in D3.0 176.10:

"The transmit and receive path data delays are reported as if the DDMP (data delay measurement point) occurs on an odd PCS lane (see 90.7). "

The 2CW odd PCS lane delay does dominate for 8:1 and 16:2 PMAs, but the text above is missing the contribution of the symbol-pair (or symbol-quartet) interleave.

What bit has the longest delay (Tx) through the PMA?

Clearly, the symbol-pair interleave (or symbol quartet interleave for 1.6T) adds variable delay.

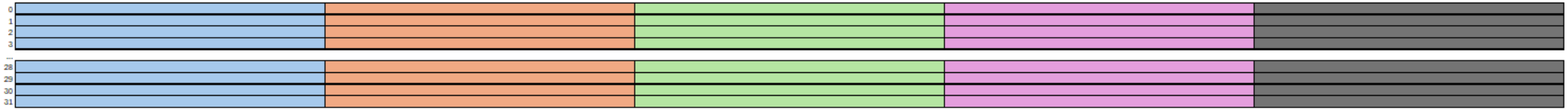
The last symbol pair within an 8:1 symbol pair interleave within a PMA lane has 140 bits (~650ps) more delay than the first symbol pair.

Also, for odd PCS lanes (which have an extra 1-symbol delay on each PCS lane), odd symbols are pushed into the *next* 8:1 symbol interleave sequence. So odd symbols can have as much as 150+140= 290 bits difference (~1360ps) through the 8:1 PMA symbol pair round-robin interleave function.

So specifying which bit to report the path data delay is worthwhile!

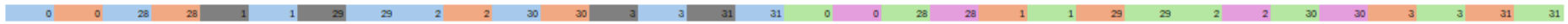
Symbol-pair interleave Illustration (32:4) SM-PMA

PCS lanes arrive aligned



Odd lanes are delayed by 1 symbol

Output PMA lane is formed by multiplexing symbol pairs from 8 PCS lanes.



Notice how symbols that arrived aligned are scattered through the symbol pair round-robin interleave sequence.

Suggested Remedy

Change the following paragraph in 176.10 from:

The transmit and receive path data delays are reported as if the DDMP (data delay measurement point) occurs on an odd PCS lane (see 90.7).

To:

For 8:1, 16:2, 32:4, 1:8, 2:16, and 4:32 SM-PMAs, the transmit and receive path data delays are reported as if the DDMP (data delay measurement point) occurs on the first bit of the last odd-PCS-lane symbol-pair within an 8:1 symbol-pair round-robin interleave sequence, across all PMA lanes.

For 16:8 and 8:16 SM-PMAs, the transmit and receive path data delays are reported as if the DDMP (data delay measurement point) occurs on the first bit of the last PCS-lane symbol-quartet within a 2:1 symbol-quartet interleave sequence.

For 1:1, 2:2, 4:4, 8:8 and 16:16 SM-PMAs, the transmit and receive path data delays are reported as if the DDMP (data delay measurement point) occurs on an arbitrary bit.

See 90.7 for more information.

Thanks!