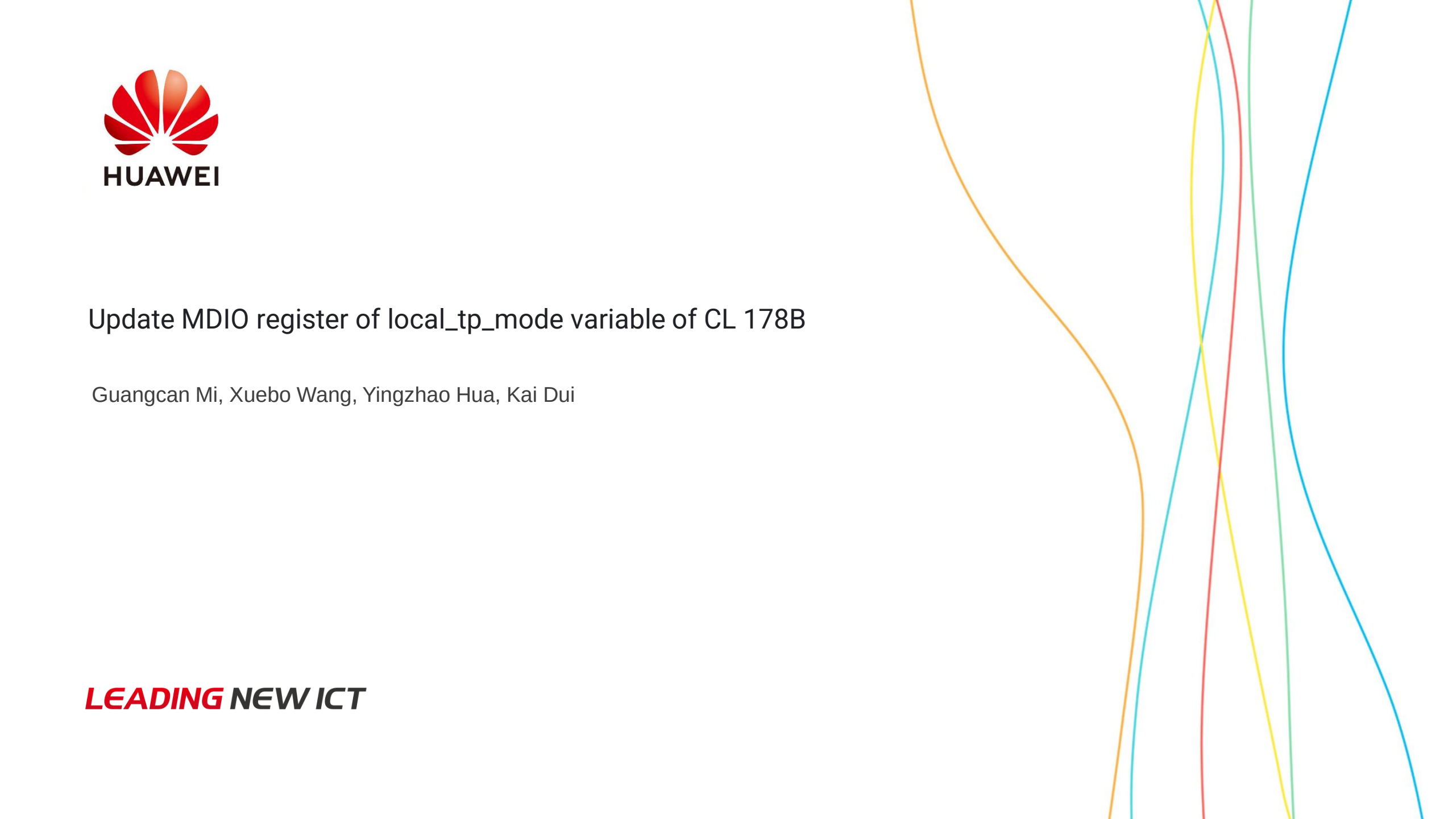

Update MDIO register of local_tp_mode variable of CL 178B

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Introduction

- Local_tp_mode is a variable of ILT state diagram. An MDIO register is mapped to this variable. However the mapping seems to be mismatching the meaning of the variable.
- A proposal of updating the MDIO mapping of the local_tp_mode is provided in this contribution.
- A similar case was found in 802.3ck.

Current mapping

178B.7.9 Training pattern setting

When a change to the received modulation and precoding request bits or the training pattern request bits is detected, the transmitted training pattern (see 178B.7.3.3) is set accordingly. To confirm that the change to the format of the training pattern was completed, the local_mc_mode variable is set to the value of the received modulation and precoding request bits and the local_tp_mode variable to the value of the received training pattern request bits. local_mc_mode and local_tp_mode are encoded in status fields (see 178B.7.5.2 and 178B.7.5.3).

local_tp_mode <= received LP training pattern request
local_tp_mode => local Training Frame status field

local_tp_mode	178B.7.5.3	1.1320.6:5[c]	45.2.1.165

[a] MDIO register/bit numbers and references are for the lower AUI component or PMD. The MDIO register/bit numbers and references for the upper AUI component are at +4000 offset.

Relates to local device control, indicates the Control field in the Training Frame sent from LD, the training pattern request bit is meant for LP

45.2.1.165 BASE-R PAM4 PMD training LD control, lane 0 through lane 3 registers (Register 1.1320 through 1.1323)

The BASE-R PAM4 PMD training LD control, lane 0 through lane 3 registers reflect the contents of the control field of the outgoing training frame for each lane. Lane 0 maps to register 1.1320, lane 1 maps to register 1.1321, lane 2 maps to register 1.1322, and lane 3 maps to register 1.1323.

Table 45–131—BASE-R PAM4 PMD training LD control, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1320.15:14	Reserved	Value always 0	RO
1.1320.13:11	Initial condition request[b]	13 12 11 1 1 1 = Reserved 1 0 1 = ~~Reserved~~ Preset 6 0 1 1 = Preset 5 0 0 1 = Preset 4 1 1 0 = Preset 3 1 0 0 = Preset 2 0 1 0 = Preset 1 0 0 0 = Individual coefficient control	R/W
1.1320.10	~~Reserved~~ Continue training	~~Value always 0~~ 1 = Continue training 0 = Switch to data when training is completed	~~RO~~ R/W
1.1320.9:8	Modulation and precoding request	9 8 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	R/W
1.1320.7~~:5~~	Reserved	Value always 0	RO
1.1320.6:5	Training pattern request	6 5 1 1 = Free-running PRBS31 1 0 = Reserved 0 1 = Free-running PRBS13 0 0 = Synchronous PRBS13	R/W

Same chain of thought applies to local_mc_mode

Related mapping – local_tp_mode

local_tp_mode <= received LP training pattern request
local_tp_mode => local Training Frame status field

Option A:
1.1120, Control information received from Link Partner, i.e., received LP training pattern request, where local_tp_mode get its value from.

45.2.1.161 BASE-R PAM4 PMD training LP control, lane 0 through lane 3 registers (Register 1.1120 through 1.1123)

The BASE-R PAM4 PMD training LP control, lane 0 through lane 3 registers reflect the contents of the first 16-bit word of the training frame most recently received for each lane. Lane 0 maps to register 1.1120, lane 1 maps to register 1.1121, lane 2 maps to register 1.1122, and lane 3 maps to register 1.1123.

The assignment of bits in the BASE-R PAM4 PMD training LP control, lane 0 register is shown in Table 45–129. The assignment of bits in the registers for lane 1 through lane 3 is equivalent to the assignment for lane 0. When training is not disabled, the bits in registers 1.1120 through 1.1123 are read only; however, when training is disabled the R/W bits become writeable.

Option B:
1.1420, Status field of the training frame sent from local device, local_tp_mode determines the value of the status field bit.

45.2.1.167 BASE-R PAM4 PMD training LD status, lane 0 through lane 3 registers (Register 1.1420 through 1.1423)

The BASE-R PAM4 PMD training LD status, lane 0 through lane 3 registers reflect the contents of the status field of the outgoing training frame for each lane. Lane 0 maps to register 1.1420, lane 1 maps to register 1.1421, lane 2 maps to register 1.1422, and lane 3 maps to register 1.1423.

The assignment of bits in the BASE-R PAM4 PMD training LD status, lane 0 register is shown in Table 45–132. The assignment of bits in the registers for lane 1 through lane 3 is equivalent to the assignment for lane 0.

Preferred by the authors

Same chain of thought applies to local_mc_mode

Proposed change to 802.3dj D3.0

local_mc_mode	178B.7.5.2	1.1320.9:8[c]	45.2.1.165
local_tp_mode	178B.7.5.3	1.1320.6:5[c]	45.2.1.165

[a] MDIO register/bit numbers and references are for the lower AUI component or PMD. The MDIO register/bit numbers and references for the upper AUI component are at +4000 offset.

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1.1420.11:10

45.2.1.167

1.1420.13:12

Change Table 45–132 (as amended by IEEE Std 802.3ck-2022) as follows:

Table 45–132—BASE-R PAM4 PMD training LD status, lane 0 register bit definitions

Bit(s)	Name	Description	R/W[a]
1.1420.15	Receiver ready	1 = Training is complete and the receiver is ready for data 0 = Request for training to continue	RO
1.1420.14~~:12~~	Reserved	Value always 0	RO
1.1420.13:12	Training pattern status	13 12 1 1 = Free-running PRBS31 1 0 = Reserved 0 1 = Free-running PRBS13 0 0 = Synchronous PRBS13	RO
1.1420.11:10	Modulation and precoding status	11 10 1 1 = PAM4 with precoding 1 0 = PAM4 0 1 = Reserved 0 0 = PAM2	RO

Similar issue in 802.3ck and CL136 of 802.3 base standard

136.8.11.5 Modulation and precoding setting

When a change to the modulation and precoding request bits is detected, the modulation and precoding mode of the transmitted training pattern (see 136.8.11.1.3) is set accordingly, and the local_tp_mode variable is then set to the value of the modulation and precoding request bits to confirm that the change to the format of the training pattern was completed. local_tp_mode is encoded in the status field (see 136.8.11.3.2).

local_tp_mode

Enumerated variable that controls the modulation and precoding mode in the transmitted training pattern (see 136.8.11.1.3) and may be assigned one of the following values: pam2, pam4, pam4 with precoding.

Table 162–7—MDIO/PMD control function mapping *(continued)*

MDIO variable	PMA/PMD register name	Register/bit number	PMD variable
Seed	PMD training pattern, lanes 0 to 3	1.1450.15:14 1.1450.10:0[b]	seed_i
Initial condition request	BASE-R PAM4 PMD training LP control, lanes 0 to 3	1.1120.13:12[b]	ic_req
Coefficient select	BASE-R PAM4 PMD training LP control, lanes 0 to 3	1.1120.4:2[b]	coef_sel
Coefficient request	BASE-R PAM4 PMD training LP control, lanes 0 to 3	1.1120.1:0[b]	coef_req
Receiver ready	BASE-R PAM4 PMD training LP status, lanes 0 to 3	1.1220.15[b]	remote_rx_ready
Modulation and precoding status	BASE-R PAM4 PMD training LP status, lanes 0 to 3	1.1220.11:10[b]	remote_tp_mode
Receiver frame lock	BASE-R PAM4 PMD training LP status, lanes 0 to 3	1.1220.9[b]	remote_tf_lock
Modulation and precoding request	BASE-R PAM4 PMD training LD control, lanes 0 to 3	1.1320.11:10[b]	local_tp_mode

- Defined in CL 136,
- not mapped to MDIO in CL 136.
- Assigned MDIO register in CL162

THANK YOU

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