Capturing Jitter Penalty During TDECQ and TFSEH Tests (comments I-259, I-260, I-261, and I-262)

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IEEE 802.3dj Interim Meeting
Munich

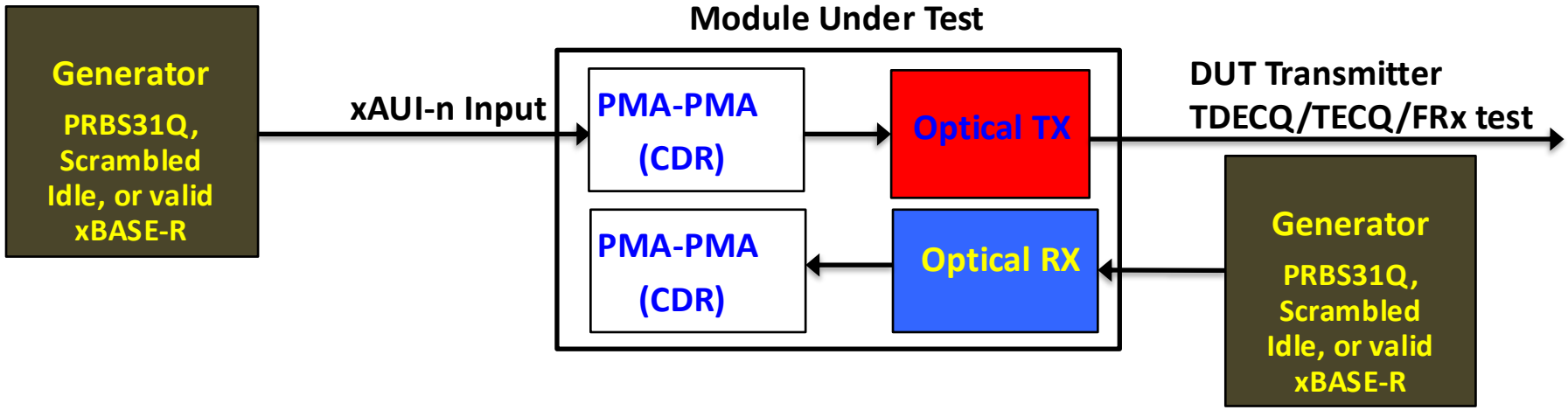
May 11, 2026

Background

- **Prior to DJ project TDECQ was defined with local SSPRQ pattern from the module ignoring jitter through the module and without counter propagating crosstalk traffic**
  - In D1.4 when xAUI-n is accessible the clock source for SSPRQ test pattern is derived from xAUI-n input
  - Also added in D1.4 was asynchronous crosstalk test pattern to optical receive input
- **Changes made in D1.4 were in the right direction**
  - Unless the test include the worst case xAUI-n input jitter TDECQ and Functional Receiver FRx will not capture problematic transmitter with high jitter
  - An xAUI-n driven from a clean generator will not transfer any jitter from xAUI-n input to TP2!

Current TECQ/TDECQ/TFSEH Jitter Shortcoming

- **Current DJ draft short coming is that xAUI-n may be a benign generator, therefore TECQ/TDECQ/TFSEH measurement will not include any host contributed jitter transfer!**
  - Annex 176D xAUI-n CDR corner frequency is 4 MHz.



xAUI-n Input Must Operate with Maximum Allowed Jitter

- **Clause 176D 200G xAUI-n jitter tolerance requirements are given by Table 176D-12**
  - Jitter in table 176D-12 when applied to an x-AUI-n 200G PMA can result in following jitter propagating to TP2
    - Integrated output jitter can be *0.05 UI* for an ideal single loop 4 MHz CDR with zero jitter peaking
    - Integrated output jitter can be *> 0.05 UI in for a single loop 4 MHz CDR with some jitter peaking*
    - Integrated output jitter can be *<0.05 UI* for a dual loop CDR with FIFO that include jitter filter
    - Integrated output jitter can be *<0.05 UI* for a single loop <4 MHz CDR but the PMA may contribute to BLER
  - Considering a typical eye opening of just ~0.2 U at TP2 the addition of 0.05 to 0.1 UI can add significant penalty to reported TECQ/TDECQ/TFSEH!

Table 176D–12—Receiver jitter tolerance parameters

Parameter	Case A	Case B	Case C	Case D	Case E	Case F	Case G	Units
Jitter frequency	0.04	0.1333	0.4	1.333	4	12	40	MHz
Jitter amplitude (peak-to-peak)	5	1.5	0.5	0.15	0.05	0.05	0.05	UI

Optical Receivers Must Operate with Maximum Allowed Jitter

- **Optical receiver conformance test is part of SRS validation and defined in clause 121.8.9.4**
  - 802.3dJ PMDs with non-inner FEC have 4 MHz corner frequency
  - 802.3dJ PMDs with inner FEC have 4.27 MHz corner frequency
- **A typical 200G DSP implementation using SAR ADC has significant delay in the CDR where CDR BW may be < 4 MHz**
  - A module that passes TDECQ and TFSEH (Transmitter Functional Symbol Error Histogram) tests that wasn't test with worst case xAUI-n input jitter when deployed into the system may have excessive jitter resulting in BLER or link flaps
  - The worst part is that both TDECQ and TFT tests can pass given current transmitter test set up but fail in system!

Table 121–12—Applied sinusoidal jitter

Frequency range	Sinusoidal jitter, peak-to-peak (UI)
$f < 40$ kHz	Not specified
40 kHz $< f \leq 4$ MHz	$2 \times 10^5 / f$
4 MHz $< f <$ 10 LB[a]	0.05

[a] LB = loop bandwidth; upper frequency bound for added sine jitter should be at least 10 times the loop bandwidth of the receiver being tested.

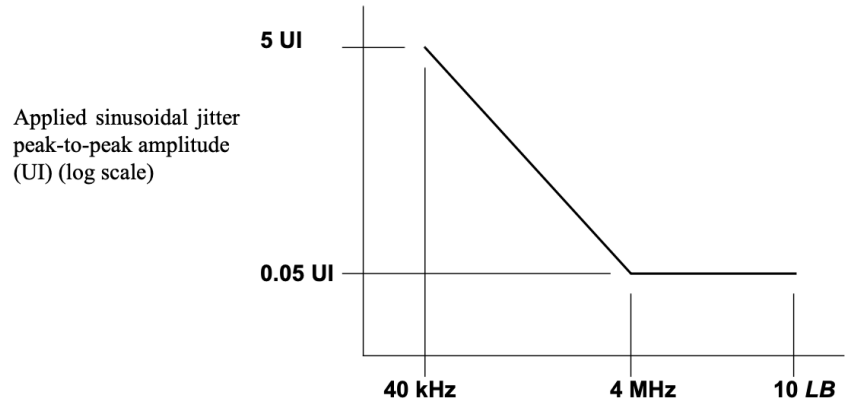


Figure 121–7—Illustration of the mask of the sinusoidal component of jitter tolerance

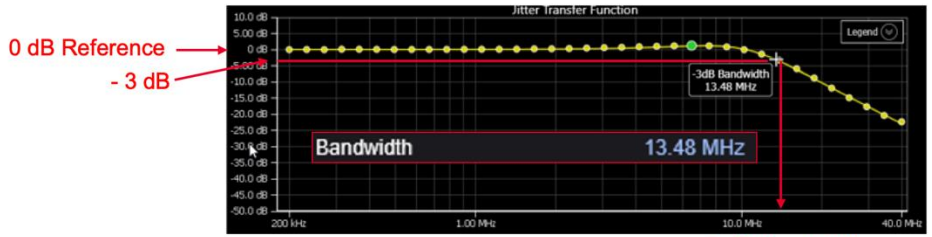
Wide Variety of CDR Implementations

- **Jitter Transfer Function (JTF) of several 56 GBd CDR's were investigated by calvin_3dj_01a_2411**
  - Single loop CDR had a BW of 13.48 GHz with 1.37 dB peaking – good tracking but passes all problem downstream
  - The dual-loop CDR input JTOL corner was 2 MHz but the jitter transfer BW was 42 kHz – great for jitter transfer but JTF corner frequency of 2 MHz may result in BLER on the AUI interface.

PLL Bandwidth and Peaking

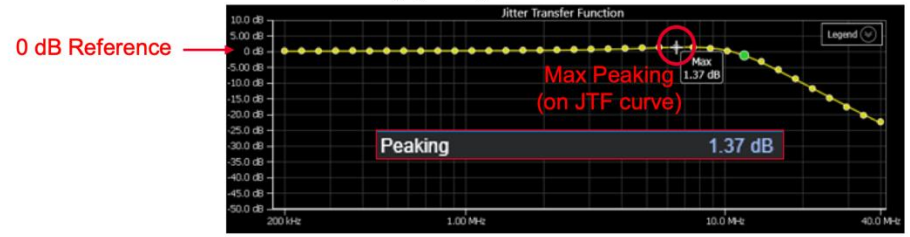
Standards typically specify PLL bandwidth and peaking (measured on the Jitter Transfer Function)

- PLL 3dB Bandwidth



- 3 dB Bandwidth (on JTF curve)

- PLL Peaking (max)



KEYSIGHT

TP1a->TP2 (Electro-Optic) JTF is observed when the reference modulator is replaced with an actual 800G Transceiver.

- The JTF of a retimed module measured up to 2MHz showing the characteristic PLL response however at frequencies much lower than expected.
- PLL BW is 42Khz in this case. 2 decades lower than specs.
- Low frequency impairments are being directly transferred to the TP2 output. The "instrumentation" performing TDECQ at TP2 is performing analog equivalent 4MHz PLL operations and nominally blind to any impairments to the left of this PLL bandwidth. Discrepancies will be significant.

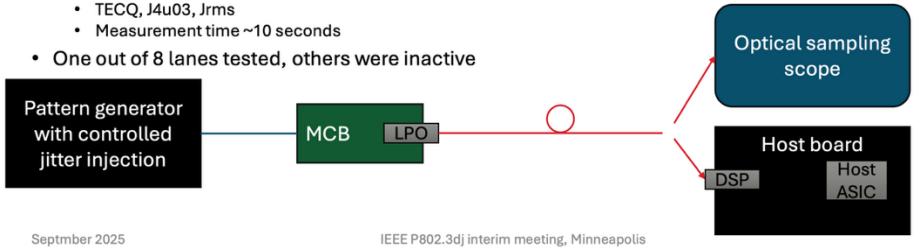
KEYSIGHT

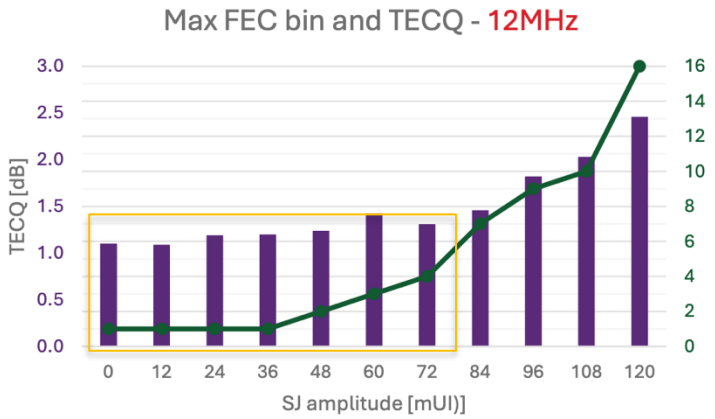
TECQ and TFSEH Results can be Affected by Jitter

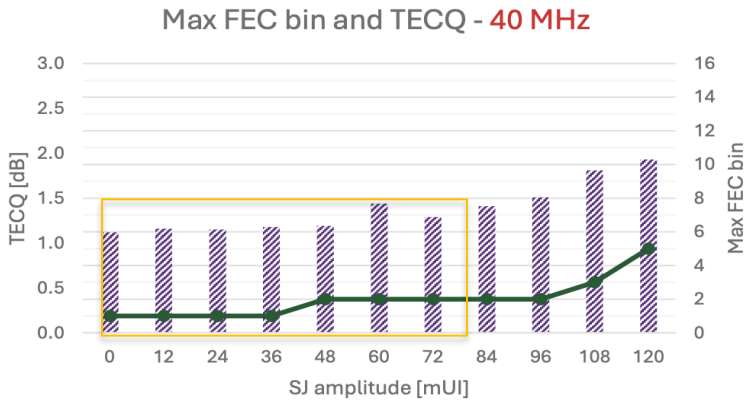
- **Results from ran_3dj_04_2509 below show impact of SJ on TECQ and FEC bins**
  - Test setup below didn't include a CDR which will filter jitter frequencies > 4 MHz assuming an ideal CDR
    - The CDR may have several dB's of peaking around the corner frequency which amplifies the jitter
  - Assuming AUI input is compliant then the integrated SJ for an ideal CDR is 50 mUI, but for non ideal CDR's with some peaking ~80 mUI maybe observed at the output (orange box below)
    - If one look at 12 MHz graph below TECQ can vary from ~1 dB no jitter to ~1.4 dB in the region of interest
    - If one look at 12 MHz graph below FEC bins can vary from single hit to 6 hits
  - The low-probability SER measurable by TFT cannot be measured by TECQ, which is essentially insensitive to probabilities below its defined threshold!

Test setup

- Transmitter:
  - 100GBASE-R + Clause 91 FEC pattern generator
    - Jitter injected: SJ at 12 MHz / 40 MHz, RJ
  - 8x100GBASE-DR1 LPO module (E/O, assumed to have no jitter contribution)
- Channel: ~1m SMF patch cord
- Receiver:
  - Compliant retimed (DSP) 8x100GBASE-DR1 module
  - Compliant host with 800GAUI-8 C2M
  - FEC statistics collected over 30 seconds (~5e8 codewords)
- TP2 Measurements (Keysight DCA, 4 MHz CRU):
  - TECQ, J4u03, Jrms
  - Measurement time ~10 seconds
- One out of 8 lanes tested, others were inactive







Current Test Setup Shortcoming

- **Module under test TECQ/TDECQ and TFSEH results are depended on how well DUT test setup captures worst case allowed jitter**
  - The highlighted module PMA-PMA may have varieties of responses which may include single/dual loop CDRs, jitter peaking, BW < 4 MHz, or BW > 4 MHz
  - Depending on the module TX PMA design the xAUI-n input jitter will have different manifestation at TP2 that can result in additional penalty as observed by ran_3dj_04_2509 results!

Table 176D–12—Receiver jitter tolerance parameters

Parameter	Case A	Case B	Case C	Case D	Case E	Case F	Case G	Units
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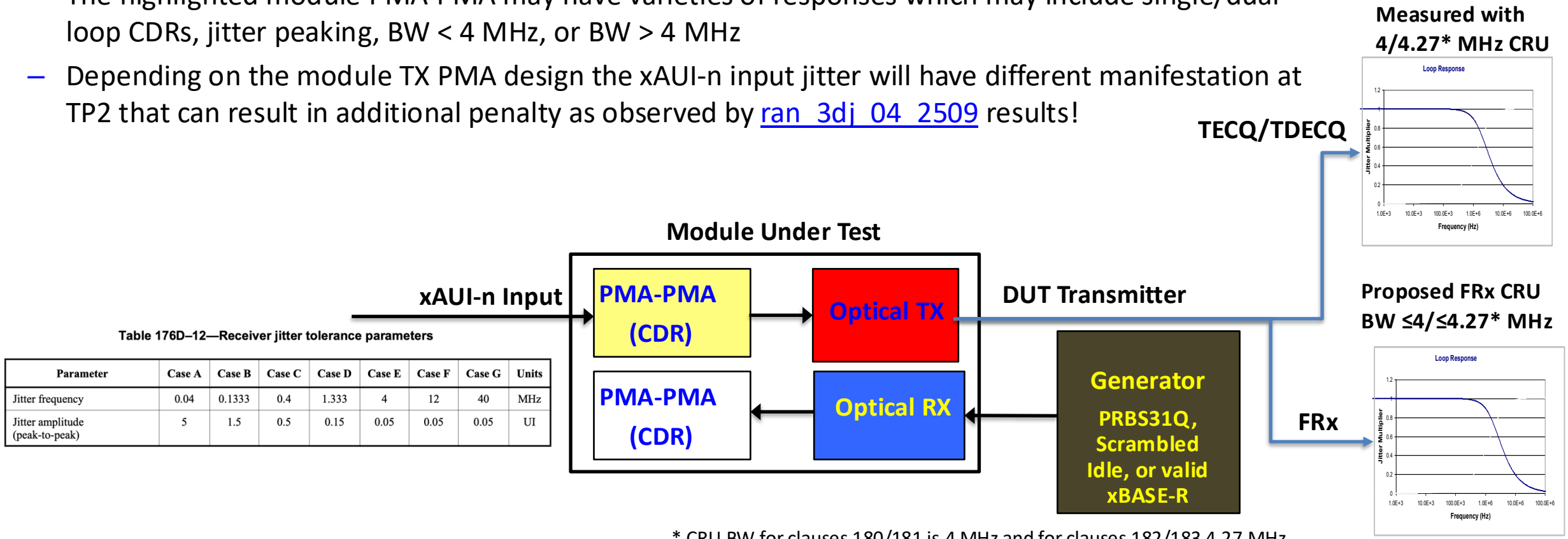

* CRU BW for clauses 180/181 is 4 MHz and for clauses 182/183 4.27 MHz.

Proposed Remedy

- **Add following sentence to include JTOL test condition to 180.9.6, 180.9.9, 181.9.6, 182.9.6, 183.9.6**
  - For those cases where there is an xAUI-n chip-to-chip (C2C) or chip-to-module (C2M) interface (see Table 180–1 through Table 180–4). The xAUI-n input operates with the receiver jitter tolerance signal parameters defined in Annex 176D.8.14 (text to be added to the draft). The clock source for the test pattern is derived from the clock recovered from the xAUI-n input signal. The pattern of the xAUI-n input signal may be PRBS31Q, scrambled idle, or a valid xBASE-R signal.
- **The proposed remedy does not require testing at all 8 JTOL test frequencies**
  - Generally, for a given DUT PMA/Module one of the JTOL frequencies may result in maximum penalty at TP2
  - Note: Manufacturers may select a jitter frequency for manufacturing tests based on device design and DVT considerations, or in some cases, may opt to test without the JTOL condition for specific PMA-PMA designs where jitter transfer penalty is minimal (optionally this note can be added to the draft).

Summary

- **In D1.4 the task force for first time added requirement that TDECQ clock is derived from x-AUI-n PMA and added counter propagating optical crosstalk for the DUT module**
  - This was a significant step in the right direction
  - The Task Force has been investigating how to better capture jitter penalties for the past 1.5 years
- **The DUT optical transmitter xAUI-n input must operate with JTOL conditions in 176D for TECQ/TDECQ and TFSEH tests to capture the penalty associated with worst case xAUI-n jitter that is allowed in the system**
  - ran_3dj_04_2509 data show with zero input SJ the TECQ and post FEC results are significantly better than with some SJ!

Thank You!