

# Proposal to add Cl186 test pattern checkers

Addresses comment 211 against D3.0

Marco Mascitto, Nokia

# Comment

CI 186

SC 186.2.4

P 660

L 1

# I-211

Mascitto, Marco

Infinera Canada Inc., Nokia

*Comment Type*

**TR**

*Comment Status*

**X**

Just as the Transmit function has a Test-pattern generator (subclause 186.2.3.12), there should be a Test-pattern checker subclause to 186.2.4. Figure 186-3 shows both a Test-pattern injection point in the transmit path and a Test-pattern extraction point in the receive path. The Test-pattern checker would be similar in functionality to that in subclause 184.6.2. Support of the subclause could be optional.

*Suggested Remedy*

A presentation that proposes text for this new subclause will be provided.

*Proposed Response*

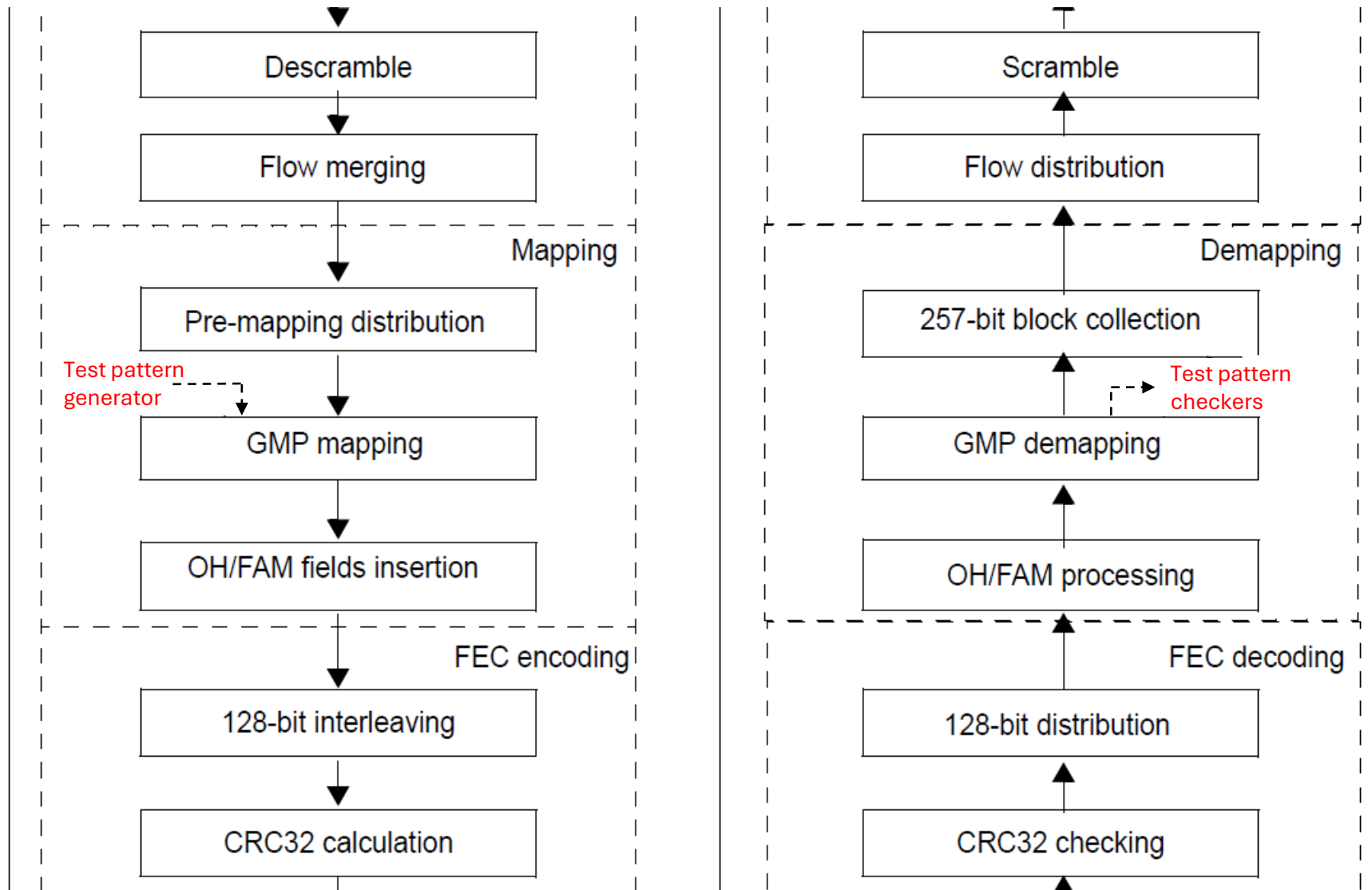
*Response Status*

**O**

# PRBS31 test patterns for ER1

- The PRBS31 test pattern generator operates at a nominal rate of 100.385723 Gb/s (+/- 50 ppm).
- Each output bit from the generator is copied into the eight tributary frame payload areas shown in Figure 186-11.
- There needs to be eight instances of PRBS31 test pattern checkers, one for each FEC flow, operating at that same nominal rate of 100.385723 Gb/s (+/- 50 ppm).

# Proposed change to Figure 186-3



# Proposed text changes (1)

- Modify CL186.2.1 (page 648, line 29):

Replace:

In the receive direction, the 800GBASE-ER1 FEC sublayer synchronization process continually monitors the PMA:IS\_SIGNAL.indication primitive.

With:

**When the receive function is in normal mode**, the 800GBASE-ER1 FEC sublayer synchronization process continually monitors the PMA:IS\_SIGNAL.indication primitive.

# Proposed text changes (2)

- Add a new paragraph to the end of 186.2.1 (page 648, line 41):

When the receive function is in test pattern mode, it operates identically to when it is in normal mode, with the exception that the output of the demapper passes each of the eight FEC flows to an associated pattern checker instance, as described in 186.2.4.11.

# Proposed text changes (3)

- Create a new clause 186.2.4.11, with the following text:

The FEC sublayer shall include eight PRBS31 test pattern checkers, one for each FEC flow presented by the GMP demapper. The group of eight PRBS31 test pattern checkers are enabled by the FEC control variable `rx_test_mode` (set to 1).

For the test configuration illustrated in Figure 174A-2, each PRBS31 test pattern checker instance shall include the block error detection and 17 related counters, as defined in Annex 174A.9.

# Proposed text changes (4)

- Fix typo in Table 186-7: replace FEC\_tx\_test\_mode with tx\_test\_mode.
- Add a new control variable for rx\_test\_mode in Table 186-7.
- Propose using the same control register bits as Cl184.

Control variable	Variable reference	MDIO register/bit number	MDIO register/bit reference
tx_test_mode	186.2.3.12	1.1501.3	45.2.1.170
rx_test_mode	186.2.4.11	1.1501.0	45.2.1.170