

Towards a 200Gbps/Lane High-Loss AUI Baseline Consensus – Status Report

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IEEE P802.3dj Task Force

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Outline

- Background and Introduction
- BER Status Recap
- Loss Target Update
- ☐ Reference Receiver Consideration
- Summary

Background and Introduction

- This presentation will update high-loss AUI baseline directions with adopted DER_0 value, as well as comparing technical characteristics between C2C and C2M in order to proceed
 - BER budget partitioning
 - Loss target consensus building
 - Channel agreement
 - Decision on MLSE
- Goals of this presentation
 - Step towards narrowing the group's focus so that the AUI baseline proposals can proceed
 - Not debating the high-loss AUI specification parameters at this time

BER Status Recap

BER related decision made in motions_3cwdfdj_2305

Motion #8

Move to:

adopt a DERO value of 2.67e-5 (equivalent to measured BER of 4e-5 with precoding ON) as the total allocation for higher-loss AUIs within a PHY (BER division between C2C and C2M as well as the measurement method to be determined later)

M: Adee Ran

S: Kishore Kota

Technical (>=75%) Procedural (>50%)

802.3 voters only

Results: Y: 75, N: 3, A: 20 passed 10:33 a.m.

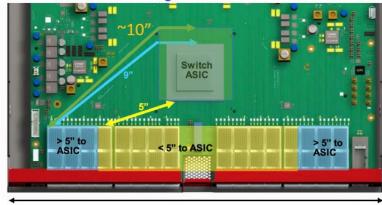
- Can all module cages accommodate host budgets without retimers?
- Is there any other DER₀ combinations?

- 200Gbps/lane AUI DER_0 target options
 - C2M and C2C AUI DER₀ 1.33e-5 → Comparable interface complexity between C2M and C2C
 - C2M and C2C AUI DER₀ 2.67e-5 → ASIC-CDR links should use retimerless systems per Type I PHY

Loss Target Update

- C2M bump-to-bump loss have been updated in oif2023.210
 - Considering high radix system with PCB implementation
 - Worst case loss is a little over 36dB
 - 2/3 of channels have a loss less than 32dB
- C2C loss budget summarized in lit_3dj_01a_2305
 - mellitz_3dj_elec_01_230504 contributed mezzanine channels of TP0-TP5 loss ~20.xdB with a total length of 260mm
 - Total package loss at two sides ~12dB
 - 6-8dB package losses proposed in benartsi 3df 01a 2211, ghiasi 3df 01 220927, and li 3dj 02 2305
 - Bump-to-bump loss ~32dB
 - Do we have consensus on 32dB bump-to-bump IL budget for high-loss C2M and C2C?





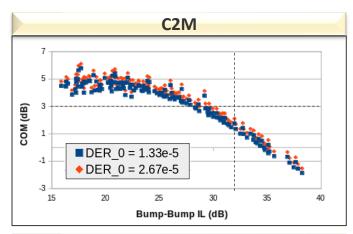
17.1"

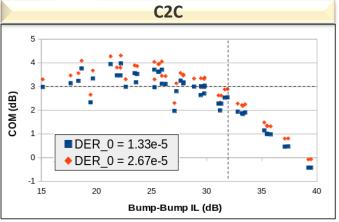
Reference RX Consideration

COM 4.0 used, test channels and spreadsheet in <u>appendix</u>

Parameter	802.3ck C2M	802.3ck C2C	802.3ck CR	802.3ck KR	Exploratory of 802.3dj AUI
DER_0	1E-5	1E-5	1E-4	1E-4	1.33E-5/2.67E-5
SNR_TX	32.5	33	32.5	33	33
R_LM	0.95	0.95	0.95	0.95	0.95
TxFIR Length	4 (2 pre)	5 (3 pre)	5 (3 pre)	5 (3 pre)	6 (4 pre)
eta_0	4.10E-08	2E-08	9E-09	8.2E-09	8.2E-09
N_b	4	6	12	12	24
N_bg	0	0	3	3	6
N_bf	-	-	3	3	3
N_f	-	-	40	40	60
MLSE	-	-	-	-	0

- For 32dB links, EQ length of 24+18 and eta_0 of 8.2e-9 are several time power-consuming than the practical receiver
- MLSE is needed to make most of the channels work, regardless of DER₀ target
 - Are those channels representative and qualified?
 - Should we adopt MLSE as part of ref RX for high-loss AUI?

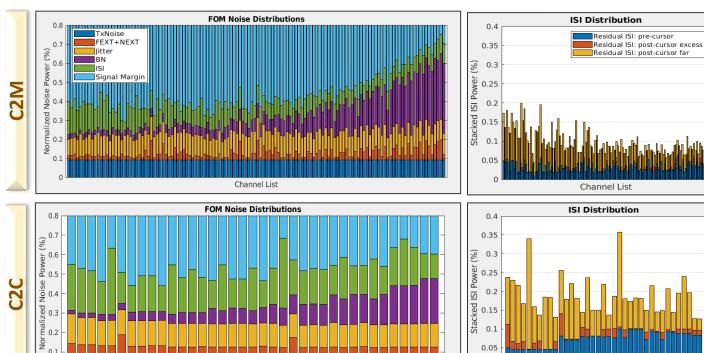


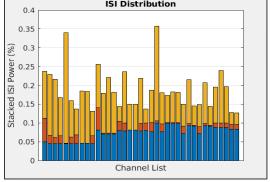


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Noise Distribution

- Medium loss AUI will suffer from reflections
- High loss AUI will suffer from signal swing reduction and noise enhancement
- C2C reflection is generally worse than that of C2M





*DER 0 = 1.33e-5 *Bump-to-bump IL <= 32dB

Channel sorted by IL

Channel List

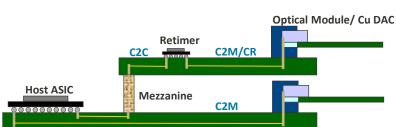
C2M vs C2C Channel Characteristic

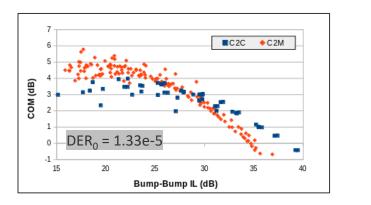
- Different constraints between paddle card for module and the mezzanine card for C2C
- Mezzanine connector is more configurable than a standardized form factor OSFP
- C2C could have two extra vias
- Receiver package assumption
 - C2M channels do not have much reflections near the module device
 - HCB is assumed with ideal T-line loss, instead of actual module design

		C2M	C2C
	z_p (TX)	[15 30; 1 1; 1 1; 0.5 0.5]	[12 31; 1 1; 1 1; 0.5 0.5]
Z_	_p (NEXT)	[8 8; 0 0; 0 0; 0 0]	[11 29; 1 1; 1 1; 0.5 0.5]
Z	_p (FEXT)	[15 30; 1 1; 1 1; 0.5 0.5]	[12 31; 1 1; 1 1; 0.5 0.5]
	z_p (RX)	[8 8; 0 0; 0 0; 0 0]	[11 29; 1 1; 1 1; 0.5 0.5]

Do we agree on channels and endpoint assumptions







Summary

- Loss target for 200Gbps/Lane high loss C2M have been updated from 36dB to 32dB based on channel optimization
- Recommend that 802.3dj C2C shall address the bump-to-bump loss of 32dB
- MLSE is required to make most of the available channels work regardless of DER₀ target
- For an AUI baseline proposal we need to agree on channels and endpoint assumptions
- Next step is to evaluate AUI baseline with updated channels and a proper receiver impairment/margin allocation
 - Plan to have AUI baseline proposal for the July 2023 plenary session
 - Please reach out to us to get involved in the suggested directions of DER₀ target, loss target, and reference receiver

Appendix

Channel List

Application	Contribution			
	akinwale_3df_01_2209			
	akinwale_3df_02_2209			
	akinwale_3df_03_2209			
cana	rabinovich_3df_01_2209			
C2M	rabinovich_3df_02_2209			
	rabinovich_3dj_02_230116			
	rabinovich_3dj_03_230116			
	Shanbhag_3dj_03_2305			
C2C	mellitz_3dj_elec_01_230504			

Example COM Configuration for 200Gbps/L C2M

Table 93A-1 parameters				I/O control			Table 93A-3 parameters		
Parameter	Setting	Units	Information	DIAGNOSTICS	• 0	logical	Parameter	Setting	Units
f b	106.25	GBd		DISPLAY WINDOW	0	logical	package tl gamma0 a1 a2	[0 0.0008455 0.000340225]	51115
f min	0.05	GHz		CSV REPORT	• 0	logical	package tl tau	0.00644805	ns/mm
Delta f	0.01	GHz		RESULT DIR	.\results\CAKR {date}\	logical	package Z c	[92 92 ; 70 70; 80 80; 100 100]	Ohm
C d	[0.4e-4 0.9e-4 1.1e-4;0.4e-4 0.9e-4 1.1e-4]	n.F	[TX RX]	SAVE FIGURES	0	logical	h	[:=:=,:::=;:::=;::::::;	
L s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]	Port Order	[1324]	.eg.ea.	Parameter	Setting	
C b	[0.3e-4 0.3e-4]	nF	[TX RX]	RUNTAG	CAKR_RCos_eval_		board tl gamma0 a1 a2	[0 6,44084e-4 3,6036e-05]	1.5 db/in @ 56G
z_p select	[12]	- 30	[test cases to run]	COM CONTRIBUTION	0	logical	board tl tau	5.790E-03	ns/mm
z p (TX)	[15 30: 1 1 : 1 1: 0.5 0.5]	mm	[test cases]	Operational			board Z c	100	Ohm
z p (NEXT)	[88;00;00]	mm	[test cases]	ERL Pass threshold	9.7	dB	z_bp (TX)	125	mm
z_p (FEXT)	[15 30; 1 1 ; 1 1; 0.5 0.5]	mm	[test cases]	COM Pass threshold	3	db	z bp (NEXT)	0	mm
z p (RX)	[88;00;00;00]	mm	[test cases]	DER 0	1.33E-05	0.0	z_bp (FEXT)	125	mm
PKG Tx FFE preset	0		[Tr	4.00E-03	ns	z_bp (RX)	0	mm
Ср	[0.5e-4 0.5e-4]	ηF	[TX RX]	FORCE TR	1	logical	C 0	[0.2e-4 0]	nF
R 0	50	Ohm	[PMD_type	C2C	8	C 1	[0.2e-4 0]	nF
R d	[50 50]	Ohm	[TX RX]	EW	1		Include PCB	0	logical
A v	0.413	V	vp/vf=	TDR and ERL options		logical		-	
A fe	0.413	v	vp/vf=	TDR	1	logical			
A ne	0.45	v	3.3	ERL	1	logical	Seletions (rectangle, gaussian, dual_ray, leigh, triangle		
	4			ERL ONLY	0	ns	Histogram_Window_Weight	gaussian	selection
м •	32			TR TDR	0.01	35	Or	0.02	UI
filter and Eg				N N	2000	logical	7		3.
f r •	0.75	*fb		TDR_Butterworth	1				
c(0)	0.54		min	beta x	0		IÇN parameters		
c(-1)	[-0.4:0.02:0]		[min:step:max]	rho x	0.618		f v	0.594	Fþ
c(-2)	[0:.02:0.2]		[min:step:max]	TDR W TXPKG	1	UI	ff	0.594	Fb
c(-3)	[-0.04:.02:0]		[min:step:max]	N bx	0	~	f n	0.594	Fb
c(-4)	[0:.02:0.02]		[min:step:max]	fixture delay time	[00]		f 2	79.688	GHz
c(1)	[-0.12:0.02:0.04]		[min:step:max]	Tukey_Window	1		A_ft	0.450	V
N b	24	UI	[типажеринак]	Noise, jitter	-	UI	A nt	0.450	v
b max(1)	0.85	9.	As/dffe1	sigma RJ	0.01	ŬI	7-3	0.150	
b max(2N b)	[0.3 0.2*ones(1,22)]		As/dfe2N b	A_DD	0.02	V^2/GHz	Floating Tap Control		
b min(1)	0		As/dffe1	eta 0	8.20E-09	dB	N bg	6	0 1 2 or 3 groups
b min(2N b)	[-0.2 -0.2*ones(1.22)]		As/dfe2N b	SNR TX	33	u.	N bf	3	taps per group
g_DC	[-20:1:0]	dB	[min:step:max]	R LM	0.95		N f	80	UI span for floating taps
f z	42.5	GHz	[mmszcpmux]		0.75		bmaxg	0.2	max DFE value for floating taps
f p1	42.5	GHz		Enforce Causality	1	1	5090	0.2	max by traide for housing caps
f p2	106.25	GHz		S-parameter magnitude extrapolation policy	trend to DC	_	MLSE	1	logical
g DC HP	[-6:1:0]	U. IL	[min:step:max]	parameter magnitude extrapolation policy			NO.	1	logical
f HP PZ	1.328125	GHz	[nzeepinton]	Filter: RxFEE			Receiver testing		
Butterworth	1	logical	include in fr	ffe_pre_tap_len	0	UI	RX CALIBRATION	0	logical
Raised Cosine	0	logical	include in fr	ffe_post_tap_len	0	ŭi l	Sigma BBN step	5.00E-03	V
RC_Start	6.70E+10		start freq for RCos	ffe_tap_step_size	0	3.	Signa Step	5.532 00	
RC end	7.97E+10	Hz	end freq for RCos	ffe main cursor min	0.7				
o_cild	***************************************	2	cha med for 1003	ffe_pre_tap1_max	0.7				
				fte_post_tap1_max	0.7	_			
				ffe_tapn_max	0.7	-			
				ffe backoff	0.7	-			
				IJE BROOM	+ 0				

Example COM Configuration for 200Gbps/L C2C

Table 93A-1 parameters				I/O control			Table 93A-3 parameters		
Parameter	Setting	Units	Information	DIAGNOSTICS	0	logical	Parameter	Setting	Units
f_b	106.25	GBd		DISPLAY_WINDOW	0	logical	package_tl_gam ma0_a1_a2	[0 0.0008455 0.000340225]	
f_min	0.05	GHz		CSV_REPORT	0	logical	package tl tau	0.00644805	ns/mm
Delta f	0.01	GHz		RESULT DIR	.\results\CAKR_{date}\		package Z c	[92 92 ; 70 70; 80 80; 100 100]	Ohm
C d	[0.4e-4 0.9e-4 1.1e-4;0.4e-4 0.9e-4 1.1e-4]	ηF	[TX RX]	SAVE FIGURES	0	logical			
Ls	[0.13 0.15 0.14; 0.13 0.15 0.14]	nΗ	[TX RX]	Port Order	[1324]		Parameter	Setting	
C b	[0,3e-4 0,3e-4]	nF	[TX RX]	RUNTAG	CAKR_RCos_eval_		board tl gamma0 a1 a2	[0 6,44084e-4 3,6036e-05]	1.5 db/in @ 56G
z p select	[12]	~	[test cases to run]	COM CONTRIBUTION	0	logical	board_tl_tau	5.790E-03	ns/mm
z p (TX)	[13 31; 1 1; 1 1; 0.5 0.5]	mm	[test cases]	Operational			board Z c	100	Ohm
z p (NEXT)	[11 29; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]	ERL Pass threshold	9.7	dB	z_bp (TX)	125	mm
z_p(FEXT)	[13 31; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]	COM Pass threshold	3	db	z_bp (NEXT)	0	mm
z p (RX)	[11 29: 1 1 : 1 1 : 0.5 0.5]	mm	[test cases]	DER 0	1.33E-05		z bp (FEXT)	125	mm
PKG_Tx_FFE_preset	0		[teet emery]	T r	4.00E-03	ns	z_bp (RX)	0	mm
C p	[0.5e-4 0.5e-4]	ηF	[TX RX]	FORCE TR	1	logical	C 0	[0.2e-4 0]	nF
R O	50	Ohm	[PMD type	C2C	5	C 1	[0.2e-4 0]	nF
R d	[50 50]	Ohm	[TX RX]	EW	1		Include PCB	0	logical
A v	0.413	V	vp/vf=	TDR and ERL options	1	logical	madde reb	1	Jogical
A fe	0.413	V	vp/vf=	TDR	1	logical			
A_ne	0.415	V	3×'3-	ERL	1	logical	Seletions (rectangle, gaussian, dual_ray, leigh, triangle		
7_0	4	•		ERL_ONLY	0	ns	Histogram Window Weight	gaussian	selection
<u>й</u> '	32			TR_TDR	0.01	- 50	Or Or	0.02	UI
filter and Eq	32			N N	2000	logical	4	0.02	9'
f r	0.75	*fb		TDR_Butterworth	1	iogicai			
c(0)	0.73	100	min	beta x	0		IÇN parameters		
c(-1)	[-0.4:0.02:0]		[min:step:max]	rho x	0.618		f v	0.594	Fb
c(-1)	[0:.02:0.2]		[min:step:max]	TDR W TXPKG	0.010	UI	f f	0.594	Fb
	[-0.04:.02:0]		[min:step:max]	N bx	0	yı .	f n	0.594	Fb Fb
c(-3) c(-4)	[0:.02:0.02]		[min:step:max]	fixture delay time	[00]		f 2	79.688	GHz
c(-4)	[-0.12:0.02:0.04]			Tukey Window	1			0.450	V GHZ
	[-0.12:0.02:0.04]		[min:step:max]		1		A_ft A_nt	0.450	V V
N_b b max(1)	0.85	ŲΙ	As/dffe1	Noise, jitter	0.01	ŲІ	A_n	0.450	V
b max(2N b)			As/dfe2N b	sigma_RJ	0.02	UI V^2/GHz	Floating Tap Control		
b_max(2N_b) b min(1)	[0.3 0.2*ones(1,22)]		As/dfe2N_b As/dffe1	A_DD eta 0	8.20E-09	dB			0.4.0 2
	ů .		As/dfe2N b			ab	N_bg	6	0 1 2 or 3 groups
b_min(2N_b)	[-0.2 -0.2*ones(1,22)]	JD.		SNR_TX	33 0.95		N_bf N f	3 80	taps per group
g_DC	[-20:1:0]	dB	[min:step:max]	R_LM	0.95			0.2	UI span for floating taps max DFE value for floating taps
f_z	42.5 42.5	GHz		F 5 0 19			bmaxg	0.2	max urt value for floating taps
f_p1	42.5 106.25	GHz		Enforce Causality	1				1
f_p2		GHz	f = 1 = -1	S-parameter magnitude extrapolation policy	trend_to_DC		MISE	0	logical
g_DC_HP	[-6:1:0]	611	[min:step:max]	s'll p ses			B 1 1 1		
f_HP_PZ	1.328125	GHz		Filter: RxFFE			Receiver testing		
Butt erworth		logical	include in fr	ffe_pre_tap_len	0	<u>U</u> I	RX_CALIBRATION	0	logical
Raised_Cosine	0	logical	include in fr	ffe_post_tap_len	0	ŲІ	Sigma BBN step	5.00E-03	V
RC_Start	6.70E+10	Hz	start freq for RCos	ffe_tap_step_size	0				
RC_end	7.97E+10	Hz	end freq for RCos	ffe_main_cursor_min	0.7				
				ffe_pre_tap1_max	0.7				
				ffe_post_tap1_max	0.7				
				ffe_tapn_max	0.7				
				ffe_backoff	0				

Thank you

Questions and Discussions