Floating Tap Feed Forward Equalization (FFE) for COM

Tobey P.-R. Li

MediaTek

IEEE P802.3dj Task Force

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Contributors

- **Richard Mellitz, Samtec**
- **Adam Gregory, Samtec**

Outline

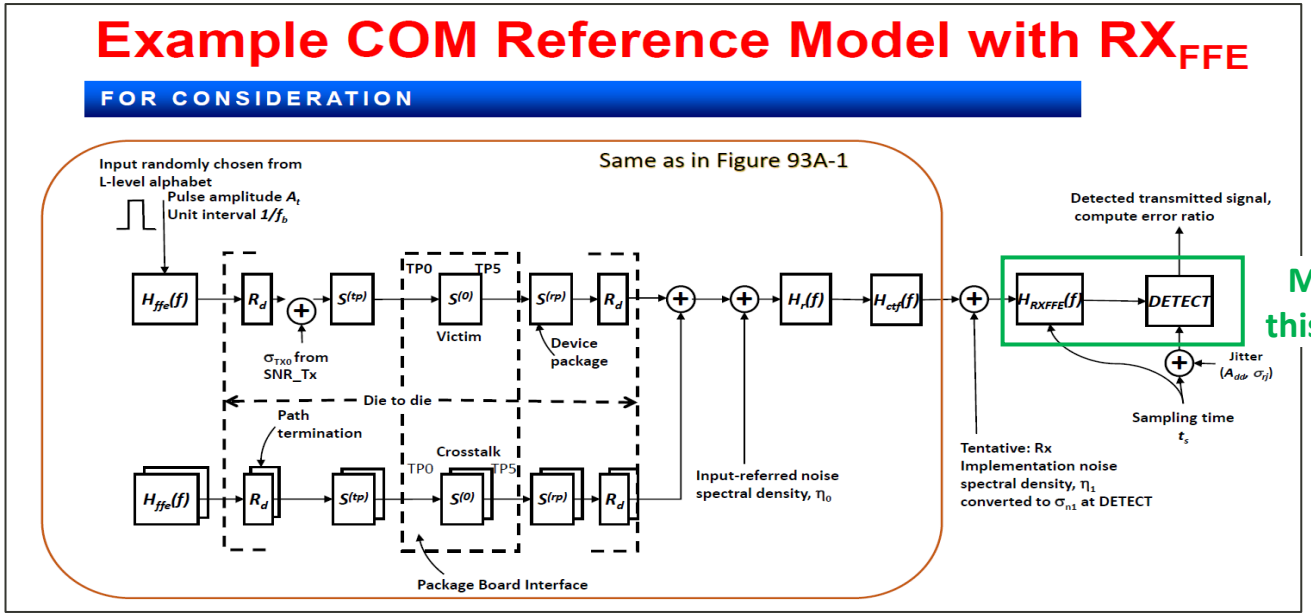
- ☐ Background and Introduction
- ☐ COM Reference Model
- ☐ COM Experiment
- ☐ Proposed Change to COM

Background and Introduction

- Directions of reference receiver taken at the July 2023 Plenary meeting
  - Strong support of direction of the RXFFE changes to Annex 93A (COM) in mellitz_3dj_01a_2307 slides 6, 7, and 8
  - Strong support of the direction of a RXFFE based reference RX to the 200G/lane AUI C2M and AUI C2C
  - See straw poll #1 & #9, motions_3cwdfdj_2307
- Most of the existing works evaluate 802.3dj baseline with reference receiver architecture of “1-tap DFE + FFE”, but with 2 different settings
  - FFE fixed taps only → Require longer equalization to cover far-end reflections
  - FFE fixed taps + DFE floating taps → COM 4.1beta2 doesn’t support FFE floating taps
- This presentation invokes the TF to adopt a simple and general receiver architecture in simulator

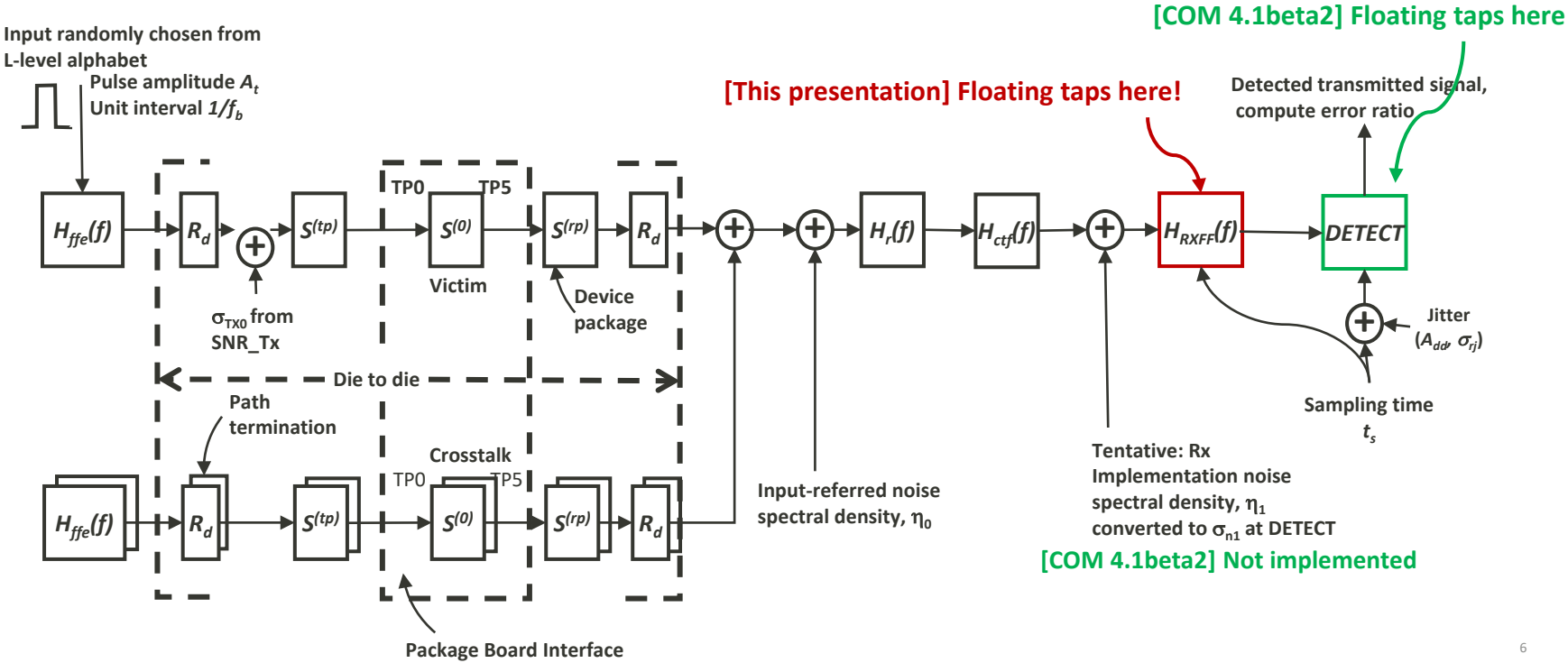
COM Reference Model Proposed in mellitz_3dj_01a_2307

- **Receiver equalization functionality in COM 4.1beta2**
  - **Fixed tap equalization: DFE/FFE**
  - **Floating tap equalization: DFE only**



COM Reference Model Proposal

- **Proposed change: Move the floating taps from DFE to FFE function**
- **No changes to the algorithms for determining FFE coefficients and floating tap locations**



Reference Parameter Highlights

- COM 4.1beta2 used, test channels and spreadsheet in appendix
  - AUIs C2C and C2M are evaluated
  - MM-CDR
- Exploratory of reference RX architecture

COM 4.1beta2 | Proposed change

[802.3ck] "Multi-Tap DFE" RX | "1-Tap DFE + FFE" RX

	Parameter	DFE-Fix + DFE-Float	FFE-Fix + DFE-Float	FFE-Fix	FFE-Fix + FFE-Float
Fixed Tap	DFE Fixed Tap	N_b	24	1	1	1
	FFE Fixed Tap	ffe_pre_tap_len	0	4	4	4
		ffe_post_tap_len	0	24	60	24
Floating Tap	DFE Floating Tap	N_bg	6	6	0	0
		N_bf	3	3	-	-
		N_f	60	60	-	-
	FFE Floating Tap	ffe_flt_tap_N_bg	NA	NA	NA	6 Groups
		ffe_flt_tap_N_bf	NA	NA	NA	3 Taps per groups
		ffe_flt_tap_N_f	NA	NA	NA	60 UI span
	RX Architecture Option		I	II	III	IV

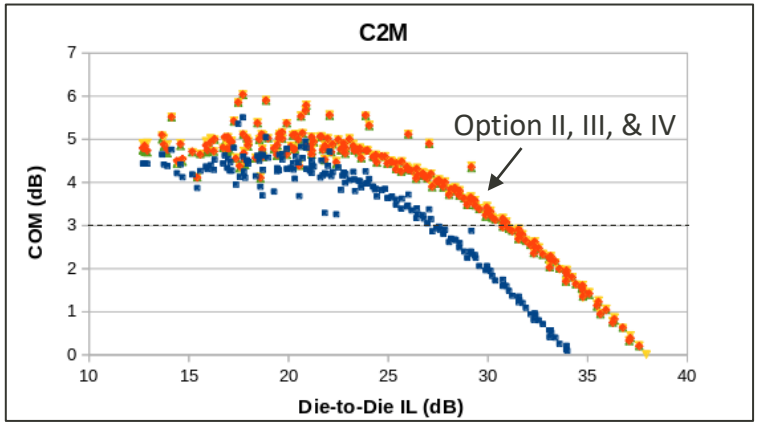
** Experimental parameters for floating FFE taps, not implemented in COM4.1beta2*

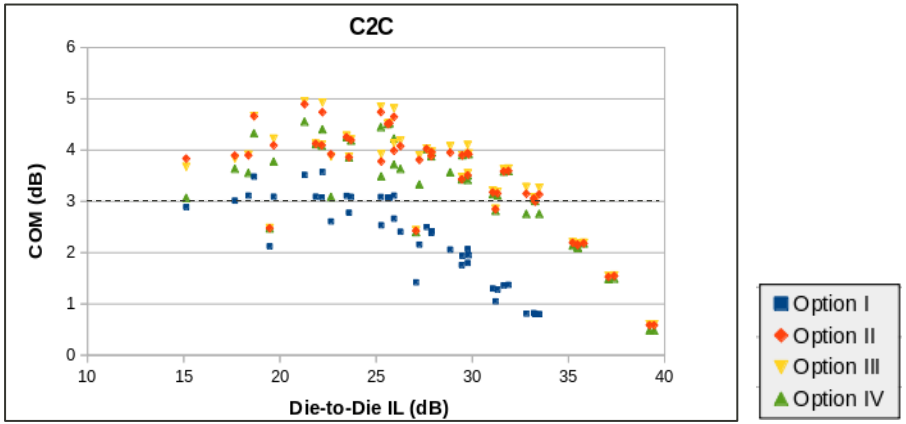
Direction of Reference Receiver Architecture

- **FFE-based receiver can outperform DFE-based receiver with less signal swing reduction, regardless of using option II, III, or IV**
- **Highly reflective channels have shown obvious COM difference among option II, III, and IV**

**** Number of post-taps***

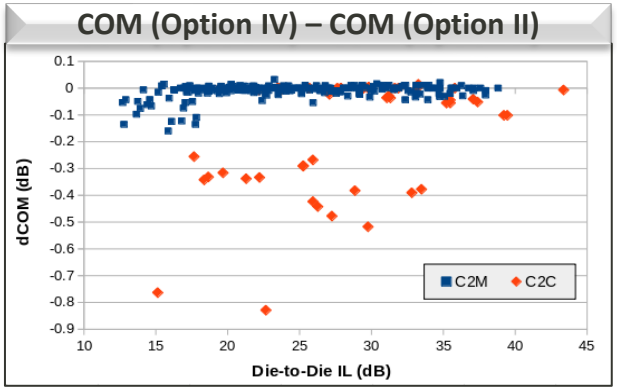
Option I	24 fixed DFE tap + 18 floating DFE tap
Option II	1 fixed DFE tap + 24 fixed FFE tap + 18 floating DFE tap
Option III	1 fixed DFE tap + 60 fixed FFE tap
Option IV	1 fixed DFE tap + 24 fixed FFE tap + 18 floating FFE tap

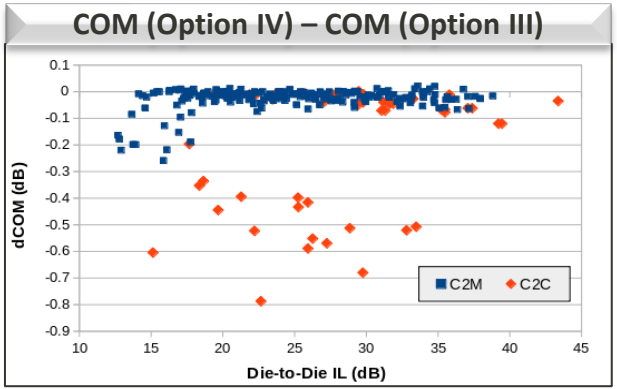




Major Concerns with FFE-based RX Architecture

- Highly possible to overestimate/underestimate the performance of short and highly reflective channels
- Inherent behavior difference between DFE and FFE floating taps, e.g., noise enhancement
  - Additional run time in searching floating tap location is required for option IV, as compared to option III, but it is minor
  - Subtraction vs convolution
- Requirement of adopting reasonable spec value in baseline equalization
  - With the same UI span, power dissipation between option III and IV can be huge
- Requirement of using representative and general receiver architecture as reference model for 200Gbps/lane design





** Number of post-taps*

Option II	1 fixed DFE tap + 24 fixed FFE tap + 18 floating DFE tap
Option III	1 fixed DFE tap + 60 fixed FFE tap
Option IV	1 fixed DFE tap + 24 fixed FFE tap + 18 floating FFE tap

Summary & Proposal

- **Different FFE-based receiver architectures can overestimate or underestimate performance, especially for highly reflective channels**
- **Propose to add the FFE floating taps into COM for baseline evaluation**
  - **Requirement of using representative and general architecture as COM reference model**
  - **Requirement of adopting reasonable spec value in baseline equalization**
- **Next step**
  - **Explore algorithms for optimizing FFE coefficients**
    - Current methodology determines the FFE coefficients without the consideration of noise distribution
    - Different algorithms may affect the DFE tap-1 coefficient → affect MLSE gain as well

Appendix

Channel List

Application	Contribution
C2M	rabinovich_3df_01_2209
	rabinovich_3df_02_2209
	rabinovich_3dj_02_230116
	rabinovich_3dj_03_230116
	Shanbhag_3dj_03_2305
	akinwale_3dj_02_2307
	akinwale_3dj_03_2307
	akinwale_3dj_04_2307
	lim_3dj_01_230629
	lim_3dj_02_230629
C2C	mellitz_3dj_elec_01_230504

Example COM Configuration for 200Gbps/Lane C2M

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[15 30 45; 1 1 1; 1 1 1; 0.5 0.5 0.5]	mm	[test cases]
z_p (NEXT)	[8 8 8; 0 0 0; 0 0 0 ; 0 0 0]	mm	[test cases]
z_p (FEXT)	[15 30 45; 1 1 1; 1 1 1; 0.5 0.5 0.5]	mm	[test cases]
z_p (RX)	[8 8 8; 0 0 0; 0 0 0; 0 0 0]	mm	[test cases]
PKG_Tx_FFE_preset	0		
C_p	[0.5e-4 0.5e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.413	V	vp/vf=
A_fe	0.413	V	vp/vf=
A_ne	0.45	V	
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.4:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.2]		[min:step:max]
c(-3)	[-0.04:.02:0]		[min:step:max]
c(-4)	[0:.02:0.02]		[min:step:max]
c(1)	[-0.12:0.02:0.04]		[min:step:max]
N_b	1	UI	
b_max(1)	0.75		As/dffe1
b_max(2..N_b)	[0.3 0.2*ones(1,22)]		As/dfe2..N_b
b_min(1)	0		As/dffe1
b_min(2..N_b)	[-0.2 -0.2*ones(1,22)]		As/dfe2..N_b
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	42.5	GHz	
f_p1	42.5	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
Butterworth	1	logical	include in fr
Raised_Cosine	0	logical	include in fr
RC_Start	6.70E+10	Hz	start freq for RCos
RC_end	7.97E+10	Hz	end freq for RCos
sample_adjustment	[0 0]	phase	
ts_anchor	0		

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	0	logical
RESULT_DIR	.\results\CAKR_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	CAKR_RCos_eval_	
COM_CONTRIBUTION	0	logical
Operational		
ERL Pass threshold	9.7	dB
COM Pass threshold	3	db
DER_0	1.33E-05	
T_r	4.00E-03	ns
FORCE_TR	1	logical
PMD_type	C2C	
EW	1	
TDR and ERL options		logical
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	2000	logical
TDR_Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	0	
fixture delay time	[0 0]	
Tukey_Window	1	
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	1.25E-08	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Enforce Causality	1
S-parameter magnitude extrapolation policy	trend_to_DC

Filter: RxFFE		
ffe_pre_tap_len	4	UI
ffe_post_tap_len	24	UI
ffe_tap_step_size	0	
ffe_main_cursor_min	0.7	
ffe_pre_tap1_max	0.7	
ffe_post_tap1_max	0.7	
ffe_tapn_max	0.7	
ffe_backoff	0	
ffe_flt_tap_N_bg	6	0 1 2 or 3 groups
ffe_flt_tap_N_bf	3	taps per group
ffe_flt_tap_N_f	60	UI span for floating taps

Table 93A-3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0008455 0.000340225]	
package_tl_tau	0.00644805	ns/mm
package_Z_c	92 92 ; 70 70; 80 80; 100 100	Ohm
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 6.44084e-4 3.6036e-05]*	1.5 db/in @ 56G
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*125*	mm
z_bp (NEXT)	0	mm
z_bp (FEXT)	*125*	mm
z_bp (RX)	0	mm
C_0	[0.2e-4 0]	nF
C_1	[0.2e-4 0]	nF
Include PCB	**0**	**logical**
Seletions (rectangle, gaussian,dual_rayleigh,triangle		
Histogram_Window_Weight	gaussian	selection
Qr	0.02	UI
ICN parameters		
f_v	0.594	Fb
f_f	0.594	Fb
f_n	0.594	Fb
f_2	79.688	GHz
A_ft	0.450	V
A_nt	0.450	V
Floating Tap Control		
N_bg	0	0 1 2 or 3 groups
N_bf	3	taps per group
N_f	60	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps
MLSE	0	logical
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

Example COM Configuration for 200Gbps/Lane C2C

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[13 31; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]
z_p (NEXT)	[11 29; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]
z_p (FEXT)	[13 31; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]
z_p (RX)	[11 29; 1 1 ; 1 1 ; 0.5 0.5]	mm	[test cases]
PKG_Tx_FFE_preset	0		
C_p	[0.5e-4 0.5e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.413	V	vp/vf=
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L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.4:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.2]		[min:step:max]
c(-3)	[-0.04:.02:0]		[min:step:max]
c(-4)	[0:.02:0.02]		[min:step:max]
c(1)	[-0.12:0.02:0.04]		[min:step:max]
N_b	1	UI	
b_max(1)	0.85		As/dffe1
b_max(2..N_b)	[0.3 0.2*ones(1,22)]		As/dfe2..N_b
b_min(1)	0		As/dffe1
b_min(2..N_b)	[-0.2 -0.2*ones(1,22)]		As/dfe2..N_b
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	42.5	GHz	
f_p1	42.5	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
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RC_Start	6.70E+10	Hz	start freq for RCos
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sample_adjustment	[0 0]	phase	
ts_anchor	0		

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	0	logical
RESULT_DIR	.\results\CAKR_[date]\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	CAKR_RCos_eval_	
COM_CONTRIBUTION	0	logical
Operational		
ERL Pass threshold	9.7	dB
COM Pass threshold	3	db
DER_0	1.33E-05	
T_r	4.00E-03	ns
FORCE_TR	1	logical
PMD_type	C2C	
EW	1	
TDR and ERL options		logical
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	2000	logical
TDR_Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	0	
fixture delay time	[0 0]	
Tukey_Window	1	
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	8.20E-09	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

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S-parameter magnitude extrapolation policy	trend_to_DC	

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ffe_post_tap1_max	0.7	
ffe_tapn_max	0.7	
ffe_backoff	0	
ffe_flt_tap_N_bg	6	0 1 2 or 3 groups
ffe_flt_tap_N_bf	3	taps per group
ffe_flt_tap_N_f	60	UI span for floating taps

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z_bp (NEXT)	*0*	mm
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C_0	[0.2e-4 0]	nF
C_1	[0.2e-4 0]	nF
Include PCB	**0**	**logical**

Seletions (rectangle, gaussian,dual_rayleigh,triangle		
Histogram_Window_Weight	gaussian	selection
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f_v	0.594	Fb
f_f	0.594	Fb
f_n	0.594	Fb
f_2	79.688	GHz
A_ft	0.450	V
A_nt	0.450	V

Floating Tap Control		
N_bg	0	0 1 2 or 3 groups
N_bf	3	taps per group
N_f	60	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps

MLSE	0	logical

Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

Thank you

Questions and Discussions