212Gb/s Per Lane PAM4 Chip-to-Module Conventional Channels Room vs. Hi Temp

James Weaver - Arista Networks
Jason Chan - Arista Networks

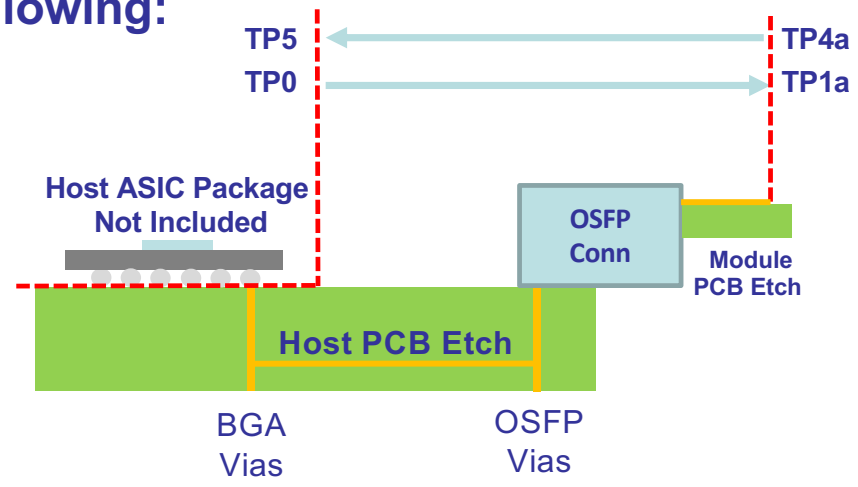
ARISTA

Overview

- This is a preliminary investigation into a typical host-to-module implementation
- The intent is to facilitate early discussion among participants using *realizable channels*
  - PCB trace s-parameter data measurement procedure similar to Delta-L but using AFR
  - All PCB footprints designed using HFSS and conform to the DFM rules of major fabricators
- These models are host BGA ball to/from module trace end to allow use with different package models
- Development is continuing, so all models are subject to continuous refinement.
  - New channels will be contributed as refinements are made

Description

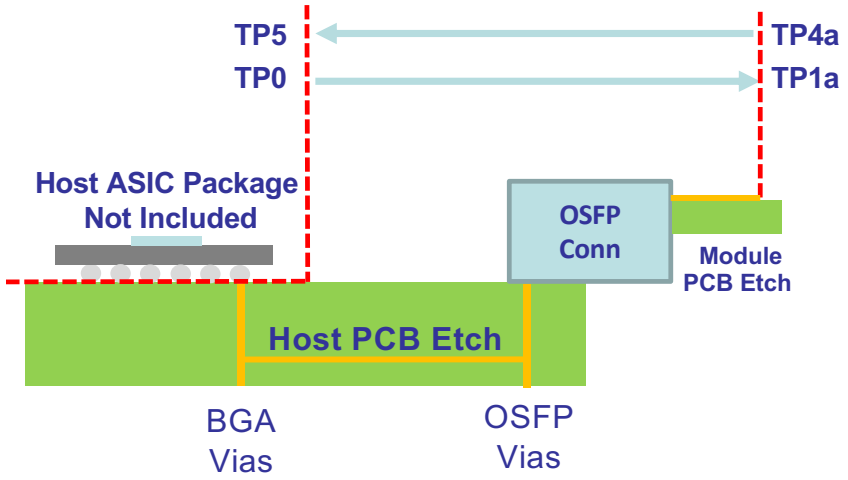
- Simulation of a typical host-to-module architecture over various trace lengths
- Composition:
  - BGA / PCB trace / OSFP via escapes simulated with HFSS
  - OSFP connector models provided by 2 vendors
- Topology does not include package effects
- The module PCB is modeled with 92Ω traces to simulate 1.3dB module loss (no crosstalk)
  - Connector PCB finger crosstalk is included
- This presentation does NOT propose the following:
  - Specific host architecture implementations
  - Specific aggregate losses



Host-to-Module Composition

- PCB Composition
  - BGA & OSFP Breakout Footprints
    - ~ 3mm worst-case PTH breakout depth
    - 8 mil vias with 5 mil stubs
    - Conforms to current PCB fab design rules
    - Nothing exotic: no skip layers, no microvias
  - Host Breakout Trace
    - Fanout lengths to OSFP vias: 3, 5, 7, 9 inches
    - Losses:
      - Room Temp: ~ 1.25 dB/in @ 53.125 GHz
      - Hi Temp: ~ 1.40 dB/in @ 53.125 GHz
    - 90 ohm @ 6 mil line width

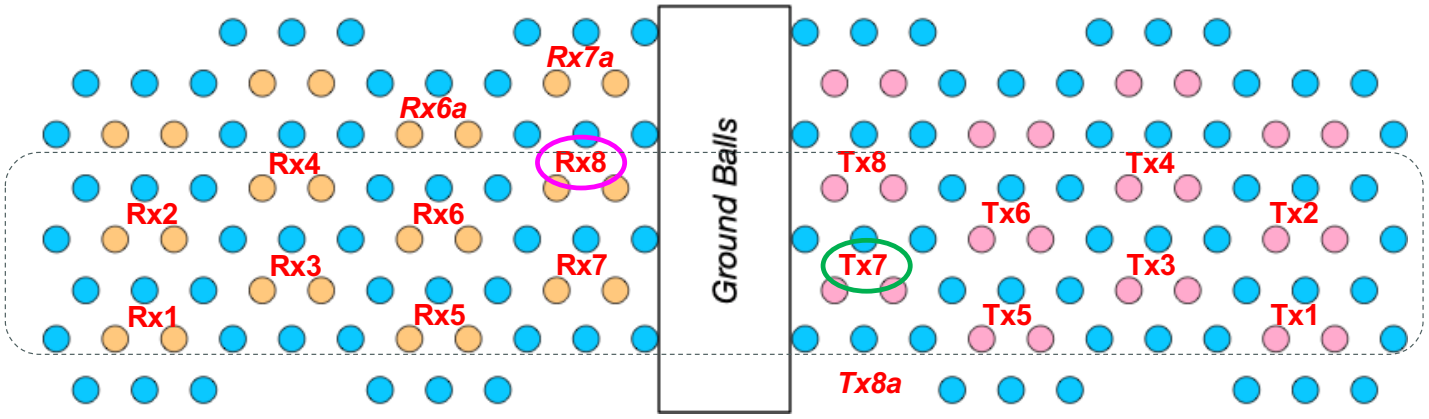
- Module Connector Composition
  - OSFP 1x1 SMT Connector
    - Vendors “X” and “Y”
    - Room Temperature only models
    - Includes 1 inch Module PCB traces @ 92 ohms



Signaling Topology

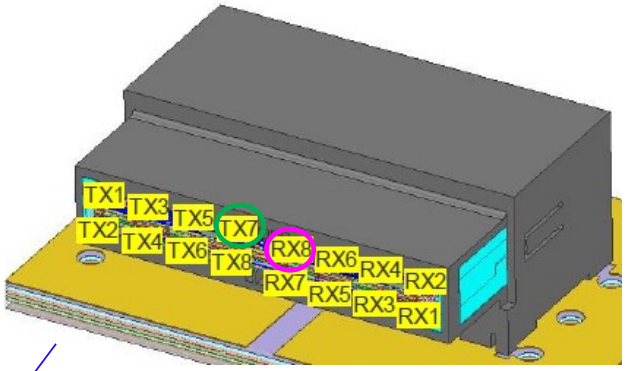
GND Pad
Rx Signal Pad
Tx Signal Pad

TP0 → TP1a Egress Victim = Tx7
TP4a → TP5 Ingress Victim = Rx8

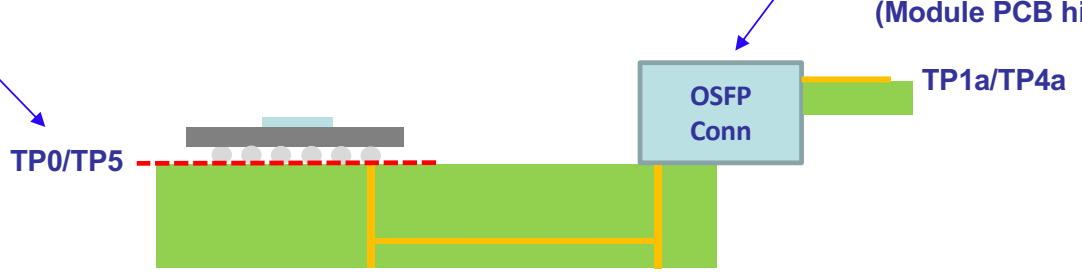


Simulated Octal

Module Connector Grid with Standard Tx/Rx OSFP Octal Assignments



(Module PCB hidden for clarity)



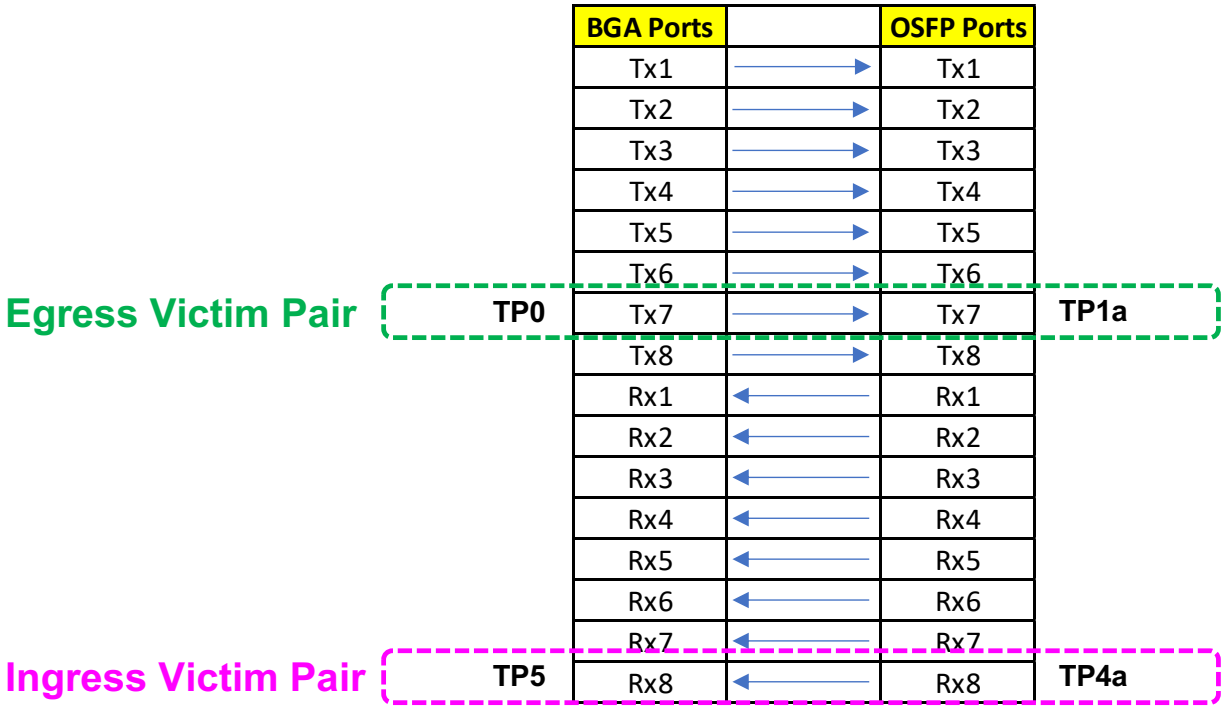
To include the "virtual" FEXT from BGA signal balls Rx5a, Rx7a & Tx8a, instantiate two copies of the following:

Tx8a: "…FEXT_TP0_Tx8_to_TP1a_Tx7.s4p"
Rx6a: "…FEXT_TP4a_Rx6_to_TP5_Rx8.s4p"
Rx7a: "…FEXT_TP4a_Rx7_to_TP5_Rx8.s4p"

See slides 18 & 19 for full file names

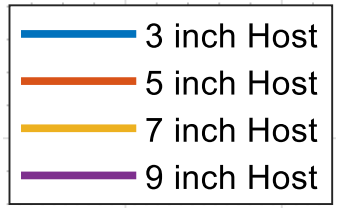
Signaling Topology

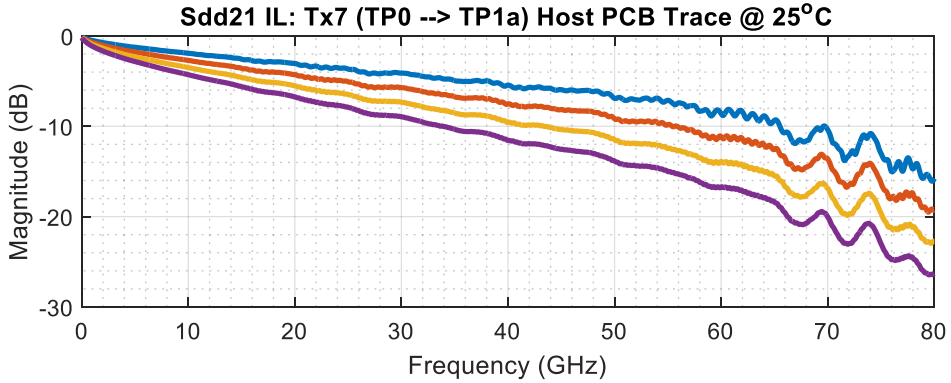
TP0 → TP1a Egress Victim = Tx7
TP4a → TP5 Ingress Victim = Rx8

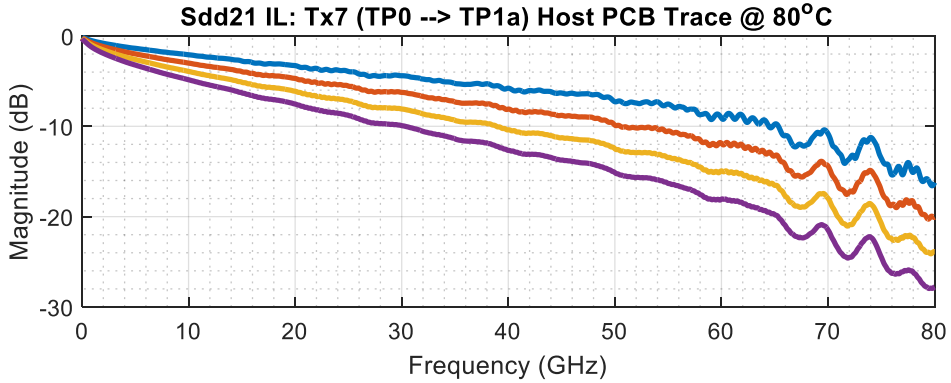


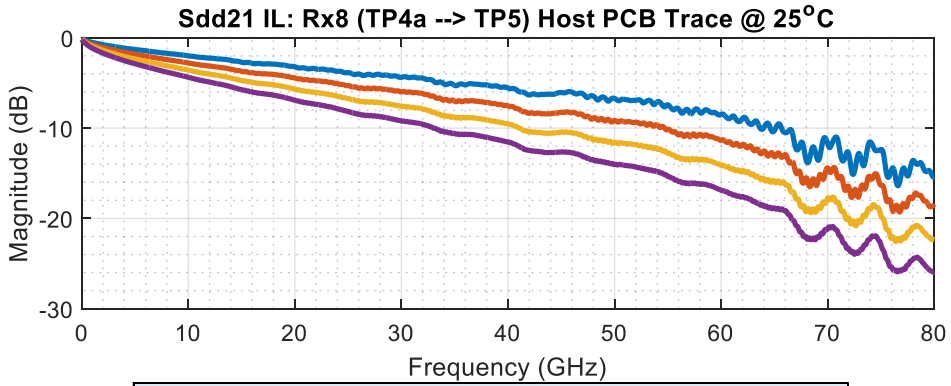
Standard Tx/Rx OSFP Octal Assignments

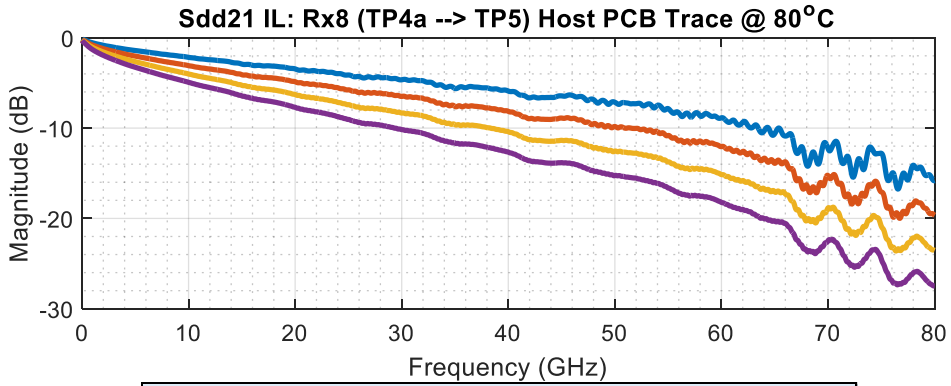
C2M Channel Model with Vendor "X" OSFP Insertion Loss vs. Temp







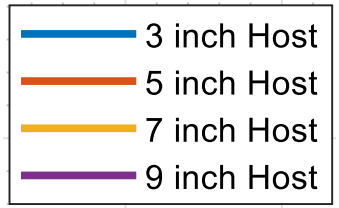


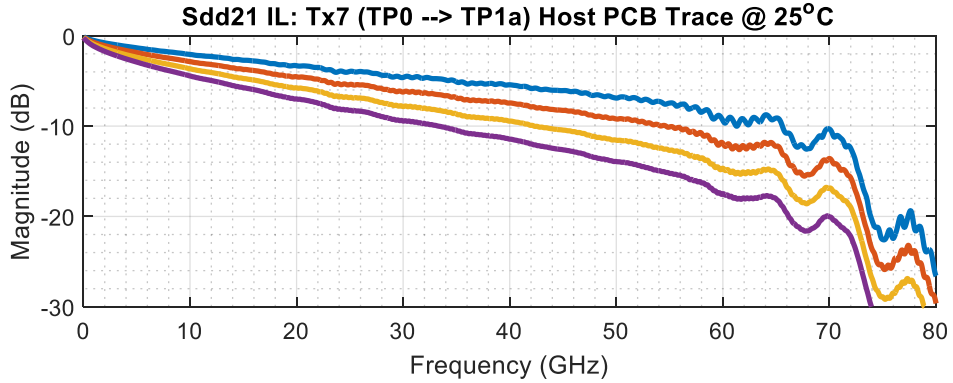


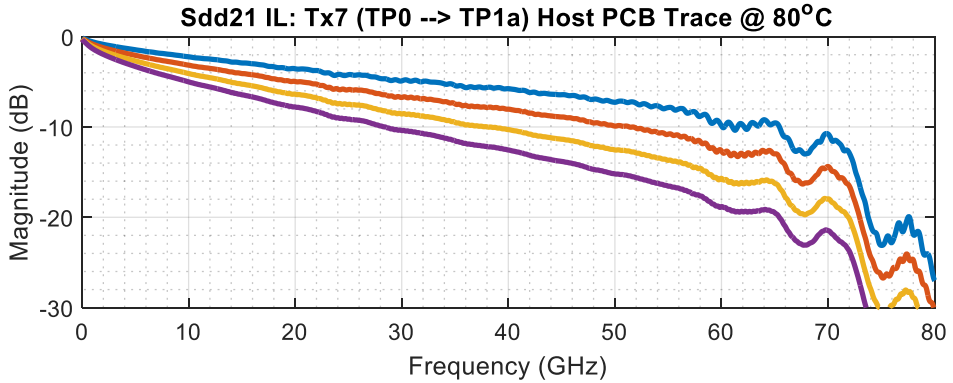
Temp = 25°C		
Host PCB Trace Length (in)	TP0 --> Tp1a Egress IL @ 53.125 GHz (dB)	TP4a --> Tp5 Ingress IL @ 53.125 GHz (dB)
3	-6.91	-6.94
5	-9.41	-9.65
7	-11.96	-12.15
9	-14.45	-14.57

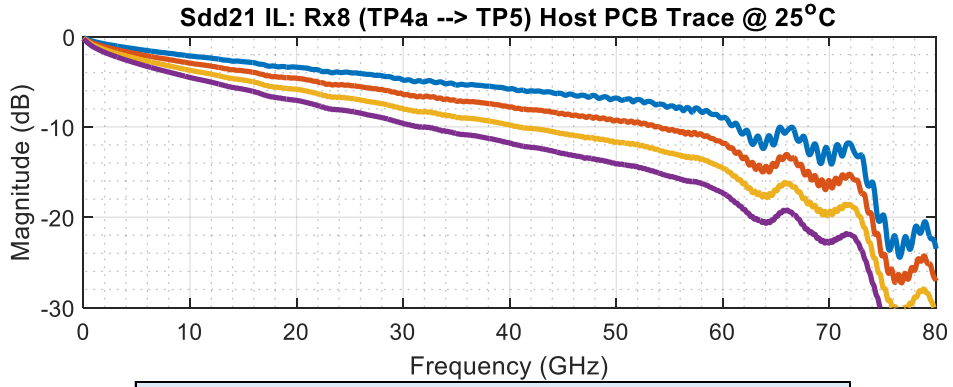
Temp = 80°C		
Host PCB Trace Length (in)	TP0 --> Tp1a Egress IL @ 53.125 GHz (dB)	TP4a --> Tp5 Ingress IL @ 53.125 GHz (dB)
3	-7.32	-7.33
5	-10.1	-10.29
7	-12.93	-13.1
9	-15.73	-15.85

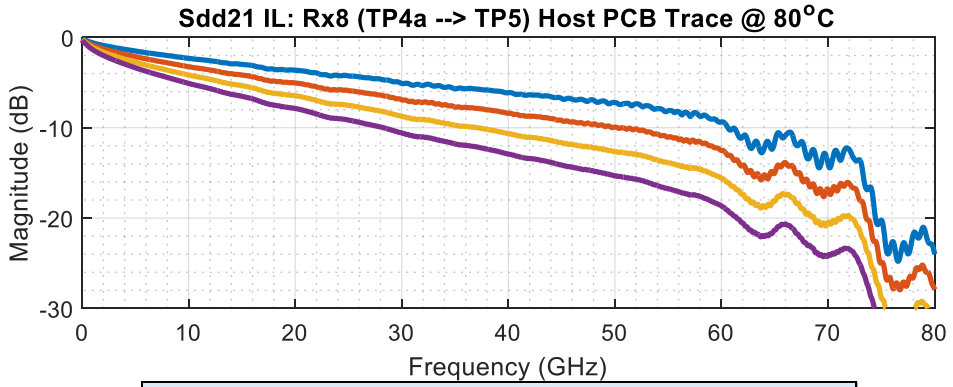
C2M Channel Model with Vendor "Y" OSFP Insertion Loss vs. Temp







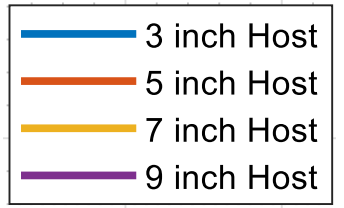


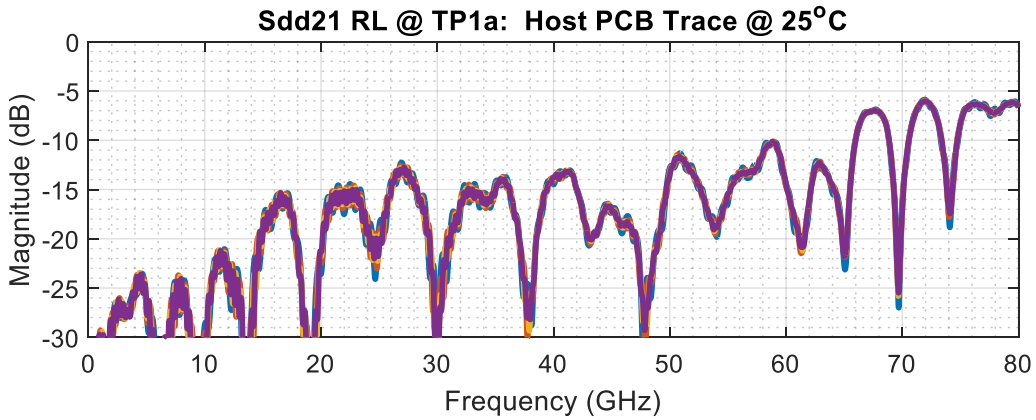


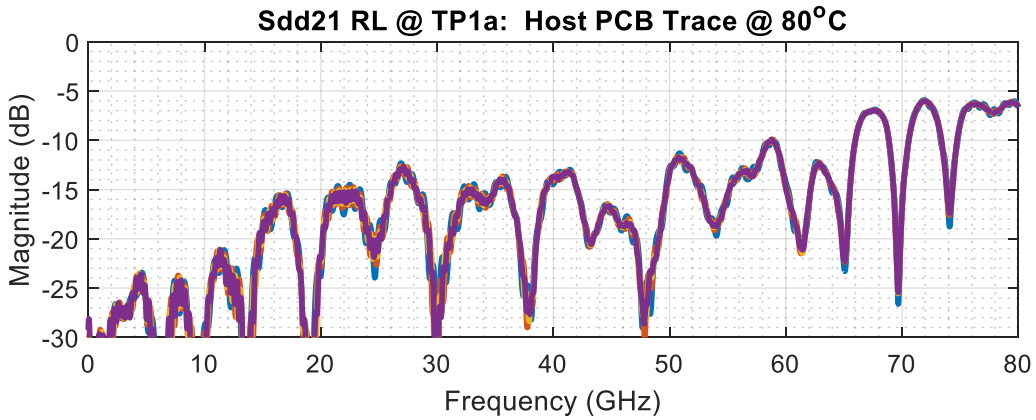
Temp = 25°C		
Host PCB Trace Length (in)	TP0 --> Tp1a Egress IL @ 53.125 GHz (dB)	TP4a --> Tp5 Ingress IL @ 53.125 GHz (dB)
3	-7.2	-7.19
5	-9.64	-9.8
7	-12.18	-12.34
9	-14.69	-14.57

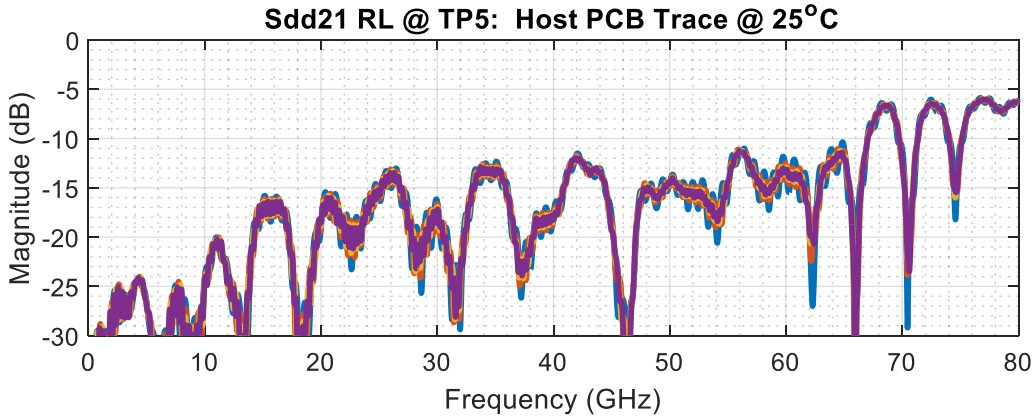
Temp = 80°C		
Host PCB Trace Length (in)	TP0 --> Tp1a Egress IL @ 53.125 GHz (dB)	TP4a --> Tp5 Ingress IL @ 53.125 GHz (dB)
3	-7.61	-7.57
5	-10.34	-10.46
7	-13.16	-13.29
9	-15.97	-16.06

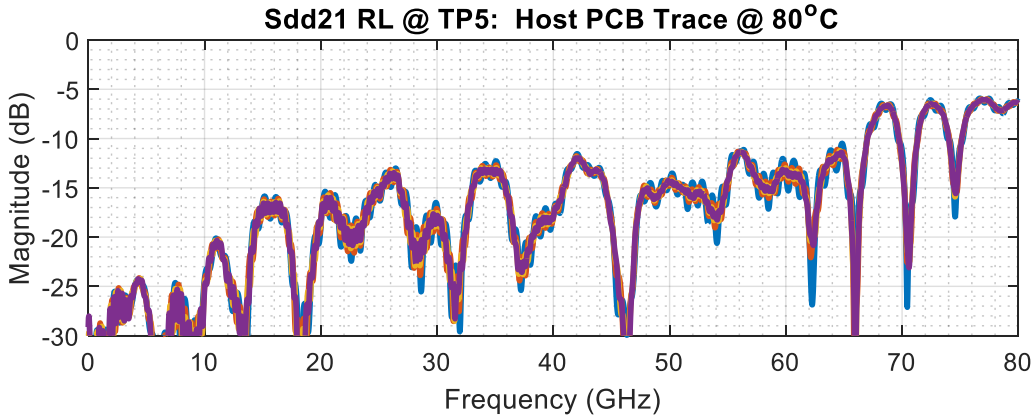
C2M Channel Model with Vendor “X” OSFP
Return Loss vs. Temp



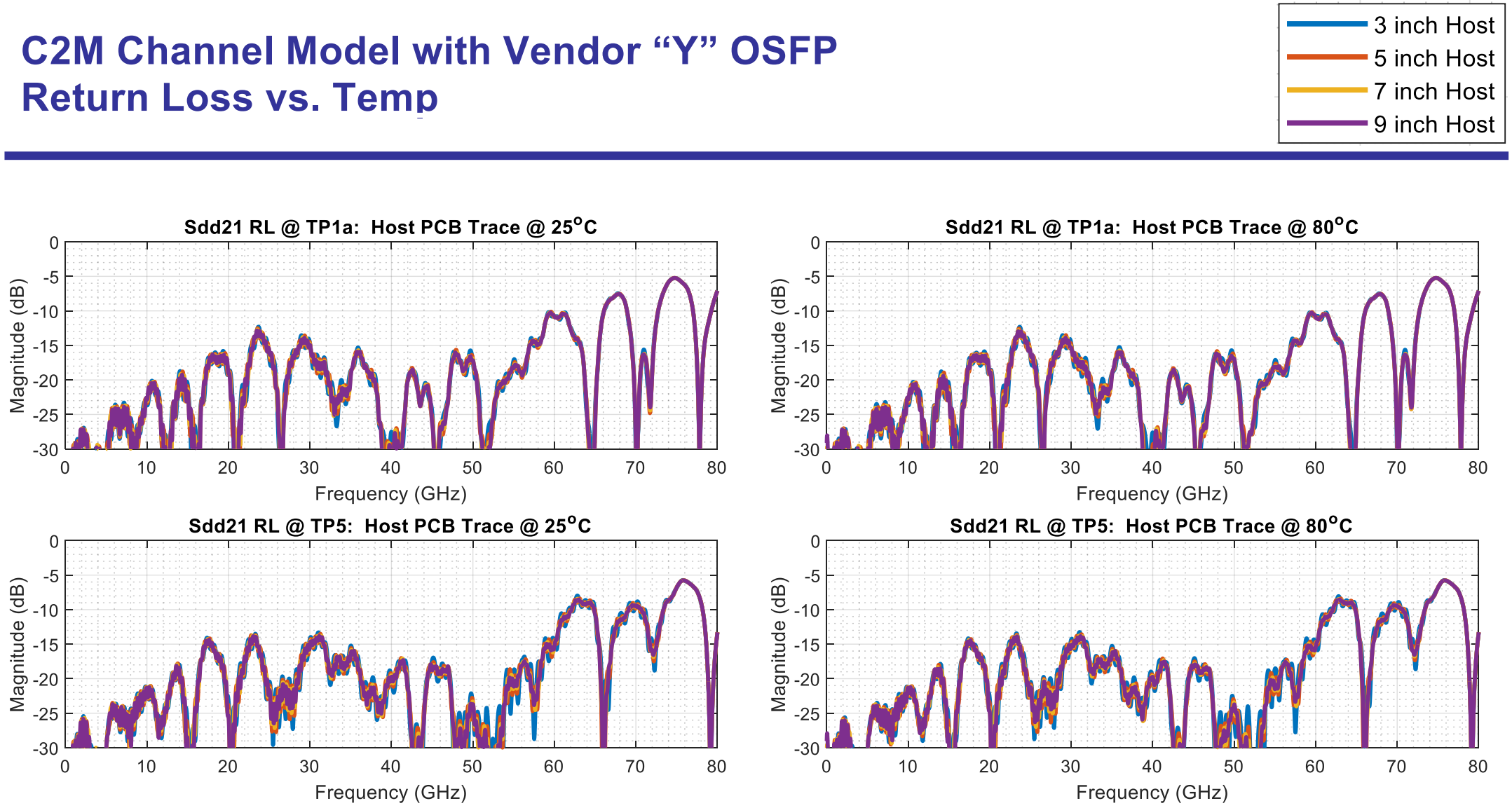




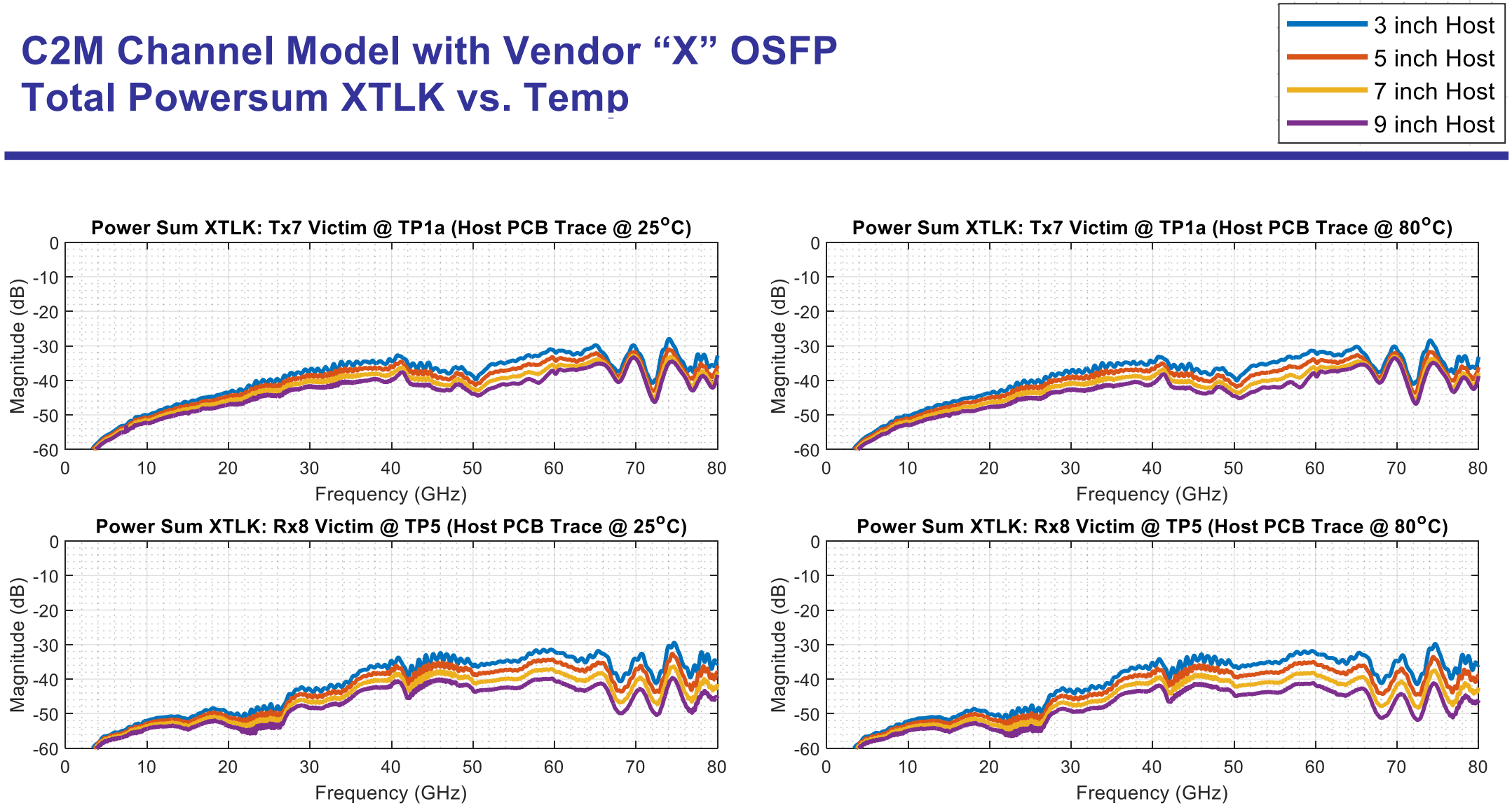




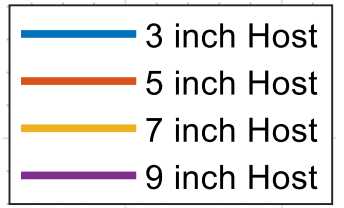
C2M Channel Model with Vendor “Y” OSFP
Return Loss vs. Temp

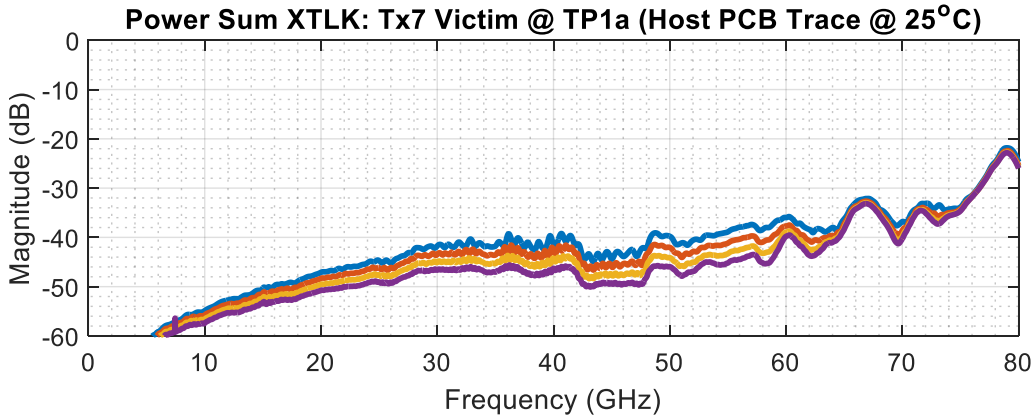


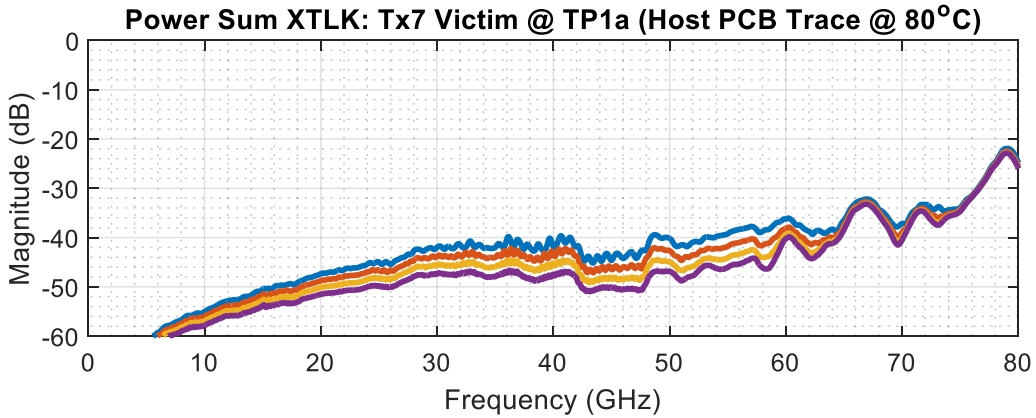
C2M Channel Model with Vendor “X” OSFP
Total Powersum XTLK vs. Temp

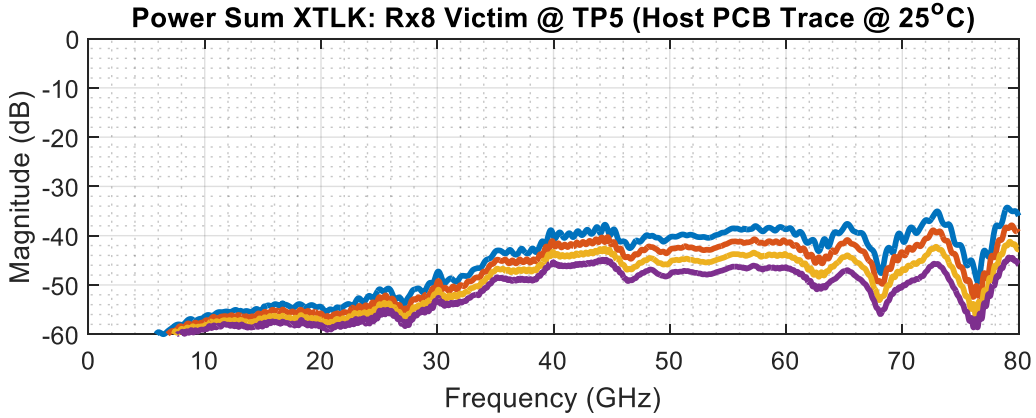


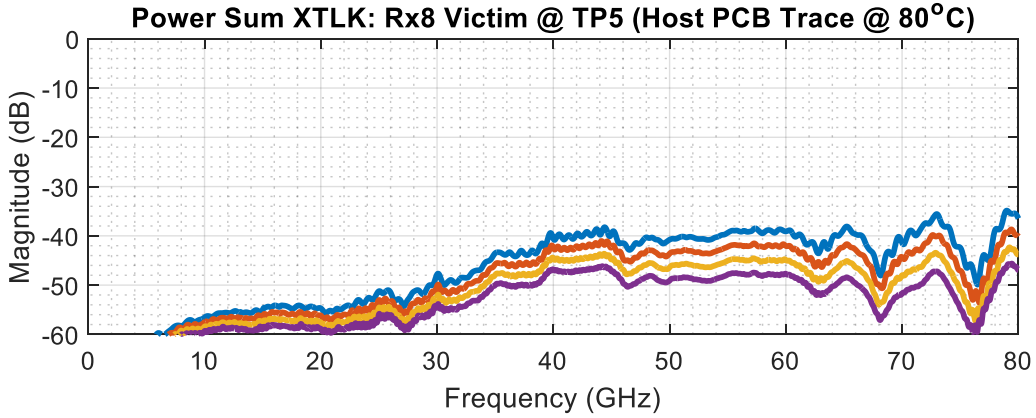
C2M Channel Model with Vendor “Y” OSFP
Total Powersum XTLK vs. Temp





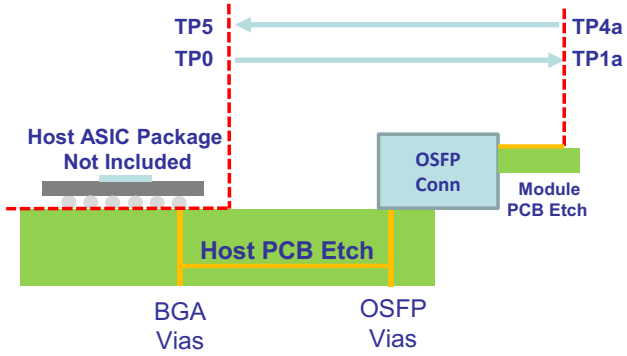






Summary

- Contributed chip-to-module channel model with SMT OSFP connectors



  - TP0 to TP1a egress insertion losses generally range from ~7dB to ~14.6dB across 4 PCB lengths over temp
  - TP4a to TP5 ingress insertion losses range from ~7.32dB to ~16dB across 4 PCB lengths over temp
  - Each victim channel contains 16 signal lanes: 1 victim and 15 aggressors
  - Return losses less than –10dB to ~65GHz
  - Power summed XTLK is generally less than –30dB to ~70GHz

Chip-to-Module Channels

File Naming Convention: TP0→TP1a Egress Thru Channels

SMT OSFP Vendor Model

= [“X”, “Y”]

PCB Trace Temp

##= [25°C, 80°C]

C2M_[#]_OSFP224_[#]in_host_PCB_[#]C_thru_TP0_Tx7_to_TP1a_Tx7.s4p

PCB Length

= [3, 5, 7, 9] inches

Chip-to-Module Channels

File Naming Convention: TP4a→TP5 Ingress Thru Channels

SMT OSFP Vendor Model

= [“X”, “Y”]

PCB Trace Temp

= [25°C, 80°C]

C2M_[#]_OSFP224_[#]in_host_PCB_[#]C_thru_TP4a_Rx8_to_TP5_Rx8.s4p

PCB Length

= [3, 5, 7, 9] inches

Chip-to-Module Channels

Egress Thru Channel Files:

C2M_X_OSFP224_3in_host_PCB_25C_thru_TP0_Tx7_to_TP1a_Tx7.s4p
C2M_X_OSFP224_5in_host_PCB_25C_thru_TP0_Tx7_to_TP1a_Tx7.s4p
C2M_X_OSFP224_7in_host_PCB_25C_thru_TP0_Tx7_to_TP1a_Tx7.s4p
C2M_X_OSFP224_9in_host_PCB_25C_thru_TP0_Tx7_to_TP1a_Tx7.s4p

C2M_X_OSFP224_3in_host_PCB_80C_thru_TP0_Tx7_to_TP1a_Tx7.s4p
C2M_X_OSFP224_5in_host_PCB_80C_thru_TP0_Tx7_to_TP1a_Tx7.s4p
C2M_X_OSFP224_7in_host_PCB_80C_thru_TP0_Tx7_to_TP1a_Tx7.s4p
C2M_X_OSFP224_9in_host_PCB_80C_thru_TP0_Tx7_to_TP1a_Tx7.s4p

C2M_Y_OSFP224_3in_host_PCB_25C_thru_TP0_Tx7_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_5in_host_PCB_25C_thru_TP0_Tx7_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_7in_host_PCB_25C_thru_TP0_Tx7_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_9in_host_PCB_25C_thru_TP0_Tx7_to_TP1a_Tx7.s4p

C2M_Y_OSFP224_3in_host_PCB_80C_thru_TP0_Tx7_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_5in_host_PCB_80C_thru_TP0_Tx7_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_7in_host_PCB_80C_thru_TP0_Tx7_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_9in_host_PCB_80C_thru_TP0_Tx7_to_TP1a_Tx7.s4p

Chip-to-Module Channels

Ingress Thru Channel Files:

C2M_X_OSFP224_3in_host_PCB_25C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
C2M_X_OSFP224_5in_host_PCB_25C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
C2M_X_OSFP224_7in_host_PCB_25C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
C2M_X_OSFP224_9in_host_PCB_25C_thru_TP4a_Rx8_to_TP5_Rx8.s4p

C2M_X_OSFP224_3in_host_PCB_80C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
C2M_X_OSFP224_5in_host_PCB_80C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
C2M_X_OSFP224_7in_host_PCB_80C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
C2M_X_OSFP224_9in_host_PCB_80C_thru_TP4a_Rx8_to_TP5_Rx8.s4p

C2M_Y_OSFP224_3in_host_PCB_25C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
C2M_Y_OSFP224_5in_host_PCB_25C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
C2M_Y_OSFP224_7in_host_PCB_25C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
C2M_Y_OSFP224_9in_host_PCB_25C_thru_TP4a_Rx8_to_TP5_Rx8.s4p

C2M_Y_OSFP224_3in_host_PCB_80C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
C2M_Y_OSFP224_5in_host_PCB_80C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
C2M_Y_OSFP224_7in_host_PCB_80C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
C2M_Y_OSFP224_9in_host_PCB_80C_thru_TP4a_Rx8_to_TP5_Rx8.s4p

Chip-to-Module Channels

File Naming Convention: XTLK Channels (Egress Victim)

SMT OSFP Vendor Model	PCB Length	PCB Trace Temp	(FEXT Aggressor Origin on BGA side) FEXT Aggressor Source
# = [“X”, “Y”]	# = [3, 5, 7, 9] inches	# = [25°C, 80°C]	# = Tx1,Tx2, … , Tx6, Tx8

C2M_[#]_OSFP224_[#]in_host_PCB_[#]C_FEXT_TP0_[#]_to_TP1a_Tx7.s4p

SMT OSFP Vendor Model	PCB Length	PCB Trace Temp	(NEXT Aggressor Origin on OSFP side) NEXT Aggressor Source
# = [“X”, “Y”]	# = [3, 5, 7, 9] inches	# = [25°C, 80°C]	# = Rx1,Rx2, … , Rx8

C2M_[#]_OSFP224_[#]in_host_PCB_[#]C_NEXT_TP1a_[#]_to_TP1a_Tx7.s4p

Chip-to-Module Channels

File Naming Convention: XTLK Channels (Ingress Victim)

SMT OSFP Vendor Model	PCB Length	PCB Trace Temp	(FEXT Aggressor Origin on OSFP side) FEXT Aggressor Source
# = [“X”, “Y”]	# = [3, 5, 7, 9] inches	# = [25°C, 80°C]	# = Rx1,Rx2, … , Rx7

C2M_[#]_OSFP224_[#]in_host_PCB_[#]C_FEXT_TP4a_[#]_to_TP5_Rx8.s4p

SMT OSFP Vendor Model	PCB Length	PCB Trace Temp	(NEXT Aggressor Origin on BGA side) NEXT Aggressor Source
# = [“X”, “Y”]	# = [3, 5, 7, 9] inches	# = [25°C, 80°C]	# = Tx1,Tx2, … , Tx8

C2M_[#]_OSFP224_[#]in_host_PCB_[#]C_NEXT_TP5_[#]_to_TP5_Rx8.s4p

Chip-to-Module Channels

XTLK Channel Files: Egress Victim

Host PCB Trace Length: ### = [3, 5, 7, 9] in

C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx1_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx1_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx2_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx2_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx3_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx3_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx4_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx4_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx5_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx5_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx6_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx6_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx8_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx8_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx1_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx1_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx2_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx2_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx3_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx3_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx4_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx4_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx5_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx5_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx6_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx6_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx7_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx7_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx8_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx8_to_TP1a_Tx7.s4p

Chip-to-Module Channels

XTLK Channel Files: Egress Victim

Host PCB Trace Length: ### = [3, 5, 7, 9] in

C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx1_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx1_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx2_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx2_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx3_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx3_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx4_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx4_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx5_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx5_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx6_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx6_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx8_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx8_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx1_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx1_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx2_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx2_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx3_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx3_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx4_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx4_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx5_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx5_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx6_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx6_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx7_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx7_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx8_to_TP1a_Tx7.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx8_to_TP1a_Tx7.s4p

Chip-to-Module Channels

XTLK Channel Files: Ingress Victim

Host PCB Trace Length: ### = [3, 5, 7, 9] in

C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx1_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx1_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx2_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx2_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx3_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx3_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx4_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx4_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx5_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx5_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx6_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx6_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx7_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx7_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx1_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx1_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx2_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx2_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx3_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx3_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx4_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx4_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx5_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx5_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx6_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx6_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx7_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx7_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx8_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx8_to_TP5_Rx8.s4p

Chip-to-Module Channels

XTLK Channel Files: Ingress Victim

Host PCB Trace Length: ### = [3, 5, 7, 9] in

C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx1_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx1_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx2_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx2_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx3_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx3_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx4_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx4_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx5_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx5_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx6_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx6_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx7_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx7_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx1_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx1_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx2_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx2_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx3_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx3_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx4_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx4_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx5_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx5_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx6_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx6_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx7_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx7_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx8_to_TP5_Rx8.s4p	C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx8_to_TP5_Rx8.s4p