212Gb/s Per Lane PAM4 Chip-to-Module Conventional Channels Room vs. Hi Temp

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Overview

- This is a preliminary investigation into a typical host-to-module implementation

- The intent is to facilitate early discussion among participants using realizable channels
  - PCB trace s-parameter data measurement procedure similar to Delta-L but using AFR
  - All PCB footprints designed using HFSS and conform to the DFM rules of major fabricators

- These models are host BGA ball to/from module trace end to allow use with different package models

- Development is continuing, so all models are subject to continuous refinement.
  - New channels will be contributed as refinements are made
Simulation of a typical host-to-module architecture over various trace lengths

Composition:
- BGA / PCB trace / OSFP via escapes simulated with HFSS
- OSFP connector models provided by 2 vendors

Topology does not include package effects

The module PCB is modeled with 92Ω traces to simulate 1.3dB module loss (no crosstalk)
- Connector PCB finger crosstalk is included

This presentation does NOT propose the following:
- Specific host architecture implementations
- Specific aggregate losses
Host-to-Module Composition

- **PCB Composition**
  - BGA & OSFP Breakout Footprints
    - ~ 3mm worst-case PTH breakout depth
    - 8 mil vias with 5 mil stubs
    - Conforms to current PCB fab design rules
    - Nothing exotic: no skip layers, no microvias
  - Host Breakout Trace
    - Fanout lengths to OSFP vias: 3, 5, 7, 9 inches
    - Losses:
      - Room Temp: ~ 1.25 dB/in @ 53.125 GHz
      - Hi Temp: ~ 1.40 dB/in @ 53.125 GHz
    - 90 ohm @ 6 mil line width

- **Module Connector Composition**
  - OSFP 1x1 SMT Connector
    - Vendors “X” and “Y”
    - Room Temperature only models
    - Includes 1 inch Module PCB traces @ 92 ohms
To include the “virtual” FEXT from BGA signal balls Rx5a, Rx7a & Tx8a, instantiate two copies of the following:

- **Tx8a:** “…FEXT_TP0_Tx8_to_TP1a_Tx7.s4p”
- **Rx6a:** “…FEXT_TP4a_Rx6_to_TP5_Rx8.s4p”
- **Rx7a:** “…FEXT_TP4a_Rx7_to_TP5_Rx8.s4p”

See slides 18 & 19 for full file names.
Signaling Topology

TP0 → TP1a Egress Victim = Tx7
TP4a → TP5 Ingress Victim = Rx8

Egress Victim Pair

Ingress Victim Pair

Standard Tx/Rx OSFP Octal Assignments
C2M Channel Model with Vendor “X” OSFP Insertion Loss vs. Temp

<table>
<thead>
<tr>
<th>Host PCB Trace Length (in)</th>
<th>TP0 --&gt; Tp1a Egress IL @ 53.125 GHz (dB)</th>
<th>TP4a --&gt; Tp5 Ingress IL @ 53.125 GHz (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>-6.91</td>
<td>-6.94</td>
</tr>
<tr>
<td>5</td>
<td>-9.41</td>
<td>-9.65</td>
</tr>
<tr>
<td>7</td>
<td>-11.96</td>
<td>-12.15</td>
</tr>
<tr>
<td>9</td>
<td>-14.45</td>
<td>-14.57</td>
</tr>
</tbody>
</table>

**Temp = 25°C**

**Temp = 80°C**
C2M Channel Model with Vendor “Y” OSFP
Insertion Loss vs. Temp

<table>
<thead>
<tr>
<th>Temp = 25°C</th>
<th>Host PCB Trace Length (in)</th>
<th>TP0 → Tp1a Egress IL @ 53.125 GHz (dB)</th>
<th>TP4a → Tp5 Ingress IL @ 53.125 GHz (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>-7.2</td>
<td>-7.19</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>-9.64</td>
<td>-9.8</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>-12.18</td>
<td>-12.34</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>-14.69</td>
<td>-14.57</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Temp = 80°C</th>
<th>Host PCB Trace Length (in)</th>
<th>TP0 → Tp1a Egress IL @ 53.125 GHz (dB)</th>
<th>TP4a → Tp5 Ingress IL @ 53.125 GHz (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>-7.61</td>
<td>-7.57</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>-10.34</td>
<td>-10.46</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>-13.16</td>
<td>-13.29</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>-15.97</td>
<td>-16.06</td>
<td></td>
</tr>
</tbody>
</table>
C2M Channel Model with Vendor “X” OSFP
Return Loss vs. Temp

Sdd21 RL @ TP1a: Host PCB Trace @ 25°C

Sdd21 RL @ TP5: Host PCB Trace @ 25°C

Sdd21 RL @ TP1a: Host PCB Trace @ 80°C

Sdd21 RL @ TP5: Host PCB Trace @ 80°C
C2M Channel Model with Vendor “Y” OSFP
Return Loss vs. Temp

Sdd21 RL @ TP1a: Host PCB Trace @ 25°C

Sdd21 RL @ TP1a: Host PCB Trace @ 80°C

Sdd21 RL @ TP5: Host PCB Trace @ 25°C

Sdd21 RL @ TP5: Host PCB Trace @ 80°C
C2M Channel Model with Vendor “X” OSFP
Total Powersum XTLK vs. Temp
C2M Channel Model with Vendor “Y” OSFP
Total Powersum XTLK vs. Temp

Power Sum XTLK: Tx7 Victim @ TP1a (Host PCB Trace @ 25°C)

Power Sum XTLK: Tx7 Victim @ TP1a (Host PCB Trace @ 80°C)

Power Sum XTLK: Rx8 Victim @ TP5 (Host PCB Trace @ 25°C)

Power Sum XTLK: Rx8 Victim @ TP5 (Host PCB Trace @ 80°C)
Summary

- Contributed chip-to-module channel model with SMT OSFP connectors

- TP0 to TP1a egress insertion losses generally range from ~7dB to ~14.6dB across 4 PCB lengths over temp
- TP4a to TP5 ingress insertion losses range from ~7.32dB to ~16dB across 4 PCB lengths over temp
- Each victim channel contains 16 signal lanes: 1 victim and 15 aggressors
- Return losses less than –10dB to ~65GHz
- Power summed XTLK is generally less than –30dB to ~70GHz
Chip-to-Module Channels

File Naming Convention: TP0→TP1a Egress Thru Channels

SMT OSFP Vendor Model
# = ["X", "Y"]

PCB Trace Temp
# = [25°C, 80°C]

PCB Length
# = [3, 5, 7, 9] inches

C2M_[#]_OSFP224_[#]in_host_PCB_[#]C_thru_TP0_Tx7_to_TP1a_Tx7.s4p
Chip-to-Module Channels

File Naming Convention: TP4a→TP5 Ingress Thru Channels

C2M[#]_OSFP224[#]in_host_PCB[#]C_thru_TP4a_Rx8_to_TP5_Rx8.s4p

SMT OSFP Vendor Model
# = ["X", "Y"]

PCB Trace Temp
# = [25°C, 80°C]

PCB Length
# = [3, 5, 7, 9] inches

Port 1
TP4a

Thru Channel

Port 2

Port 3

Port 4

TP5
## Chip-to-Module Channels

### Egress Thru Channel Files:

<table>
<thead>
<tr>
<th>Description</th>
<th>File Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>C2M_X_OSFP224_3in_host_PCB_25C_thru_TP0_Tx7_to_TP1a_Tx7.s4p</td>
<td></td>
</tr>
<tr>
<td>C2M_X_OSFP224_5in_host_PCB_25C_thru_TP0_Tx7_to_TP1a_Tx7.s4p</td>
<td></td>
</tr>
<tr>
<td>C2M_X_OSFP224_7in_host_PCB_25C_thru_TP0_Tx7_to_TP1a_Tx7.s4p</td>
<td></td>
</tr>
<tr>
<td>C2M_X_OSFP224_9in_host_PCB_25C_thru_TP0_Tx7_to_TP1a_Tx7.s4p</td>
<td></td>
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<tr>
<td>C2M_X_OSFP224_3in_host_PCB_80C_thru_TP0_Tx7_to_TP1a_Tx7.s4p</td>
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<td>C2M_Y_OSFP224_3in_host_PCB_25C_thru_TP0_Tx7_to_TP1a_Tx7.s4p</td>
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<td></td>
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<tr>
<td>C2M_Y_OSFP224_9in_host_PCB_80C_thru_TP0_Tx7_to_TP1a_Tx7.s4p</td>
<td></td>
</tr>
</tbody>
</table>
Chip-to-Module Channels

**Ingress Thru Channel Files:**

- C2M_X_OSFP224_3in_host_PCB_25C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
- C2M_X_OSFP224_5in_host_PCB_25C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
- C2M_X_OSFP224_7in_host_PCB_25C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
- C2M_X_OSFP224_9in_host_PCB_25C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
- C2M_X_OSFP224_3in_host_PCB_80C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
- C2M_X_OSFP224_5in_host_PCB_80C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
- C2M_X_OSFP224_7in_host_PCB_80C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
- C2M_X_OSFP224_9in_host_PCB_80C_thru_TP4a_Rx8_to_TP5_Rx8.s4p

- C2M_Y_OSFP224_3in_host_PCB_25C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
- C2M_Y_OSFP224_5in_host_PCB_25C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
- C2M_Y_OSFP224_7in_host_PCB_25C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
- C2M_Y_OSFP224_9in_host_PCB_25C_thru_TP4a_Rx8_to_TP5_Rx8.s4p

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- C2M_Y_OSFP224_5in_host_PCB_80C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
- C2M_Y_OSFP224_7in_host_PCB_80C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
- C2M_Y_OSFP224_9in_host_PCB_80C_thru_TP4a_Rx8_to_TP5_Rx8.s4p
Chip-to-Module Channels

File Naming Convention: XTLK Channels (Egress Victim)

SMT OSFP Vendor Model
# = [“X”, “Y”]

PCB Length
# = [3, 5, 7, 9] inches

PCB Trace Temp
# = [25°C, 80°C]

FEXT Aggressor Source
# = Tx1, Tx2, …, Tx6, Tx8

C2M_[#]_OSFP224_[#]in_host_PCIE_[#]C_FEXT_TP0_[#]to_TP1a_Tx7.s4p

PCB Length
# = [3, 5, 7, 9] inches

PCB Trace Temp
# = [25°C, 80°C]

SMT OSFP Vendor Model
# = [“X”, “Y”]

NEXT Aggressor Source
# = Rx1, Rx2, …, Rx8

C2M_[#]_OSFP224_[#]in_host_PCIE_[#]C_NEXT_TP1a_[#]to_TP1a_Tx7.s4p

(FEXT Aggressor Origin on BGA side)

(NEXT Aggressor Origin on OSFP side)
**Chip-to-Module Channels**

**File Naming Convention: XTLK Channels (Ingress Victim)**

- **SMT OSFP Vendor Model**: 
  - # = ["X", "Y"]
- **PCB Length**: 
  - # = [3, 5, 7, 9] inches
- **PCB Trace Temp**: 
  - # = [25°C, 80°C]
- **FEXT Aggressor Source**: 
  - # = Rx1, Rx2, …, Rx7

**C2M_[#]_OSFP224_[#]in_host_PCB_[#]C_FEXT_TP4a_[#]_to_TP5_Rx8.s4p**

- **SMT OSFP Vendor Model**: 
  - # = ["X", "Y"]
- **PCB Length**: 
  - # = [3, 5, 7, 9] inches
- **PCB Trace Temp**: 
  - # = [25°C, 80°C]
- **NEXT Aggressor Source**: 
  - # = Tx1, Tx2, …, Tx8

**C2M_[#]_OSFP224_[#]in_host_PCB_[#]C_NEXT_TP5_[#]_to_TP5_Rx8.s4p**

(FEXT Aggressor Origin on OSFP side)

(NEXT Aggressor Origin on BGA side)
Chip-to-Module Channels

**XTLK Channel Files: Egress Victim**

Host PCB Trace Length: ### = [3, 5, 7, 9] in

C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx1_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx2_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx3_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx4_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx5_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx6_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx8_to_TP1a_Tx7.s4p

C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx1_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx2_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx3_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx4_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx5_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx6_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP0_Tx8_to_TP1a_Tx7.s4p

C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx1_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx2_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx3_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx4_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx5_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx6_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx7_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx8_to_TP1a_Tx7.s4p

C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx1_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx2_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx3_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx4_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx5_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx6_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx7_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP1a_Rx8_to_TP1a_Tx7.s4p
Chip-to-Module Channels

**XTLK Channel Files: Egress Victim**

Host PCB Trace Length: ### = [3, 5, 7, 9] in

C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx1_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx2_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx3_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx4_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx5_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx6_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx8_to_TP1a_Tx7.s4p

C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx1_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx2_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx3_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx4_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx5_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx6_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx7_to_TP1a_Tx7.s4p
C2M_X_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx8_to_TP1a_Tx7.s4p

C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx1_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx2_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx3_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx4_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx5_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx6_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP0_Tx8_to_TP1a_Tx7.s4p

C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx1_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx2_to_TP1a_Tx7.s4p
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C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx7_to_TP1a_Tx7.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP1a_Rx8_to_TP1a_Tx7.s4p
Chip-to-Module Channels

**XTLK Channel Files: Ingress Victim**

Host PCB Trace Length: 

```
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx1_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx2_to_TP5_Rx8.s4p
C2M_X(OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx3_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx4_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx5_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx6_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx7_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx8_to_TP5_Rx8.s4p

C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx1_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx2_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx3_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx4_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx5_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx6_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx7_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_FEXT_TP4a_Rx8_to_TP5_Rx8.s4p

C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx1_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx2_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx3_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx4_to_TP5_Rx8.s4p
C2M_X(OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx5_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx6_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx7_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx8_to_TP5_Rx8.s4p

C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx1_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx2_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx3_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx4_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx5_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx6_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx7_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_25C_NEXT_TP5_Tx8_to_TP5_Rx8.s4p
```
Chip-to-Module Channels

**XTLK Channel Files:**  Ingress Victim

Host PCB Trace Length:  \(### = [3, 5, 7, 9]\) in

C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx1_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx2_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx3_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx4_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx5_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx6_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx7_to_TP5_Rx8.s4p
C2M_X_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx8_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx1_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx2_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx3_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx4_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx5_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx6_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx7_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_FEXT_TP4a_Rx8_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx1_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx2_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx3_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx4_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx5_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx6_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx7_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx8_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx9_to_TP5_Rx8.s4p
C2M_Y_OSFP224_###in_host_PCB_80C_NEXT_TP5_Tx10_to_TP5_Rx8.s4p