Priority of Next Steps for P802.3dj Electrical Track – 7 December Update

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Introduction - Recap

- Significant progress on the 200G/lambda optical PMDs was made at the November 2023 Plenary meeting
- High-quality and comprehensive baseline proposals for 200G/lane electrical interfaces and electrical PHYs are urgently needed

- We need to prioritize our efforts to progress baselines in a timely manner
  - Updated 3dj TF timeline adopted last month

Priorities – Phase 1: January 2024

- AUI C2M loss target and EQ parameter values
- CR/KR EQ parameter values
- COM architecture and features for all electrical interfaces/PHYs
  - Define MLSE?
  - Define floating taps or keep fixed?
  - Decide which interfaces to apply them on: CR, KR, C2M, C2C?
- Electrical link training (LT): concept, interface usage (CR, KR, C2M, C2C), commonality
- AUI C2M host & module output TX settings (“fixed” vs. “adjustable”)

Priorities – Phase 2: March 2024

- AUI C2M transmitter and receiver compliance
  - Methodologies
  - Parameter values
- Electrical link training details: pattern, format, bit definitions, etc.
- AUI specification and measurement method: BER, CER, FLR, FEC symbol error ratio, PAM4 decision error ratio, etc.
- CR/KR transmitter and receiver compliance and CA channel test methods

Summary

- The electrical baseline effort is just beginning
  - It does not stop in January, nor March, nor May, nor…
- There are many dependencies between the different electrical interfaces and electrical PHYs
  - There will likely be departures from previous conventions, and will require offline consensus building
- Resolving Phase 1 priorities no later than January 2024 is vital to progress the electrical baselines
  - Consensus contributions help us to summarize agreement and identify gaps
  - Please engage me and electrical track editors in contribution developments