KEYSIGHT

Report out on 212.5Gbps TP2 and TP1a Phy layer measurement capabilities, relevant to IEEE 802.3dj baseline proposals

Rev 4.9-R6
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Presenters: John Calvin/Hadrien Louchet (Keysight)
Contributors: Robert Sleigh (Keysight)
Ray Schmelzer (Wilder Technologies)

Contributors and Supporters

- Rick Rabinovich (Keysight)
- Steve Sekel(Wilder Technologies)
- Richard Mellitz (Samtec)
- Geoff Zhang (AMD)
- Phil Sun (Credo)
- Adee Ran (Cisco)

212Gbps physical layer measurement validation Objectives:

Priority: 1

TP1a come up with VEC and EH at ~30dB. All on PRBS13Q's

Core validation framework around an extension of clause 120G to 212G:

TP1a electrical validation. Taking into account current proposed (pick one) reference equalization strategies.
Jitter (4 measurements), VEC, SNDR, SNR ISI (not included in this analysis, future presentation),

Priority: 2

TP2 jitter at 23dB PRBS13Q's

Are clause 162 techniques viable at 212Gbps?

Goal: Collect above measurements with preliminary channels in mind.

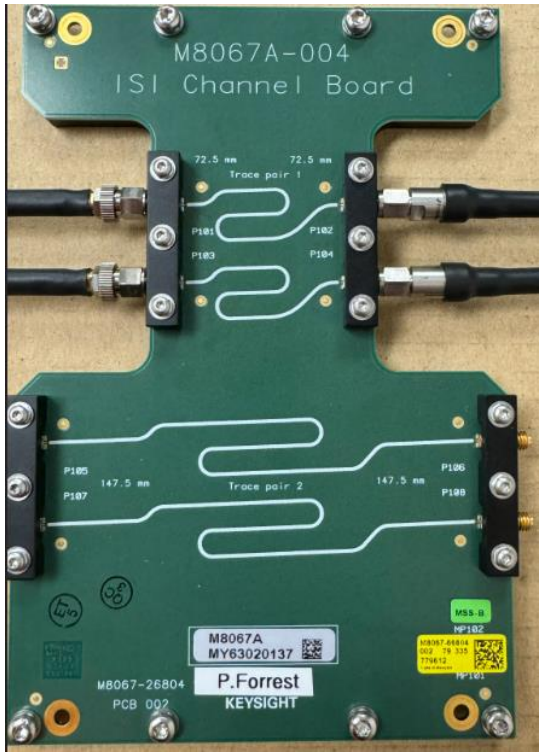
212G, (HH-HL) Channel

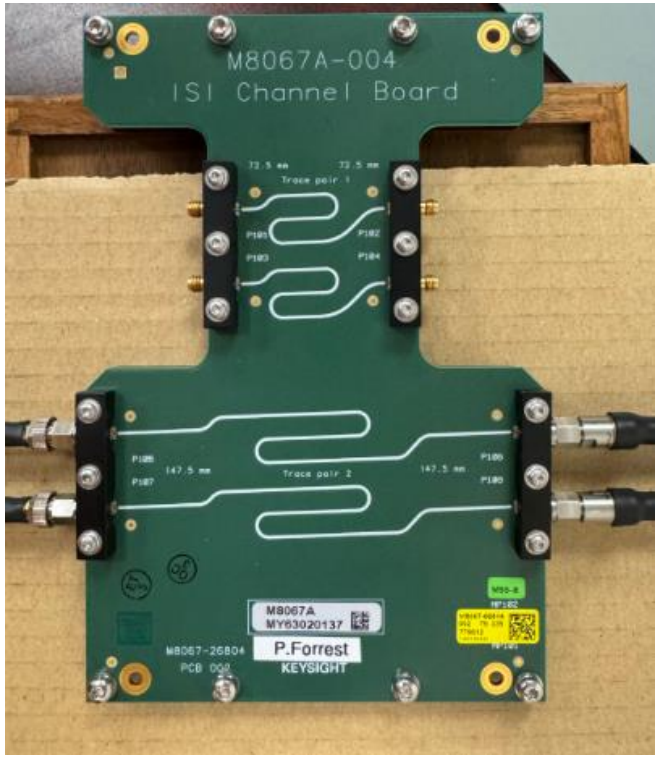
If work-arounds are needed, document and *discuss*.

Channel configurations used in this study:

Closest attainable physical proxies for:
CR/TP2 targeting (HH-HL) 22.35dB
C2M/TP1a targeting (HL-HL) ~33dB

Reference : https://www.ieee802.org/3/dj/public/23_11/diminico_3dj_01_2311.pdf pg 9





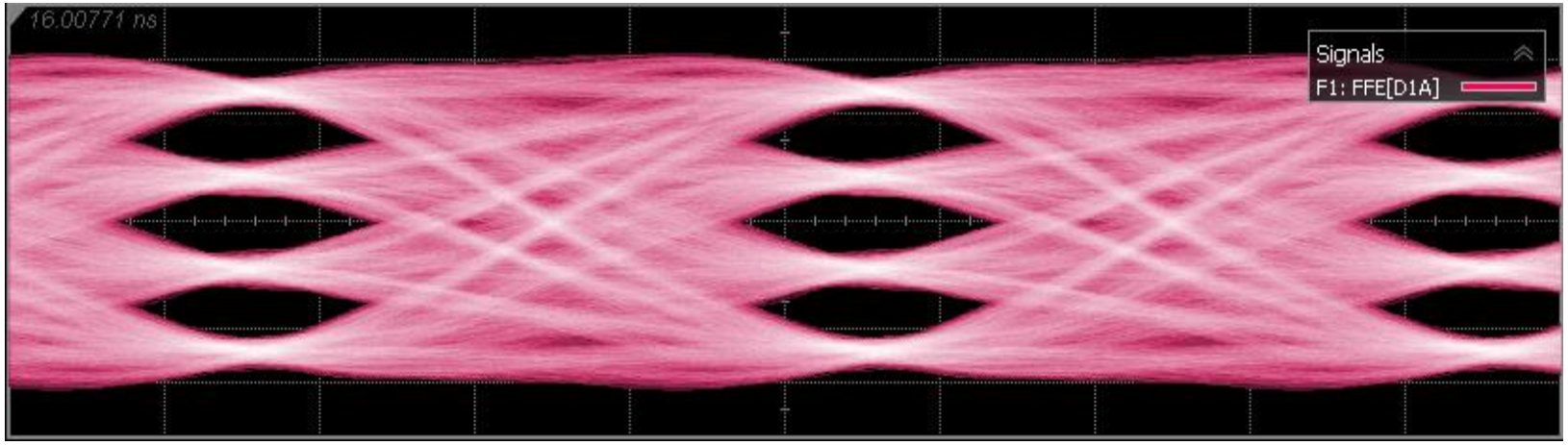
TP0d Instrument direct setup

Pattern Acquisition (0%)

Graphs | Output Jitter

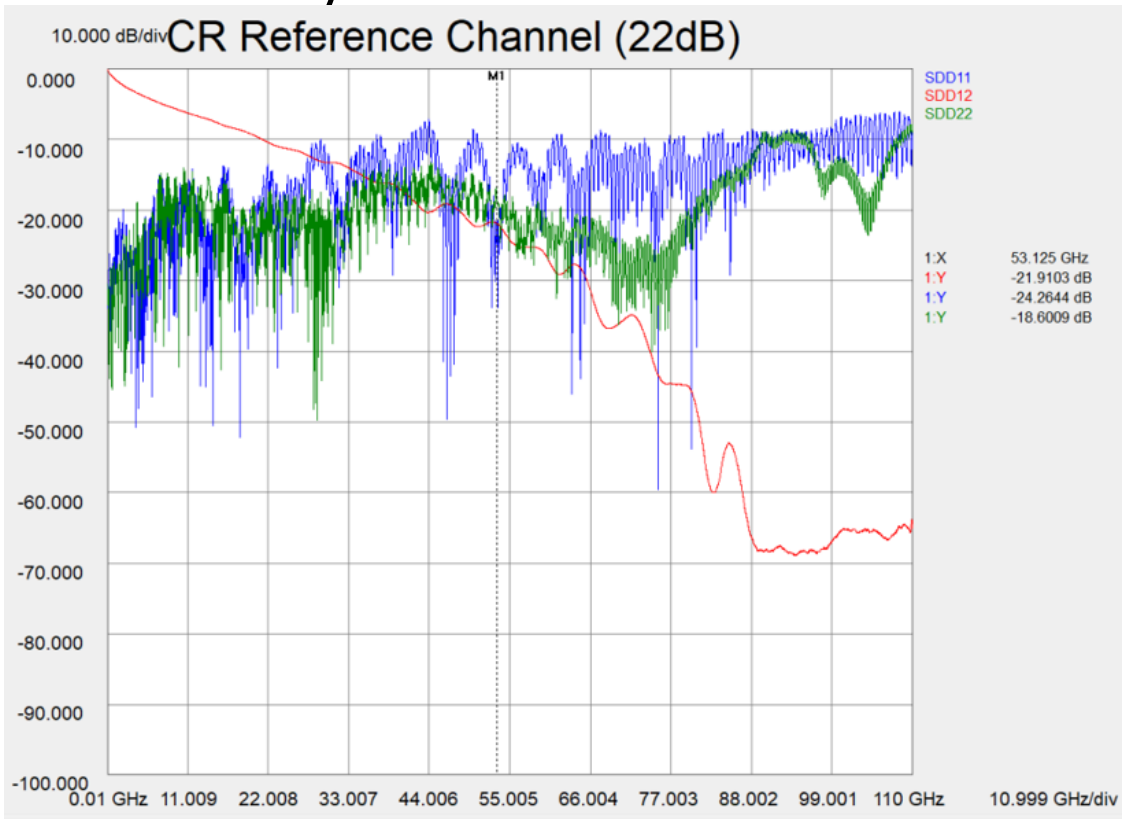
Src: JM Rate: 106.25000 GBd Pat. Length: 8191

Measurement	To L0	To L1	To L2	To L3
J3u (All)	133 mUI			
J3u (R03/F30)	112 mUI			
From L3	109 mUI	115 mUI	132 mUI	--
From L2	115 mUI	131 mUI	--	145 mUI
From L1	142 mUI	--	136 mUI	114 mUI
From L0	--	145 mUI	117 mUI	115 mUI
Jrms (All)	19.6 mUI			
Jrms (R03/F30)	17.0 mUI			
From L3	16.5 mUI	17.5 mUI	20.4 mUI	--
From L2	17.6 mUI	19.8 mUI	--	22.3 mUI
From L1	21.4 mUI	--	20.7 mUI	17.4 mUI
From L0	--	22.2 mUI	17.9 mUI	17.5 mUI
EOJ (All)	19 mUI			
EOJ (R03/F30)	6 mUI			
From L3	1 mUI	9 mUI	14 mUI	--
From L2	4 mUI	1 mUI	--	19 mUI
From L1	2 mUI	--	12 mUI	0 UI
From L0	--	18 mUI	11 mUI	6 mUI



TP0d Conditions:
80GHz 4BT
Direct Measurement from outputs of generator's remote head
Explicit clocking (no CDR, results in slightly higher Jitter values)
Instrument grade TX with 700mV SE/ 1.4V Differential
7 TAP FFE (3 Pre)

Approximate CR Channel: Instrument Grade Host Loss (M8067A-004-Trace 1) and 1mm based OSFP MTF Assembly



config_com_ieee8023_93a=df_200G_PAM4_RXFFE_CAKR_10-05-2023_60_60taps

CR (TP2) Measurements, after 22dB channel used in previous slide

Conditions:

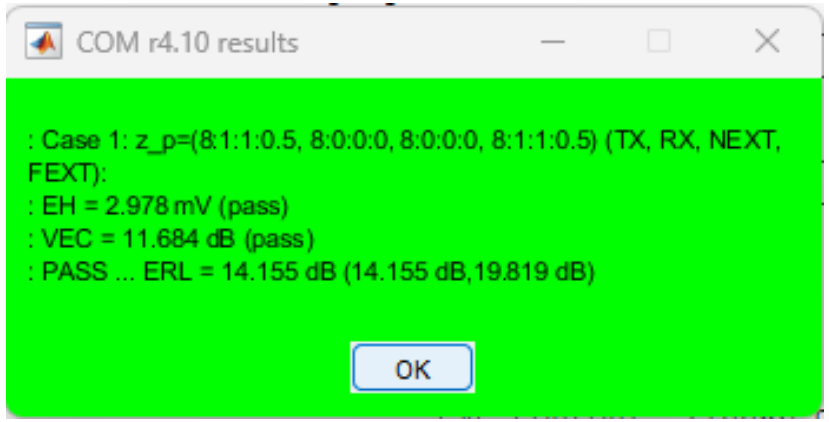
- 80GHz 4BT
- Explicit clocking (no CDR)
- Instrument grade TX (M8050) with 700mV SE/ 1.4V Differential
- No TX FFE

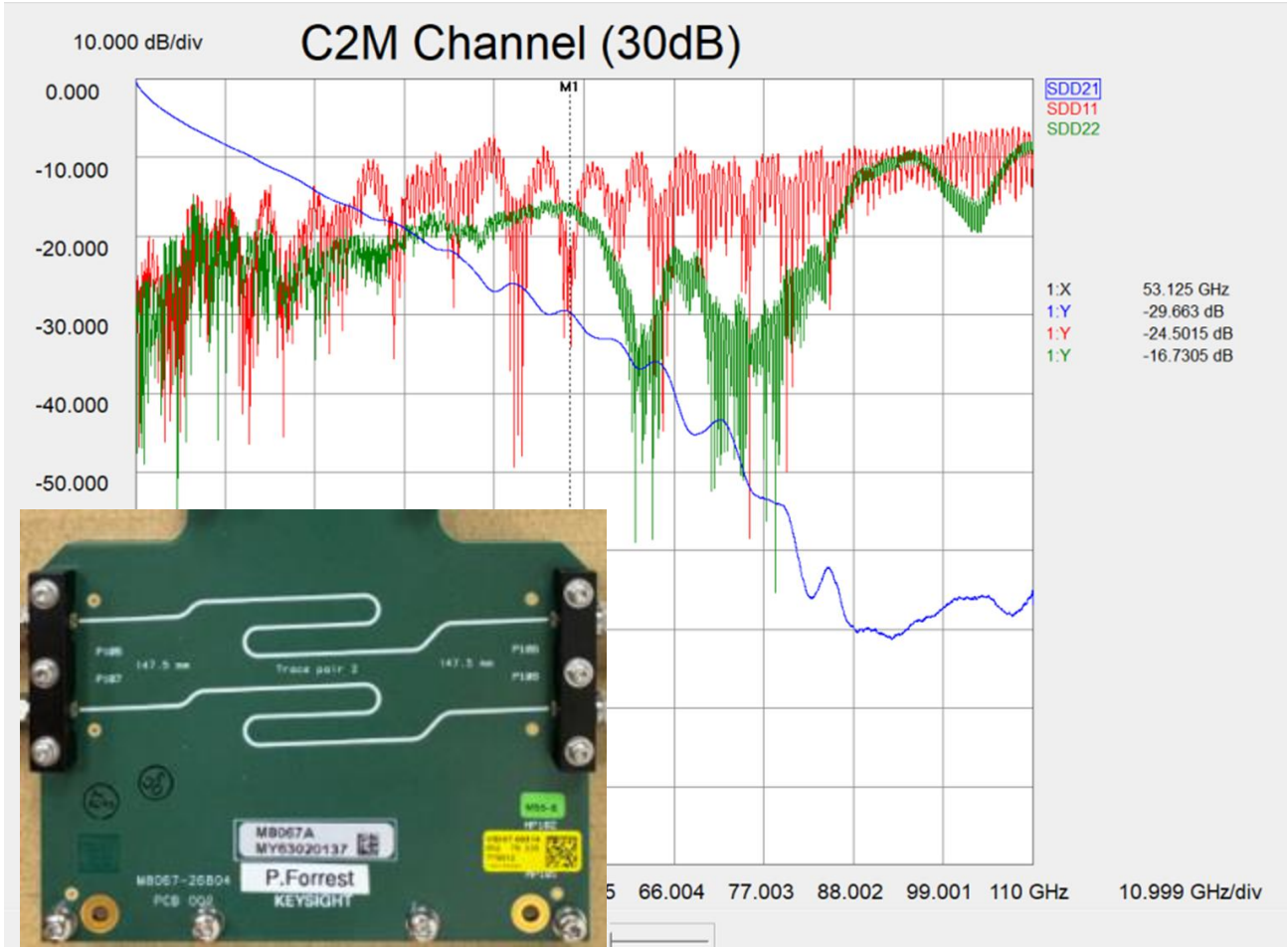
Leveraging TP2/Clause 162 methods for 802.3dj seems reasonable.

Will likely want to revisit EOJ to leverage higher PLL frequency (e.g. 8+MHz) to eliminate pattern harmonic contributions from the measurement.

Note: EOJ is high here (20mUI should be 2x lower) and is a measurement aberration from the strong 1'st (3.2MHz) and 2'nd (6.4MHz) pattern harmonic that equivalent time instruments are uniquely sensitive to.

Channels (C2M)): Instrument Grade Host Loss (M8067A-004-Trace 2) and 1mm based Wilder OSFP MTF Assembly





Instrument based EH/VEC operations here are very challenging. The high loss (and associated RX EQ) introduces some non-linear behavior.
60 Tap RX FFE + 8 Tap DFE needed to get anything useful here.

config_com_ieee8023_93a=df_200G_PAM4_RXFFE_C2M_12-18-2023_TDMODE_zero

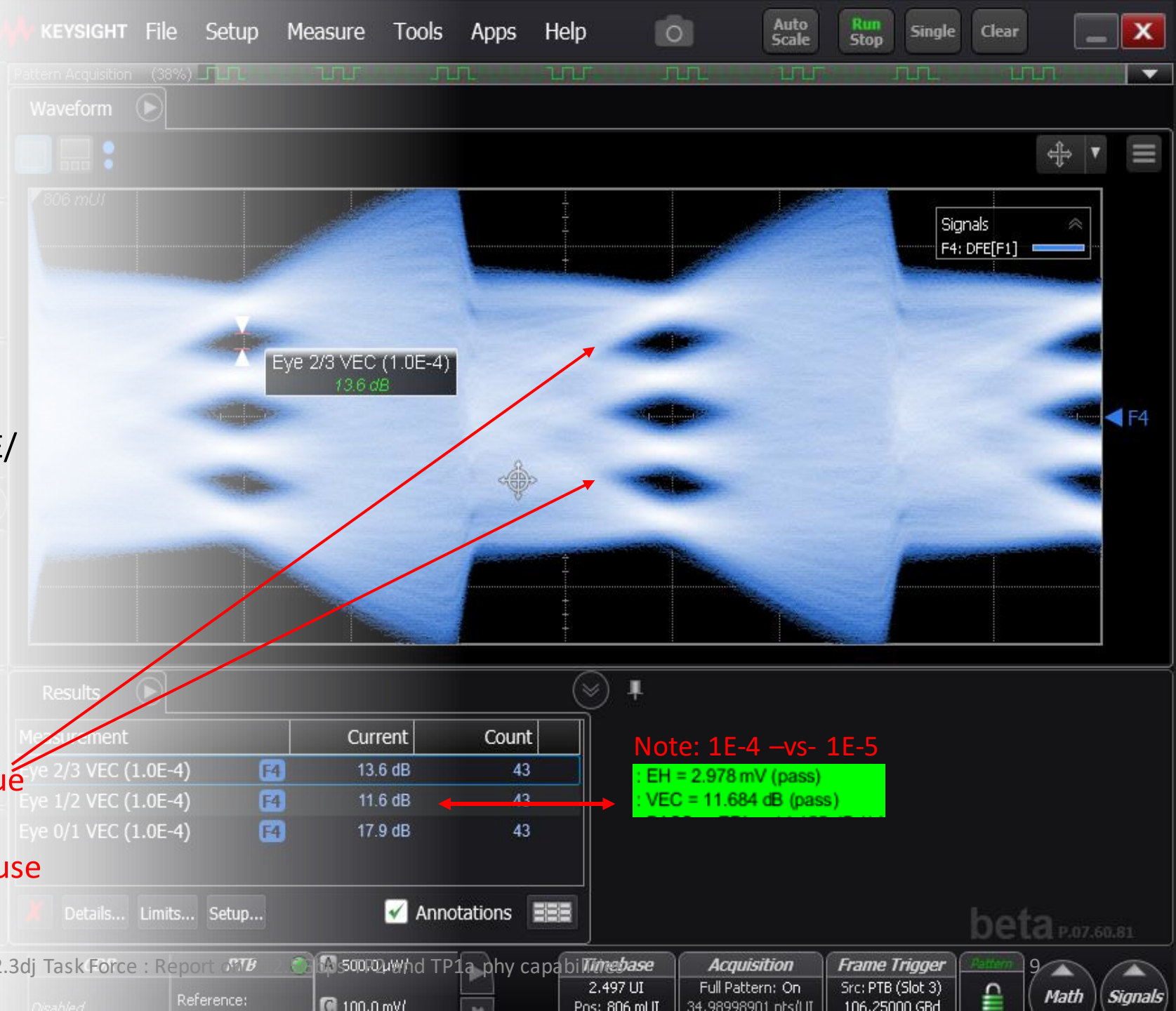
TP1A (30dB, RXFFE(16/60) + DFE (8)+ VEC@1E-4

Conditions:

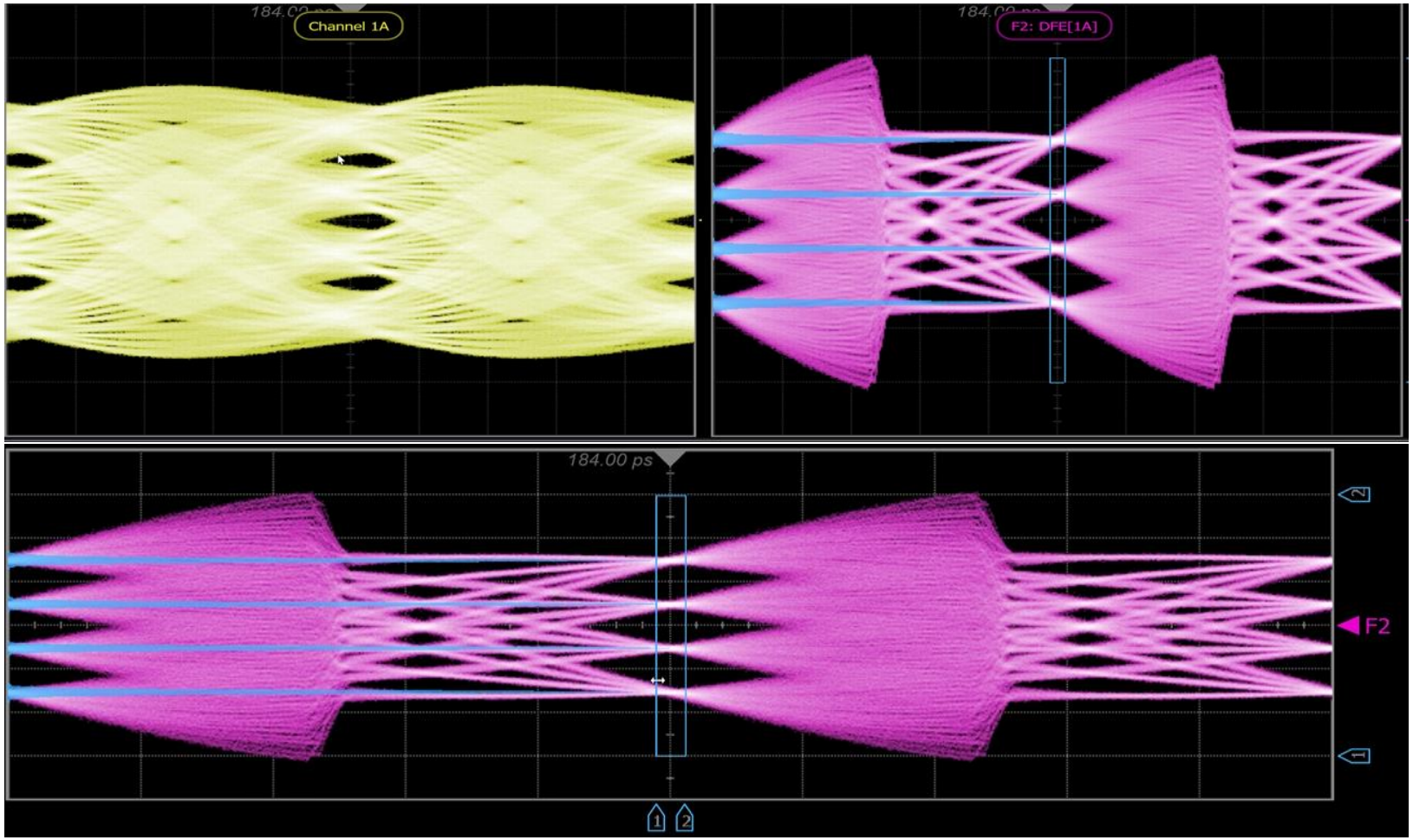
- 80GHz 4BT
- Explicit clocking (no CDR)
- Instrument grade TX with 700mV SE/ 1.4V Differential
- No TX FFE
- No RX CTLE
- No Input Referred Noise
- t_s via Mueller-Muller

Optimize at a point (t_s). Windowing around this point causes worse VEC due to "canted" behavior of DFE outputs.

Recommend revisiting methods in clause 120E.4.3 (Vertical eye closure) or re-write to operate with *MLSE*..



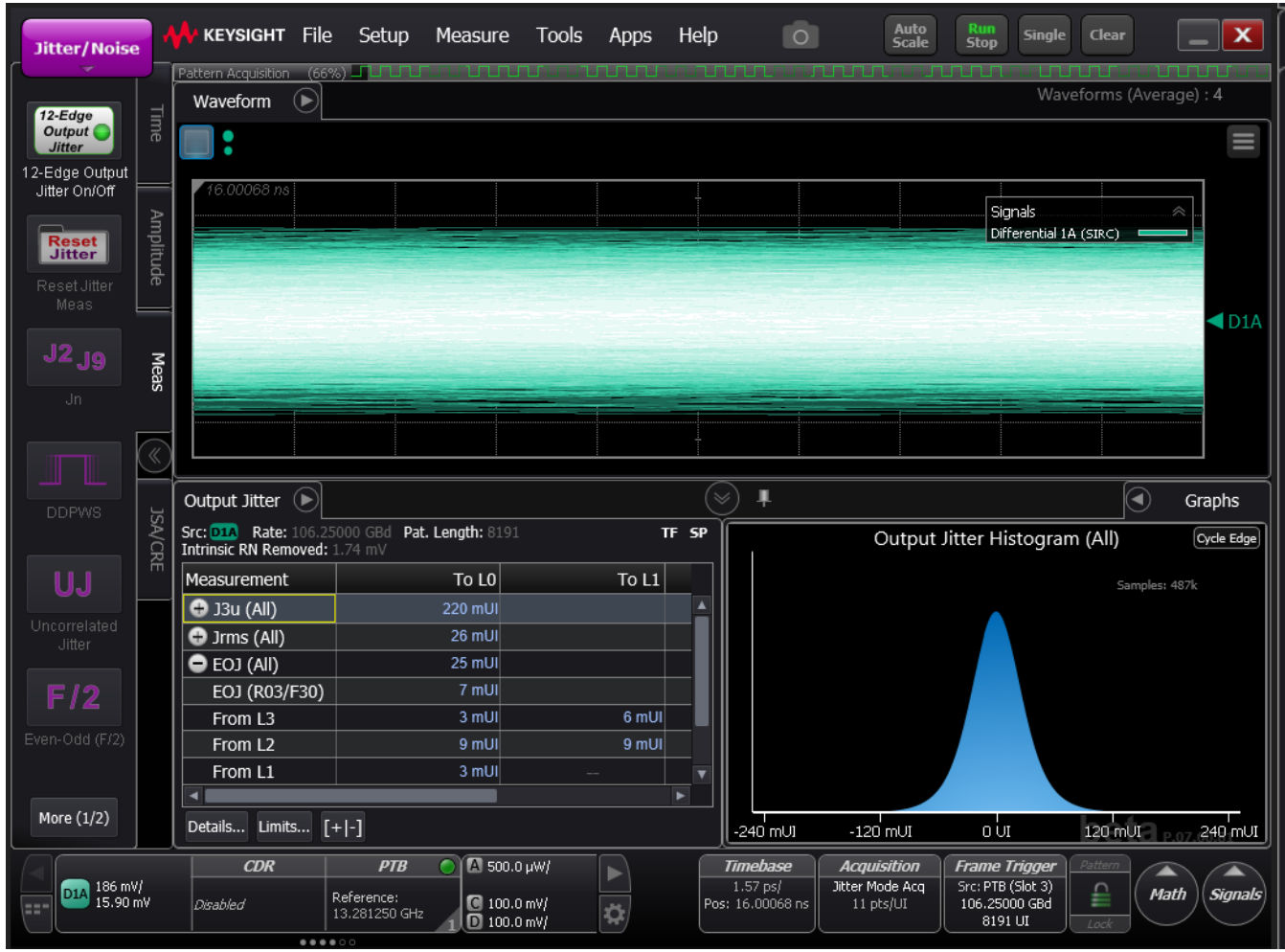
VEC revision (Proposed)



Abandon the Mueller-Muller for t_s.
Perform a best fit t_s based on optimization of EH/VEC.

Continue Minimum EH criteria?
Just focus on VEC.

What If: We apply Clause 162 to TP2?
Jnu at 30+ dB is less of a headache than VEC



Graphs | Output Jitter

Src: JM Rate: 106.25000 GBd Pat. Length: 8191
Intrinsic RN Removed: 1.74 mV

Measurement	To L0	To L1	To L2	To L3
J3u (All)	220 mUI			
J3u (R03/F30)	126 mUI			
From L3	123 mUI	140 mUI	225 mUI	--
From L2	150 mUI	265 mUI	--	215 mUI
From L1	260 mUI	--	205 mUI	130 mUI
From L0	--	190 mUI	136 mUI	127 mUI
Jrms (All)	26 mUI			
Jrms (R03/F30)	19.0 mUI			
From L3	18.7 mUI	21.0 mUI	34 mUI	--
From L2	22.2 mUI	36 mUI	--	32.5 mUI
From L1	34 mUI	--	29.5 mUI	21 mUI
From L0	--	28 mUI	20.6 mUI	19.2 mUI
EOJ (All)	25 mUI			
EOJ (R03/F30)	7 mUI			
From L3	3 mUI	6 mUI	24 mUI	--
From L2	9 mUI	9 mUI	--	25 mUI
From L1	3 mUI	--	8 mUI	4 mUI
From L0	--	21 mUI	14 mUI	7 mUI

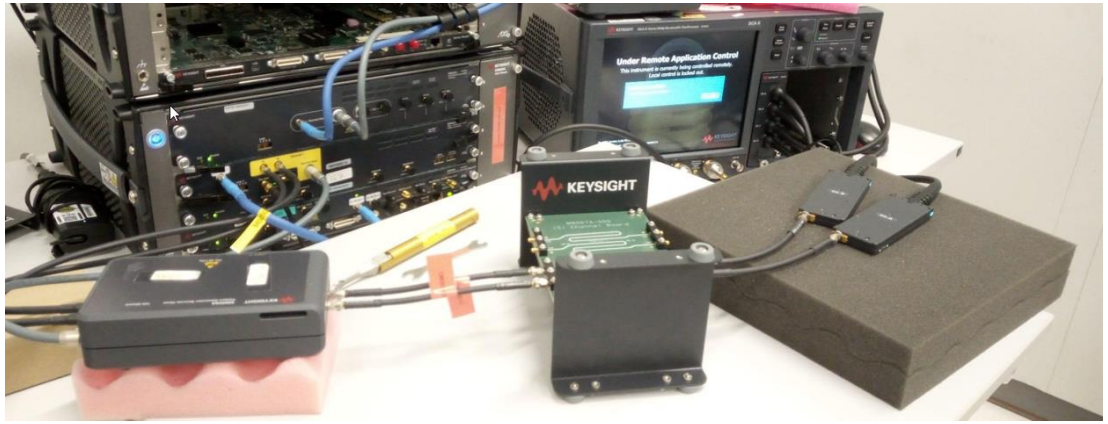
Wish List: Remove Rn effects from Jitter. If we want to keep it reference the fastest edge.
We already account for Rn in the Sigma-n calculation in SNDR, no need to account for it twice.
RSS average the Jnu composite in math. Don't "Combine" the histograms (120D.3.1.8.1) just do math on individual Jnu scalars for the 12 edges and "do the right thing"

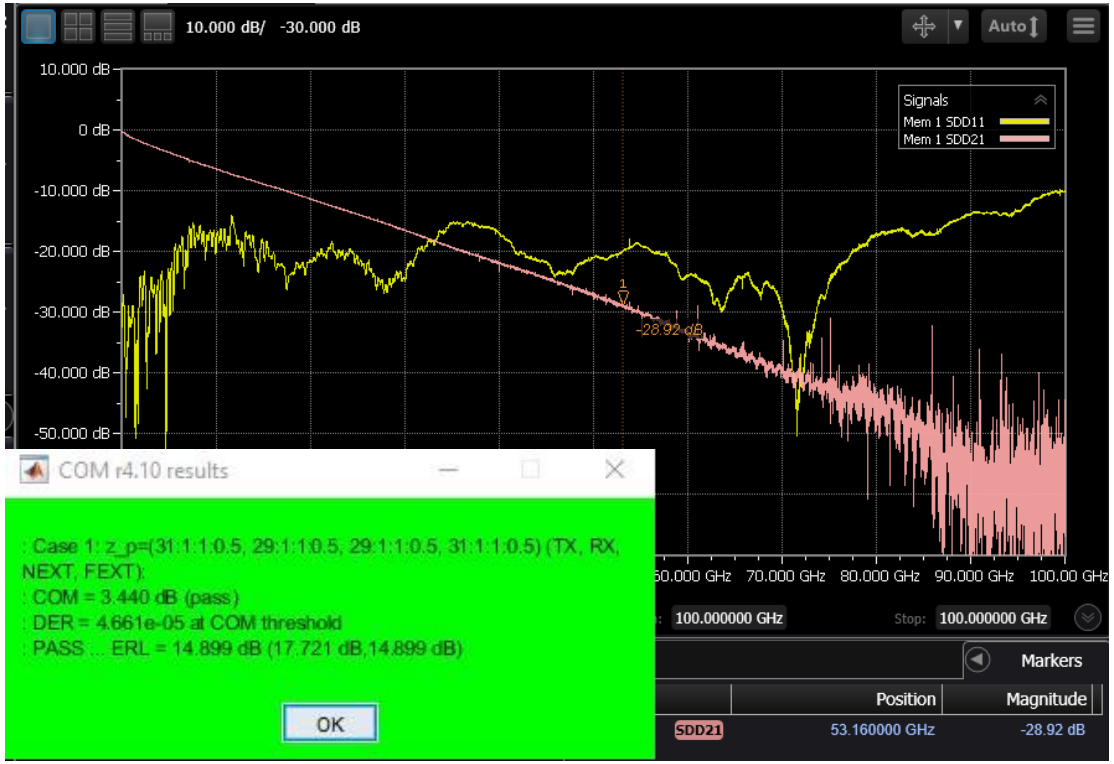
Summary

- TP2 measurement techniques from clause 162 with “adjusted” limits is effective and suitable to scale forward to 212.5Gbps with “minor” changes.
- TP1a measurement techniques from clause 120G needs a very strong reference receiver implementation to extract meaningful EH measurements which are a precursor to VEC.
  - Noise from this deep (60 tap RX FFE) is an issue and can be handled with averaging.
  - Additional dialogs around other equalization methods would be appropriate here.
- C2M and CR, instrument grade Host Channel and 212.5Gbps MTF S4P’s are available from this exercise that pass COM.

Backup-Notes

Work from previous contributions related to channel loss profiles and COM tables.





212.5 Gb/s Measurement with 30dB channel

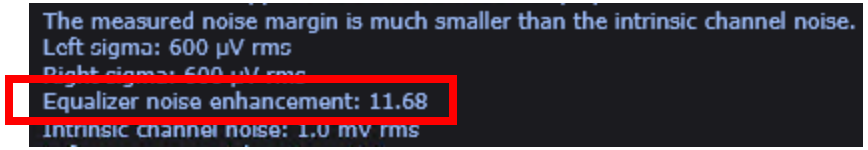
"C2M channel condition" with a new channel

- M8042A PG
  - no Tx de-emphasis
- M8067A-005-Trace 2
  - 29dB @53.125GHz
- N1000A+N1046A Sampling scope
  - Explicit Clock
  - SIRC: 80GHz 4th order Bessel
  - Input referred noise 6e-9V²/GHz

C2M measurement with 30dB channel

15 taps FFE to open the eye

- large noise enhancement (no Tx de-emphasis)



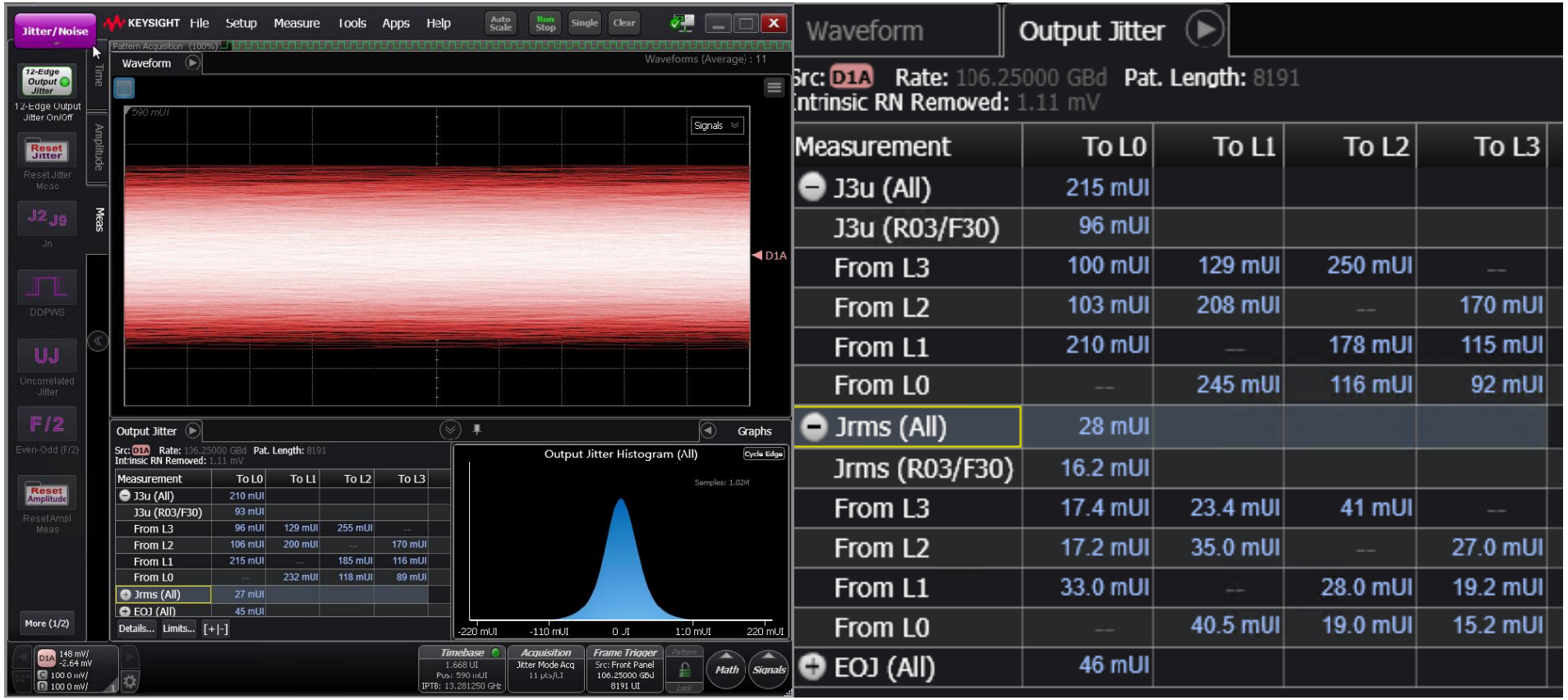
- Eyes still closed at 1e-5 probability but VEC/EH measurement possible at 1e-4 probability
- DDJ/ISI-J main contributor to TJ Jitter
  - 850mUI TJ (1e-4) → 760mUI DDJ
  - Non-compensable DDJ? Issue with the algorithm to open the eye? Something else?

→ Is 1e-5 measurement probability necessary if MLSD is expected to follow?

12-edge Jitter measurement with 30dB channel

Jitter measurements (Jnu, Jrms, EOJ) possible after 30dB channel

(potential negative impact of CDR and Tx de-emphasis to be investigated)



Waveform | Output Jitter

Src: D1A Rate: 106.25000 GBd Pat. Length: 8191
Intrinsic RN Removed: 1.11 mV

Measurement	To L0	To L1	To L2	To L3
J3u (All)	215 mUI			
J3u (R03/F30)	96 mUI			
From L3	100 mUI	129 mUI	250 mUI	--
From L2	103 mUI	208 mUI	--	170 mUI
From L1	210 mUI	--	178 mUI	115 mUI
From L0	--	245 mUI	116 mUI	92 mUI
Jrms (All)	28 mUI			
Jrms (R03/F30)	16.2 mUI			
From L3	17.4 mUI	23.4 mUI	41 mUI	--
From L2	17.2 mUI	35.0 mUI	--	27.0 mUI
From L1	33.0 mUI	--	28.0 mUI	19.2 mUI
From L0	--	40.5 mUI	19.0 mUI	15.2 mUI
EOJ (All)	46 mUI			

In-line with jitter measurement reported in slide 11 for the C2M channel

212Gbps CR Channel Configurations

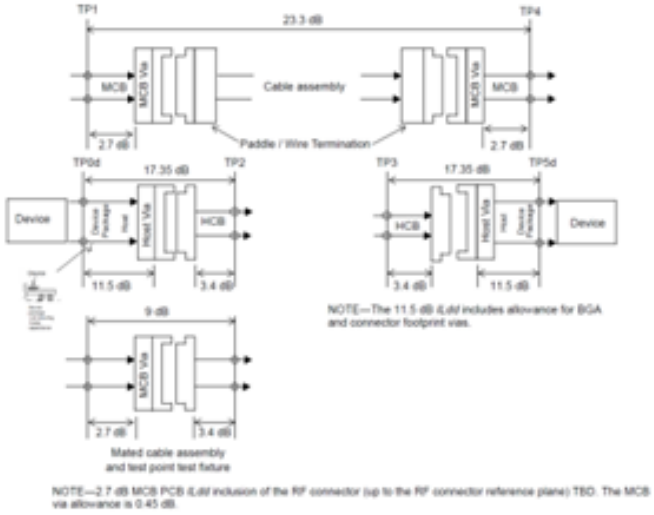
Reference : https://www.ieee802.org/3/dj/public/23_11/diminico_3dj_01_2311.pdf pg 9

Passive Copper Channels

TP2 (HH-HL) 22.35dB worst loss (validate)

IEEE P802.3dj Annex xxxA (informative)

- Flexible host architectures and cable assemblies HN-HN depicted

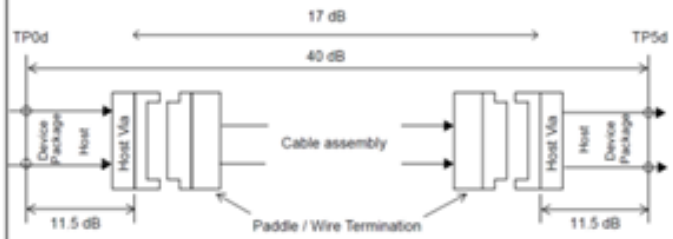


NOTE—The 11.5 dB *ILdd* includes allowance for BGA and connector footprint vias.

NOTE—2.7 dB MCB PCB *ILdd* inclusion of the RF connector (up to the RF connector reference plane) TBD. The MCB via allowance is 0.45 dB.

Figure XXXA–3—Cable assembly, host, and test fixture insertion loss at 53.125 GHz

Adopted



Die-to-die *ILdd* = 40 dB @ 53.125 GHz = 2*(11.5+2.45)+12.1

NOTE—Die-to-die *ILdd* derived from cable assembly host, and mated test fixture

Figure XXXA–4—Die-to-die insertion loss at 53.125 GHz

- Informative annex with inclusion of flexible host architectures and cable assemblies IL dB @53.125 GHz

Cable Assembly	Link Configurations IL	TP0d-TP2 IL (dB)	TP3-TP5d IL (dB	Cable +2*connectors IL (dB)	TP1-TP4 IL (dB)	MTF IL (dB)	Die-to-die IL (dB)
CA-A	HH-HN	22.35	17.35	12	18.3	9	40
CA-B	HH-HL	22.35	12.35	17	23.3	9	40
CA-B - depicted	HN-HN	17.35	17.35	17	23.3	9	40
CA-C	HN-HL	17.35	12.35	22	28.3	9	40
CA-D	HL-HL	12.35	12.35	27	33.3	9	40

9

802.3dj Task Force

Channel loss summary references (Prior contributions)

https://www.ieee802.org/3/dj/public/23_11/tracy_3dj_01a_2311.pdf

Proposed CR die-to-die Informative Annex - Insertion Loss @53.125 GHz, page 1

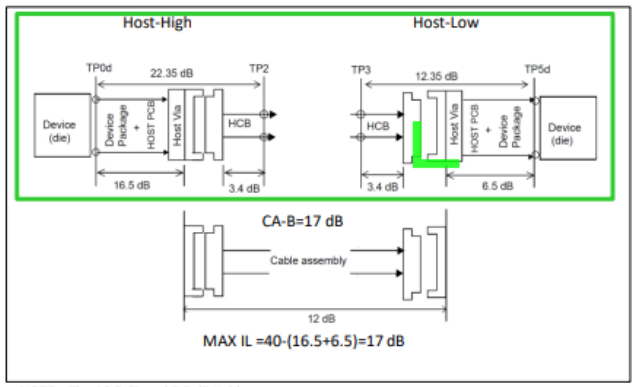
- Flexible host architectures and cable assemblies

Link Configurations IL (TX to RX)

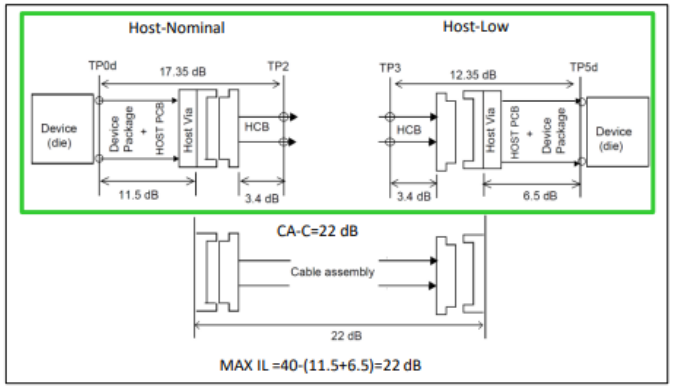
Device Package + Host PCB	Host-Low 6.5 dB	Host-Nominal 11.5 dB	Host-High 16.5 dB
Host -Low 6.5 dB	CA-A,B,C,D	CA-A,B,C	CA-A,B
Host-Nominal 11.5 dB	CA-A,B,C	CA-A,B	CA-A
Host-High 16.5 dB	CA-A,B	CA-A	not supported

Cable Assembly	Insertion Loss Cable + 2*Connectors
CA-A	12 dB
CA-B	17 dB
CA-C	22 dB
CA-D	27 dB

Proposed baseline content



NOTE—The 16.5 dB and 6.5 dB ILdd includes allowance for BGA and connector footprint vias.



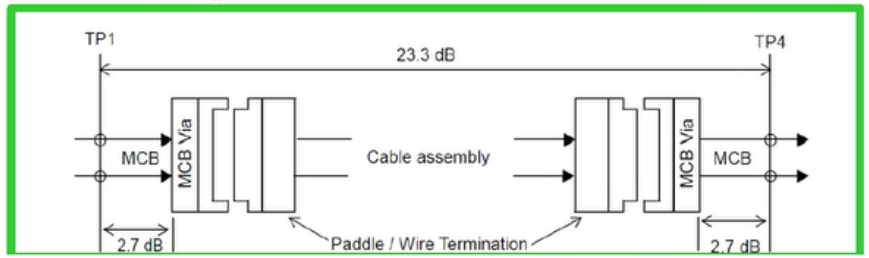
NOTE—The 11.5 dB and 6.5 dB ILdd includes allowance for BGA and connector footprint vias.

*Host Losses predicated on MTF IL assumptions https://www.ieee802.org/3/df/public/adhoc/electrical/22_0502/diminico_3df_01_220502.pdf slide 7

connector + MCB via is 2.9=9-(2.7+3.4)
connector is 2.45; it was 2 in earlier version; I thought thats what you asked...

On Tuesday, November 14, 2023 at 06:06:47 PM EST, cdimi80749@aol.com <cdimi80749@aol.com> wrote:

23.3 dB=17+((2*0.45)+(2*2.7))



On Tuesday, November 14, 2023 at 04:48:47 PM EST, Rick Rabinovich <rick.rabinovich@keysight.com> wrote:

Note: Module compliance board (MCB) is not shown and is the subject of a separate proposal

COM table for CR (Slide 6)

config_com_ieee8023_93a=df_200G_PAM4_RXFFE_CAKR_10-05-2023_60_60taps

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.413	V	vp/vf=
A_fe	0.413	V	vp/vf=
A_ne	0.45	V	
L	4		
M	32		
filter and Eq			
f_r	0.58	*fb	
c(0)	0.54		min
c(-1)	[-0.4:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.1]		[min:step:max]
c(-3)	0		[min:step:max]
c(-4)	0		[min:step:max]
c(1)	0		[min:step:max]
N_b	1	UI	
b_max(1)	0.75		As/dffe1
b_max(2..N_b)	0.3		As/dfe2..N_b
b_min(1)	0		As/dffe1
b_min(2..N_b)	-0.15	S	As/dfe2..N_b
g_DC	[-15:1:-3]	dB	[min:step:max]
f_z	25.16	GHz	
f_p1	40.00	GHz	
f_p2	56.00	GHz	
g_DC_HP	[-5:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\KRCR_1_{date}\	
SAVE_FIGURES	0	logical
Port Order	**[1 3 2 4]**	
RUNTAG	CRKR_eval_	
COM_CONTRIBUTION	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	6000	logical
TDR_Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	20	
fixture delay time	[0 0]	
Tukey_Window	1	
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	V^2/GHz
eta_0	6.00E-09	dB
SNR_TX	33	
R_LM	0.95	
benartsi_3df_01a_221	2.4 dB, 5.8 dB, 7 dB, 9.1 dB	
mli_3df_02_220316		
healey_3dj_01_2309	slide 6 rounded up	
lim_3dj_04_2309		

Table 93A–3 parameters			
Parameter	**Setting**	**Units**	Information
package_tl_gamma0_a1_a2	[0 0.0008455 0.000340225]		
package_tl_tau	0.00644805	ns/mm	
package_Z_c	[92 92 ; 70 70; 80 80; 100 100]	Ohm	
z_p select	[3]		[test cases to run]
z_p (TX)	[9 25 31 41 ; 1 1 1 1; 1 1 1 1 ; 0.5 0.5 0.5 0.5]	mm	[test cases]
z_p (NEXT)	[7 22 29 39 ; 1 1 1 1; 1 1 1 1 ; 0.5 0.5 0.5 0.5]	mm	[test cases]
z_p (FEXT)	[9 25 31 41 ; 1 1 1 1; 1 1 1 1 ; 0.5 0.5 0.5 0.5]	mm	[test cases]
z_p (RX)	[7 22 29 39 ; 1 1 1 1; 1 1 1 1 ; 0.5 0.5 0.5 0.5]	mm	[test cases]
C_p	[0.5e-4 0.5e-4]	nF	[TX RX]
Filter: Rx FFE			
ffe_pre_tap_len	6	UI	
ffe_post_tap_len	60	UI	
ffe_tap_step_size	0		
ffe_main_cursor_min	1		
ffe_pre_tap1_max	1		
ffe_post_tap1_max	1		
ffe_tapn_max	1		
Operational			
ERL Pass threshold	10	dB	
COM Pass threshold	3	db	
DER_0	1.00E-04		
T_r	0.00400	ns	
FORCE_TR	1	logical	
PMD_type	C2C		
EW	1		
MLSE	0	logical	
ts_anchor	1		
sample_adjustment	[-2 12]		
Local Search	2		

SAVE_CONFIG2MAT	1	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
ICN parameters		
f_v	0.278	Fb
f_f	0.278	Fb
f_n	0.278	Fb
f_2	61.625	GHz
A_ft	0.450	V
A_nt	0.450	V

Parameter	**Setting**	
board_tl_gamma0_a1_a2	*5.44084e-4 3.6036e-*	1.4 db/in @ 53.125G
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*32*	mm
z_bp (NEXT)	*32*	mm
z_bp (FEXT)	*32*	mm
z_bp (RX)	*32*	mm
C_0	[0.2e-4 0]	nF
C_1	[0.2e-4 0]	nF
Include PCB	**0**	**logical**
Seletions (rectangle, gaussian,dual_rayleigh,triangle		
Histogram_Window_Weight	gaussian	selection
Qr	*0.02*	UI

Floating Tap Control		
N_bg	0	0 1 2 or 3 groups
N_bf	4	taps per group
N_f	60	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps
B_float_RSS_MAX	0.2	rss tail tap limit
N_tail_start	61	(UI) start of tail taps limit

COM table for C2M (Slide 8)

config_com_ieee8023_93a=df_200G_PAM4_RXFFE_C2M_12-18-2023_TDMODE_zero

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[45 45]	Ohm	[TX RX]
A_v	0.386	V	vp/vf=
A_fe	0.386	V	vp/vf=
A_ne	0.6	V	
L	4		
M	32		
filter and Eq			
f_r	0.58	*fb	
c(0)	0.55		min
c(-1)	[-0.4:0.02:0]		[min:step:max]
c(-2)	[0:.02:0.1]		[min:step:max]
c(-3)	0		[min:step:max]
c(-4)	0		[min:step:max]
c(1)	[-0.2:0.05:0]		[min:step:max]
N_b	1	UI	
b_max(1)	0.75		As/dffe1
b_max(2..N_b)	1		As/dfe2..N_b
b_min(1)	0		As/dffe1
b_min(2..N_b)	-0.15	S	As/dfe2..N_b
g_DC	[-15:1:-3]	dB	[min:step:max]
f_z	25.16	GHz	
f_p1	40.00	GHz	
f_p2	56.00	GHz	
g_DC_HP	[-5:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
Butterworth	1	logical	include in fr
Local Search	2		
Force Peak Sample	1		
sor Minus Precurso	0		
sample_adjustment	[-16:16]		

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	0	logical
RESULT_DIR	.\results\C2M_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	2M TP1a_COMTD_MODE	
COM_CONTRIBUTION	0	logical
Operational		
ERL Pass threshold	10	dB
COM Pass threshold	3	db
VEC Pass threshold	12	mV
DER_0	2.50E-05	
T_r	4.00E-03	ns
FORCE_TR	1	logical
Min_VEO_Test	0	mV
PMD_type	C2M	
EH_min	-100	Value
EH_max	1000	Value
T_O	50	mUI
samples_for_C2M	100	amples/UI
EW	1	
MLSE	0	
TDMODE	0	
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	1000	logical
TDR_Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	20	
fixture delay time	[0 0]	
Tukey_Window	1	
Noise, jitter		UI
sigma_RJ	0.01221875	UI
A_DD	0.0286875	UI
eta_0	0.00E+00	V^2/GHz
SNR_TX	34	dB
R_LM	0.98	

Table 93A–3 parameters			
Parameter	Setting	Units	Information
package_tl_gamma0_a1_a2	[5e-4 0.00065 0.0003]		
package_tl_tau	0.006141	ns/mm	
package_Z_c	[92 92 ; 70 70; 80 80; 100 100]	Ohm	
z_p select	[1]		[test cases to run]
z_p (TX)	[8 24 30 45 ; 1 1 1 1; 1 1 1 1 ; 0.5 0.5 0.5 0.5]	mm	[test cases]
z_p (NEXT)	[8 8 8 8; 0 0 0 0 ;0 0 0 0 ;0 0 0 0]	mm	[test cases]
z_p (FEXT)	[8 24 30 45 ; 1 1 1 1; 1 1 1 1 ; 0.5 0.5 0.5 0.5]	mm	[test cases]
z_p (RX)	[8 8 8 8; 0 0 0 0 ;0 0 0 0 ;0 0 0 0]	mm	[test cases]
C_p	[0.4e-4 0.4e-4]	nF	[TX RX]
Floating Tap Control			
N_bg	0	0 1 2 or 3 groups	
N_bf	4	taps per group	
N_f	60	UI span for floating taps	
bmaxg	0.2	max DFE value for floating taps	
B_float_RSS_MAX	0.1	rss tail tap limit	
N_tail_start	61	(UI) start of tail taps limit	
Filter: Rx FFE			
ffe_pre_tap_len	6	UI	
ffe_post_tap_len	60	UI	may need to adjus
ffe_tap_step_size	0		
ffe_main_cursor_min	0.7		
ffe_pre_tap1_max	0.7		
ffe_post_tap1_max	0.7		
ffe_tapn_max	0.7		
ffe_backoff	0		

minutes_3cwdfdj_2309_unapproved	
benartsi_3dj_01_2311	
mli_3df_02_220316	
dc24 pg dca work	

SAVE_CONFIG2MAT	0	
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
ICN parameters		
f_v	0.588	Fb
f_f	0.278	Fb
f_n	0.278	Fb
f_2	61.625	GHz
A_ft	0.450	V
A_nt	0.450	V

Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 6.44084e-4 3.6036e-05]*	1.4 db/in @ 53.125G
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*32*	mm
z_bp (NEXT)	*32*	mm
z_bp (FEXT)	*32*	mm
z_bp (RX)	*32*	mm
C_0	[0.2e-4 0]	nF
C_1	[0.2e-4 0]	nF
Include PCB	**0**	**logical**
Seletions (rectangle, gaussian,dual_rayleigh,triangle		
Histogram_Window_Weigh	gaussian	selection
Qr	*0.02*	UI