AUI Types vs. FEC Partitioning

IEEE P802.3dj Optical ad hoc
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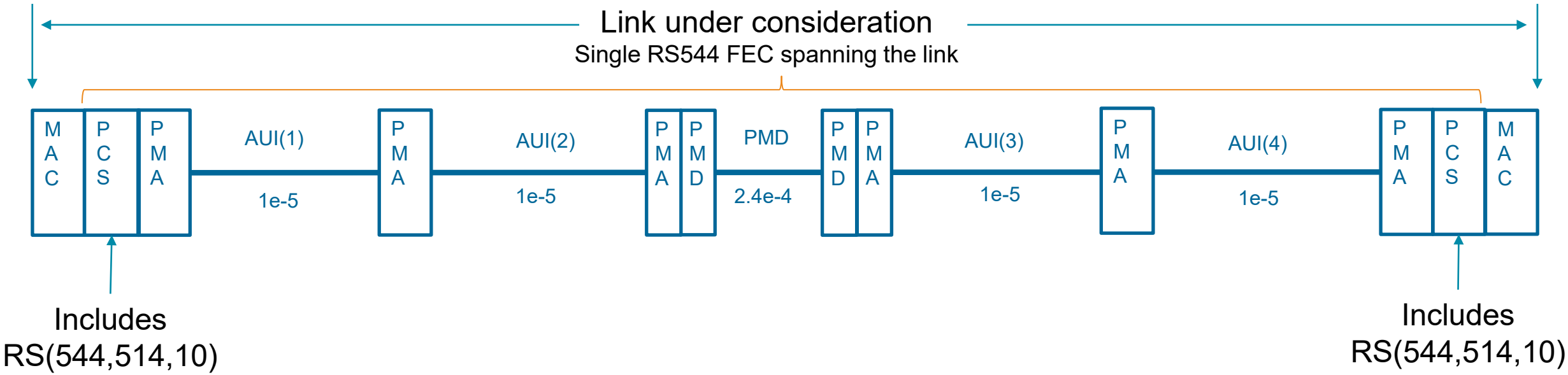
Introduction

- We are developing a standard that seeks to enable as many implementations as possible
  - Some instantiations of AUI's may require FEC partitioning
  - Target PHYs or PMDs may necessitate different FEC codes or partitioning

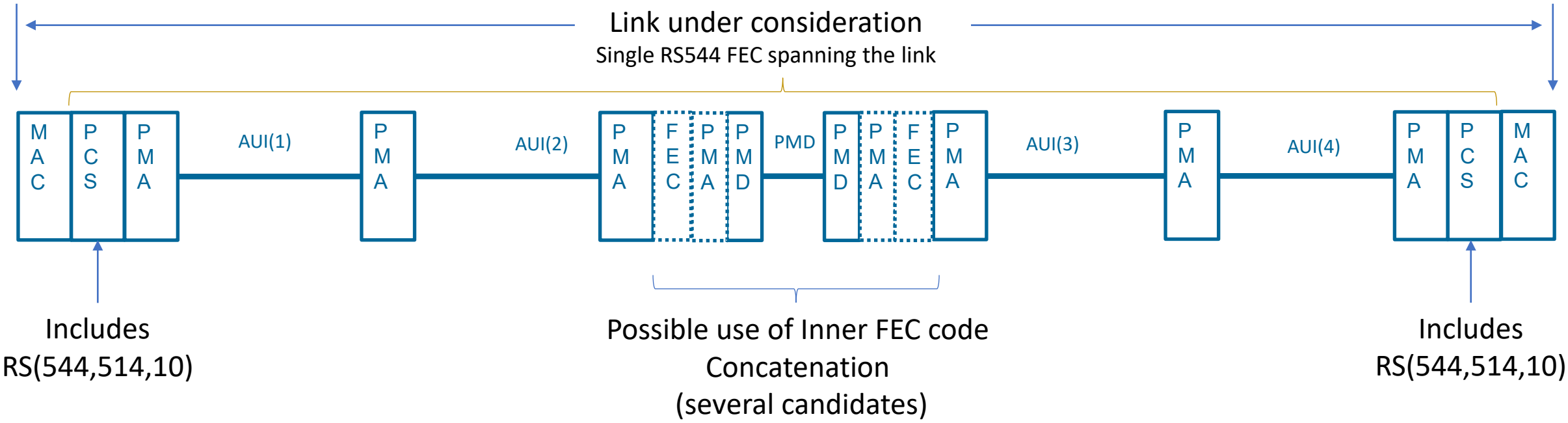
- Review of adopted logic architecture and its ability to support these various implementations

Recap – 400GbE Architecture at 100G/Lane



- AUI's absorb small portion of FEC budget (no high loss AUIs)
- Assumes random errors for optical PMD
- See Pete Anslow's analysis for end-to-end BER/FLR (see opsasnick_3df_logic_220630a.pdf for summary of references)

New considerations for 800 GbE



- Two different 200 Gb/s based AUI loss ranges
- Consideration of a concatenated FEC to support some optical PMDs
- Use of extender sublayers might be required to reset (segment) FEC due to increased utilization of FEC budget for AUI
- Usage of DFE/MLSE will increase error correlation (burstiness)
- Potential Symbol muxing for 200Gb/s AUI's needs to co-exist with bit-muxed 100Gb/s AUI's
- Successful P802.3dj adoption will need to consider all the above

- BER is used as a convenience in the rest of this presentation, but what really matters is FLR and properly accounting for burst errors

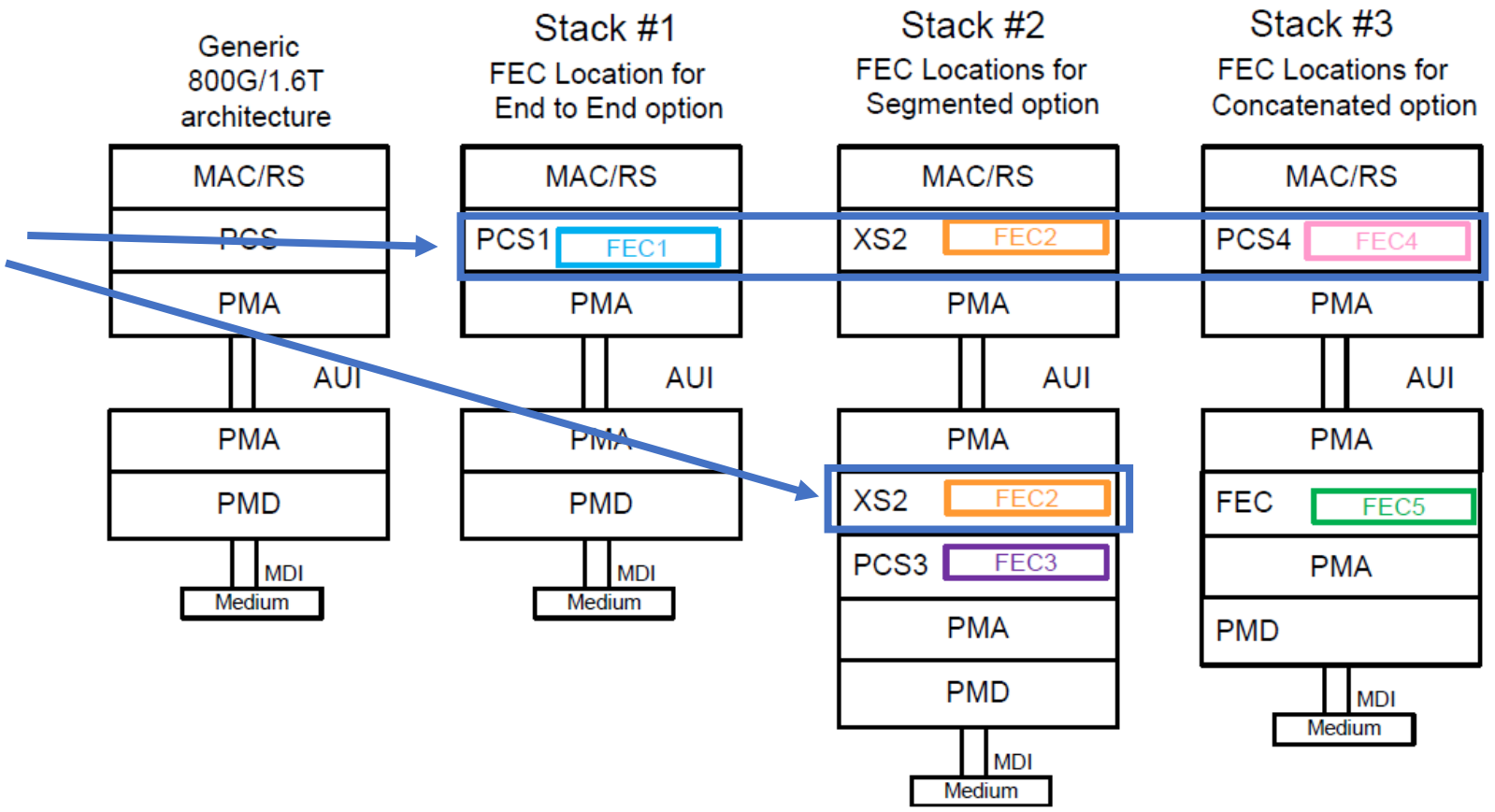
Adopted Logic Architecture for Reference

Proposed 800GbE/1.6TbE Architecture

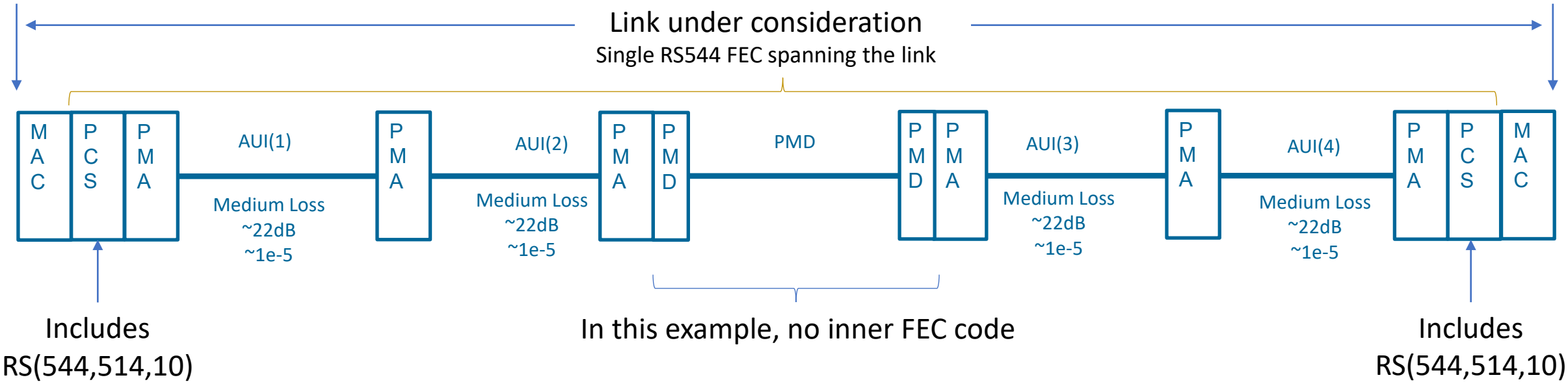
- How various FEC schemes fit into the architecture
- FECs might or might not be reused across schemes

FEC1 = End to End FEC
FEC2 = AUI FEC for Segmented
FEC3 = PMD FEC for Segmented
FEC4 = Outer FEC for Concatenated
FEC5 = Inner FEC for Concatenated

FEC for 200G/lane AUIs already adopted (RS(544))

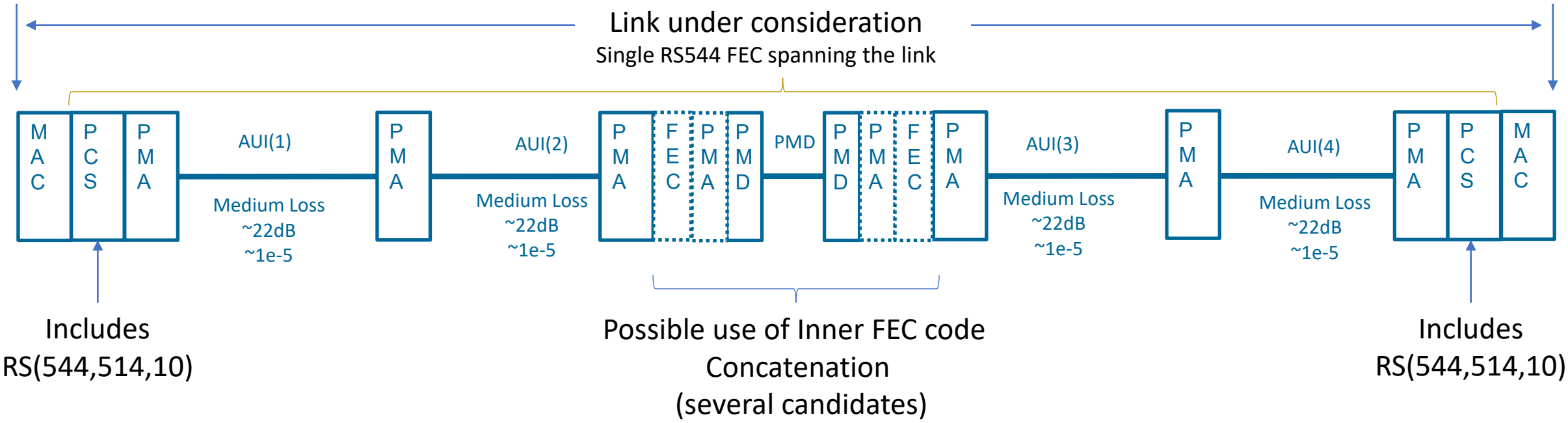


Only Medium Loss AUIs – No Inner FEC example



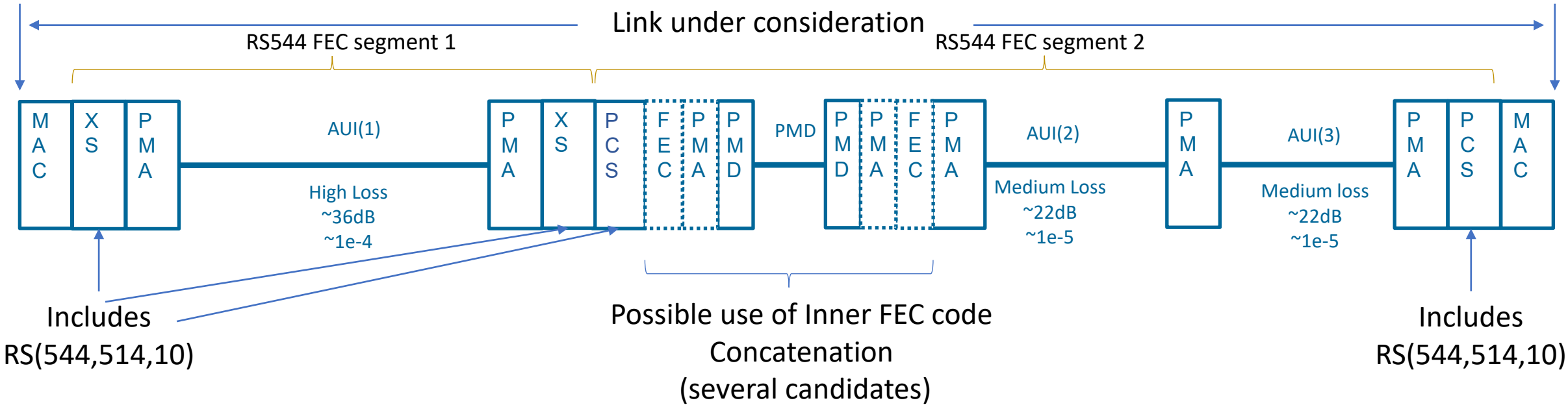
- No extender sublayers in this link
- Current assumption: Each AUI maintains a BER of ~1e-5, but may have worst case burst errors, needs more analysis
- The combination of the AUI and PMD link BERs must be analyzed, tradeoffs must be made
- Lowest latency option of the possible AUI configurations
- Assuming 200G AUIs; this also works for 100G AUIs

Only Medium Loss AUIs – With possible Inner FEC example



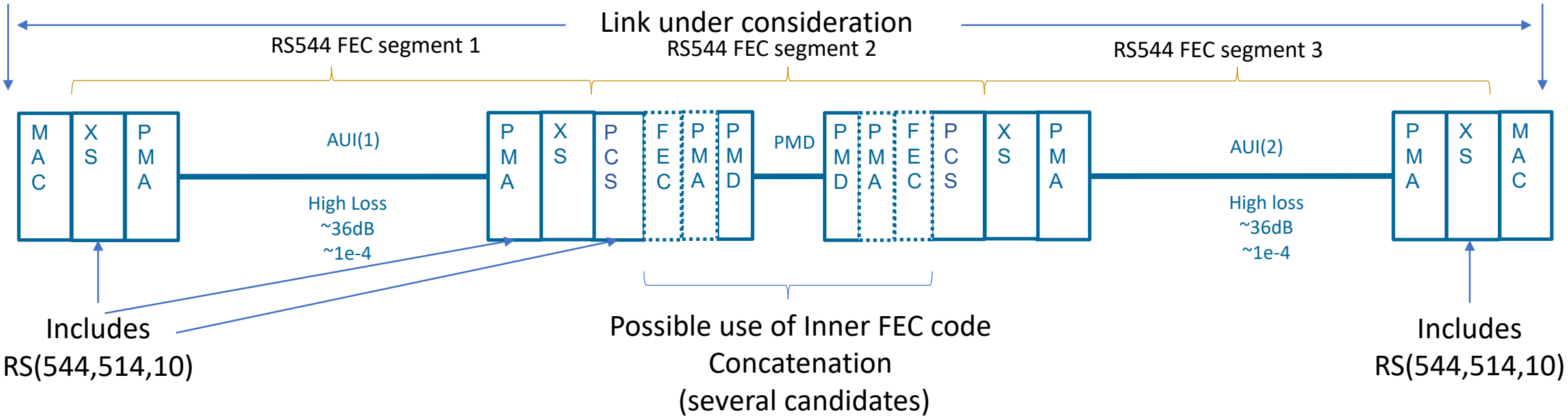
- No extender sublayers in this link
- Current assumption: Each AIU must maintain a BER of ~1e-5 , but may have worst case burst errors
- The combination of the AUI and PMD link BERs must be analyzed, tradeoffs must be made
- Lowest latency option of the possible AUI configurations (but inner FEC add latency)
- Assuming 200G AUIs; this also works for 100G AUIs

One High Loss AUI



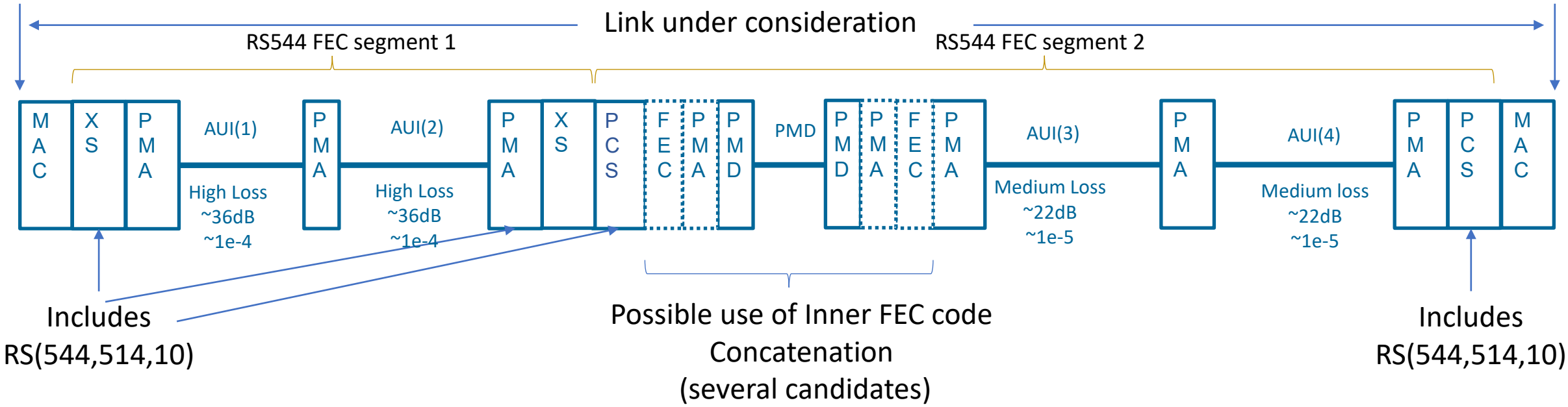
1. Current assumption: High loss AUIs targeting ~1e-4 require XS
   - Isolates errors from the high loss AUI
2. Higher latency option due to XS across the AUI(1) (does not consider FEC inner code decision)

Two High Loss AUIs



1. Current assumption: High loss AUIs targeting ~1e-4 require XS
   - Isolates errors from the high loss AUI
     - PMD can't take advantage of this, must support worst case
   - Two extenders in this example
2. Input BER to PMD portion of the link ~0
3. Highest latency option due to XS across the AUI(1) and AUI(2) (does not consider FEC inner code decision)

Two High Loss AUIs on one side



1. Current assumption: High loss AUIs targeting ~1e-4 require XS
   - Isolates errors from the high loss AUI
   - One extender in this example (covering two high loss AUIs)
2. Higher latency option (does not consider FEC inner code decision)

Summary

- The presentation looks at how the FEC partitioning is impacted by the AUI assumptions
  - How the FEC is segmented is dependent on the AUI type (medium or high loss)
- List of assumptions/Rules:
  - Medium loss AUIs don’t require XS
    - Targeting ~1e-5 BER
  - High loss AUIs must use and XS (extender) sublayer
    - Targeting ~1e-4 BER
    - Is this the right direction?
  - XS can cover up to two high loss AUIs (on one side of the link)
  - Detailed BER/FLR analysis is required to partition BER/FLR across the link

- Any FEC baseline proposal should include a BER/FLR partitioning analysis