FEC_I Sublayer Architecture Proposal for Type 2 PHYs

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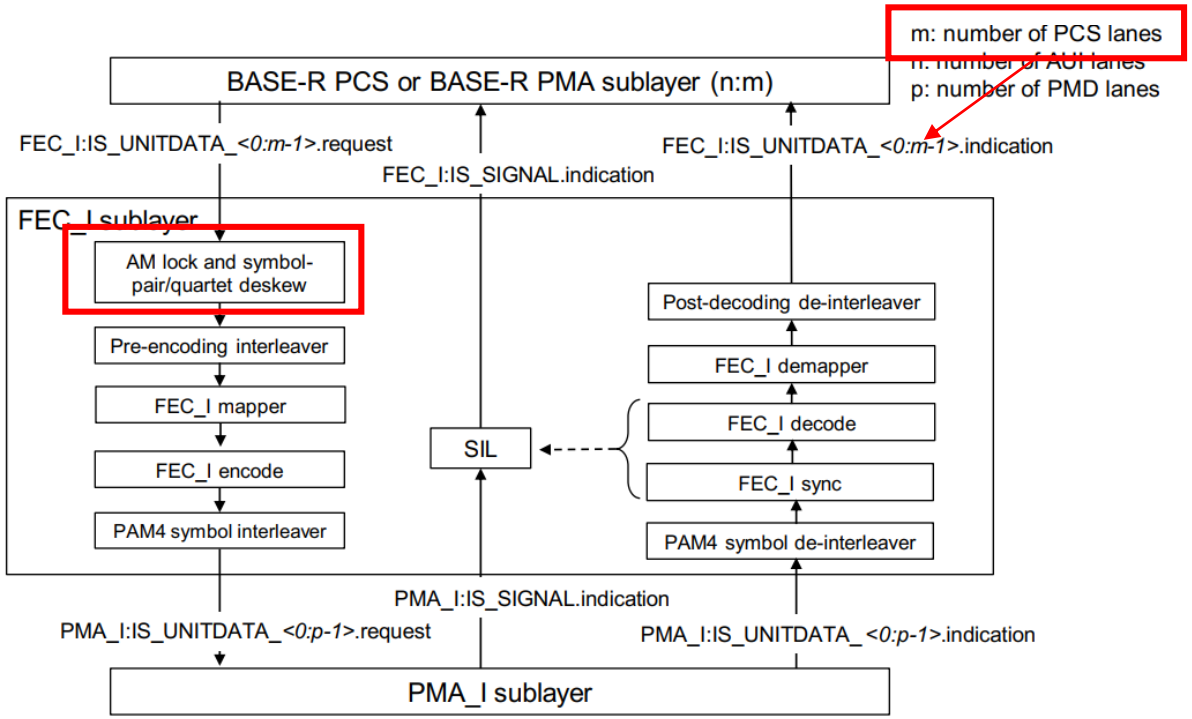
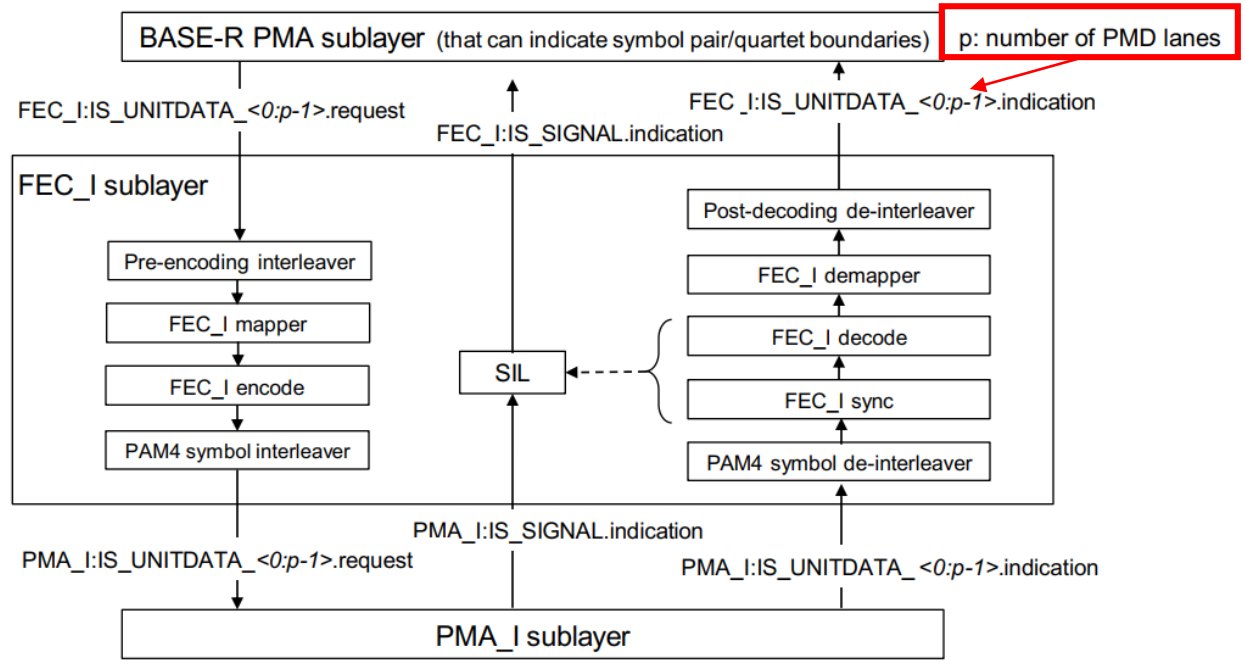
Introduction

- Type 2 PHY/FEC scheme has been adopted with Hamming(128,120) as the inner FEC.
  - See parthasarathy_3dj_02a_2303, and motions_3dfdj_2303.
  - Detailed design regarding convolutional interleaver and FEC lane rates are TBD.
- Symbol-pair muxing has been adopted for 200G/lane AUIs.
  - See ran_3dj_01a_2303, and motions_3dfdj_2303.
- Convolutional interleaver has been proposed to randomize errors from inner FEC.
  - See patra_3dj_01b_2303.pdf, huang_3df_01a_2211 and he_3dj_01a_230206.pdf.
  - Three different lane rates were proposed: 25G/lane, 100G/lane and 200G/lane.
  - The convolutional interleaver should be avoided for shorter PMDs due to high latency.
    - See he_3dj_02a_230206, dawe_3dj_01a_2303.
    - Latency impact has been analyzed in brown_3dj_optx_01b_230413 and brown_3dj_elec_01_230420.
- This presentation focuses on FEC_I lane rates, and recommend to use 200G/lane design.
  - Convolutional interleaver in the following slides could be excluded if not needed.

Architecture Overview

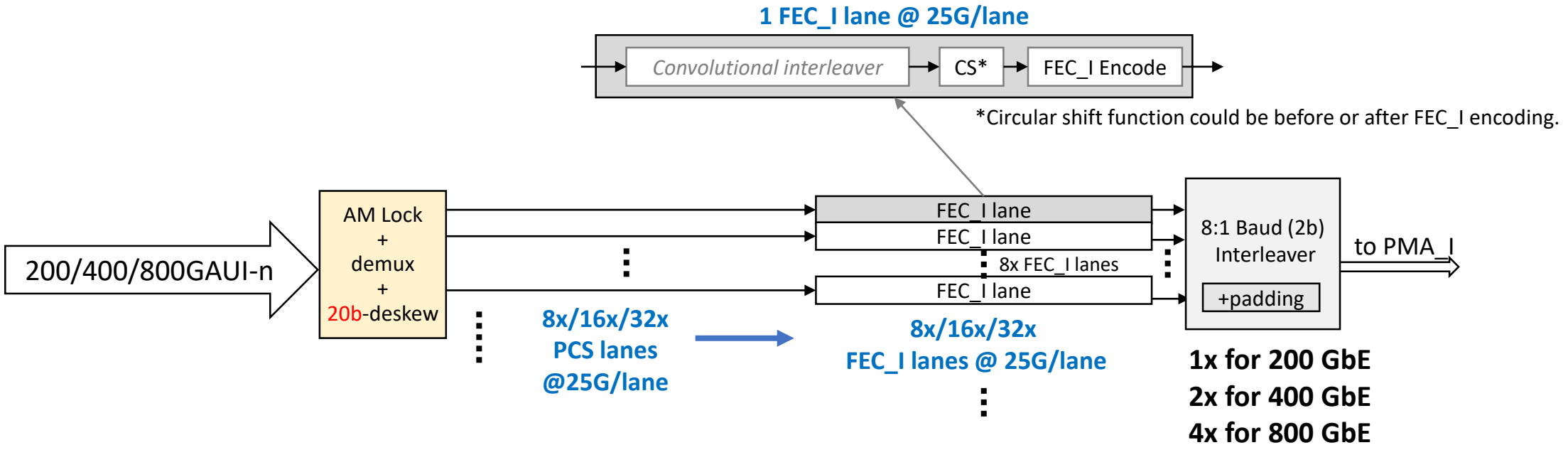
- The three FEC lane designs can be viewed as two main options, one has PCS lane based design, and the other has PMA/PMD lane based design.
  - Both options have exactly the same performance in terms of FEC gain.
  - Both options have the same number of bits storage for convolutional interleaver if used.





25G/lane Design – 200 GbE, 400 GbE and 800 GbE

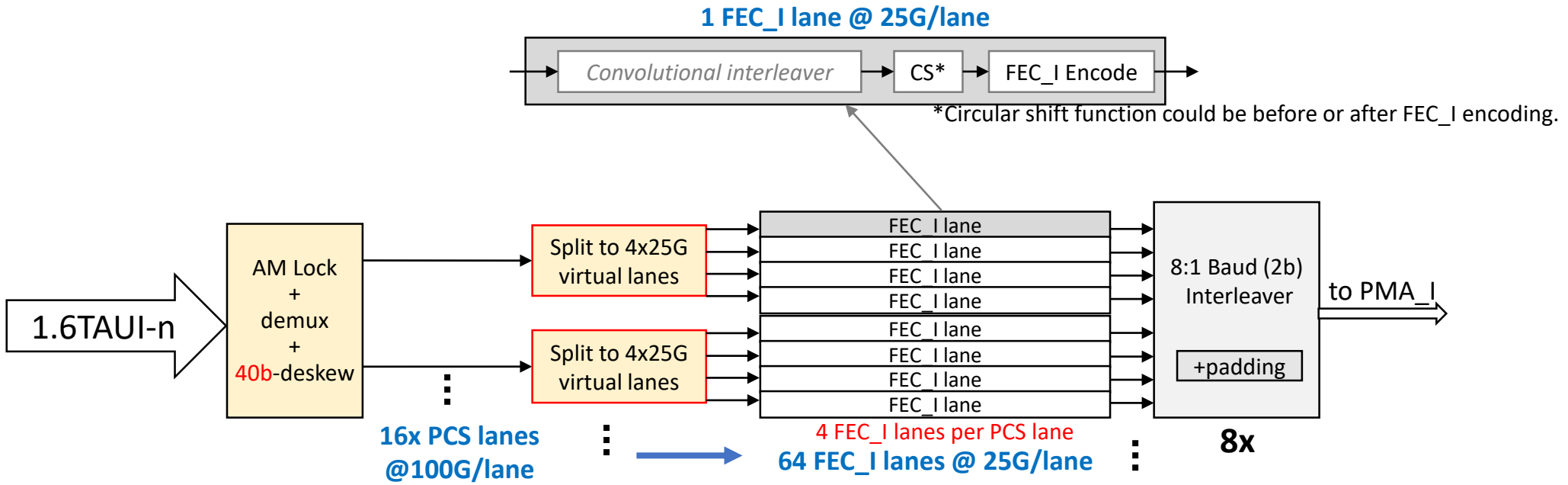
- Data from AUI is de-muxed to PCS lanes first, and deskewed to RS symbol-pair (20b) boundary.
- FEC_I sublayer is based on 100G/lane.
  - For 200/400/800 GbE, PCS lane rate is 25G/lane, and each has its own FEC_I lane.
- 8-lane per 200G PMD lane naturally supports 8:1 channel interleaver.



***Highlighted boxes are rate-specific functions.**

25G/lane Design – 1.6 TbE

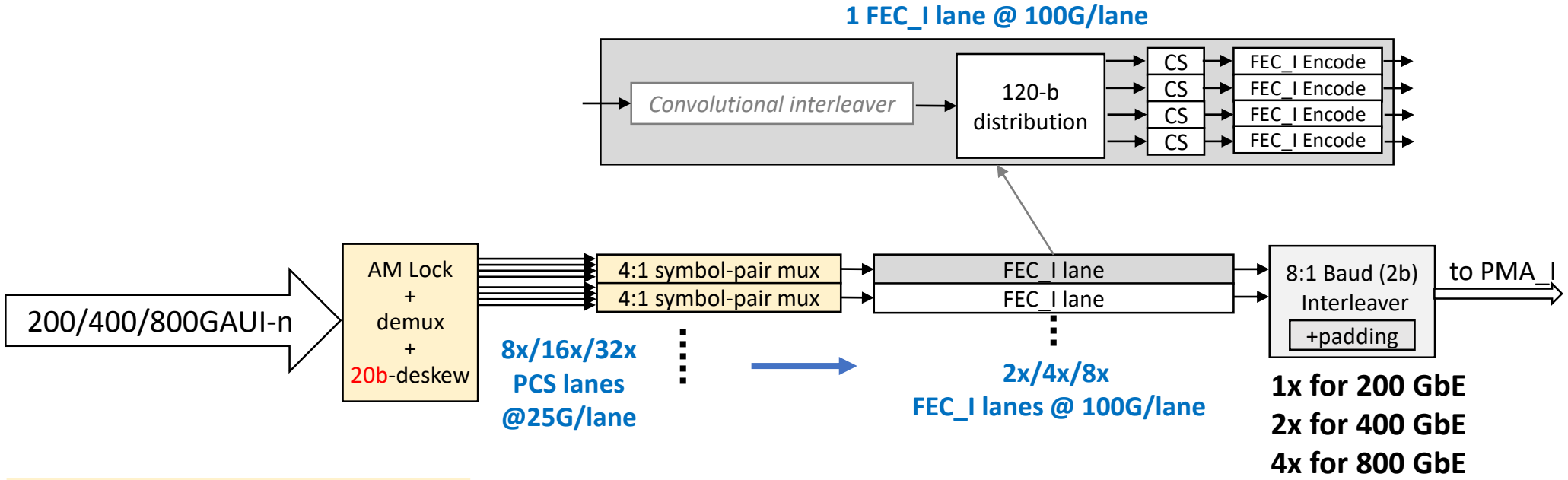
- Data from AUI is de-muxed to PCS lanes first, and deskewed to RS symbol-quartet (40b) boundary.
- FEC_I sublayer is based on 100G/lane.
  - For 1.6 TbE, each PCS lane rate is 100G, and each needs to be split into 4x25G “virtual” lanes.
  - 4x25G virtual lanes need to be recombined back to a PCS lane on Rx side.



***Highlighted boxes are rate-specific functions.**

100G/lane Design – 200 GbE, 400 GbE and 800 GbE

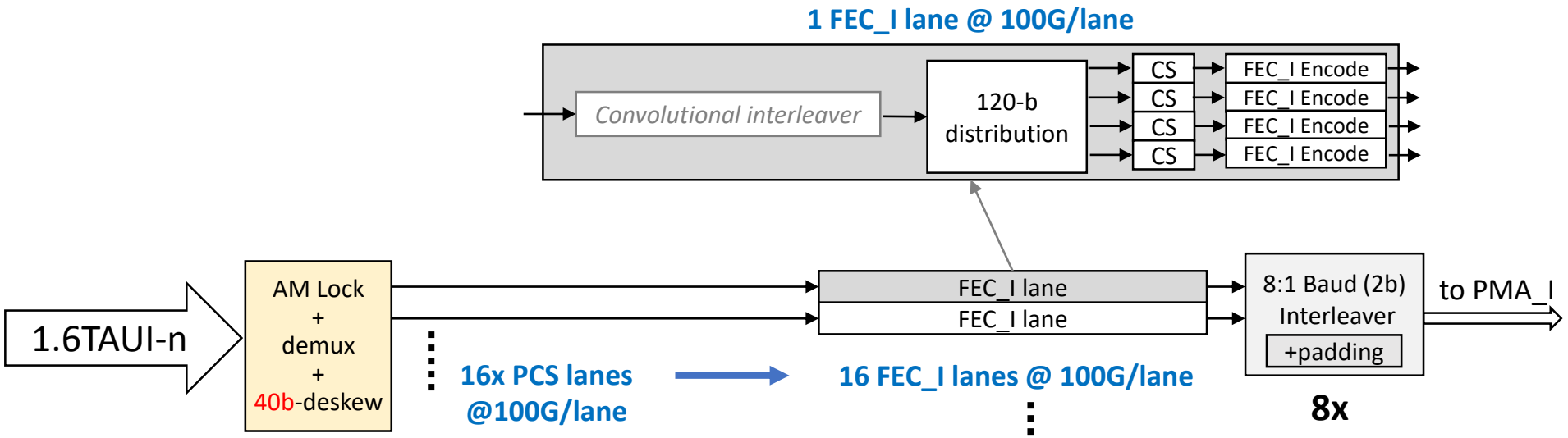
- Data from AUI is de-muxed to PCS lanes first, and deskewed to RS symbol-pair (20b) boundary.
- FEC_I sublayer is based on 100G/lane.
  - For 200/400/800 GbE, a 4:1 symbol-pair mux is needed for each FEC_I lane.
- 100G/lane design could also support 8:1 (or higher ratio) post-encoding Baud interleaver.
  - Circular shift function could be before or after FEC_I encoding.



***Highlighted boxes are rate-specific functions.**

100G/lane Design – 1.6 TbE

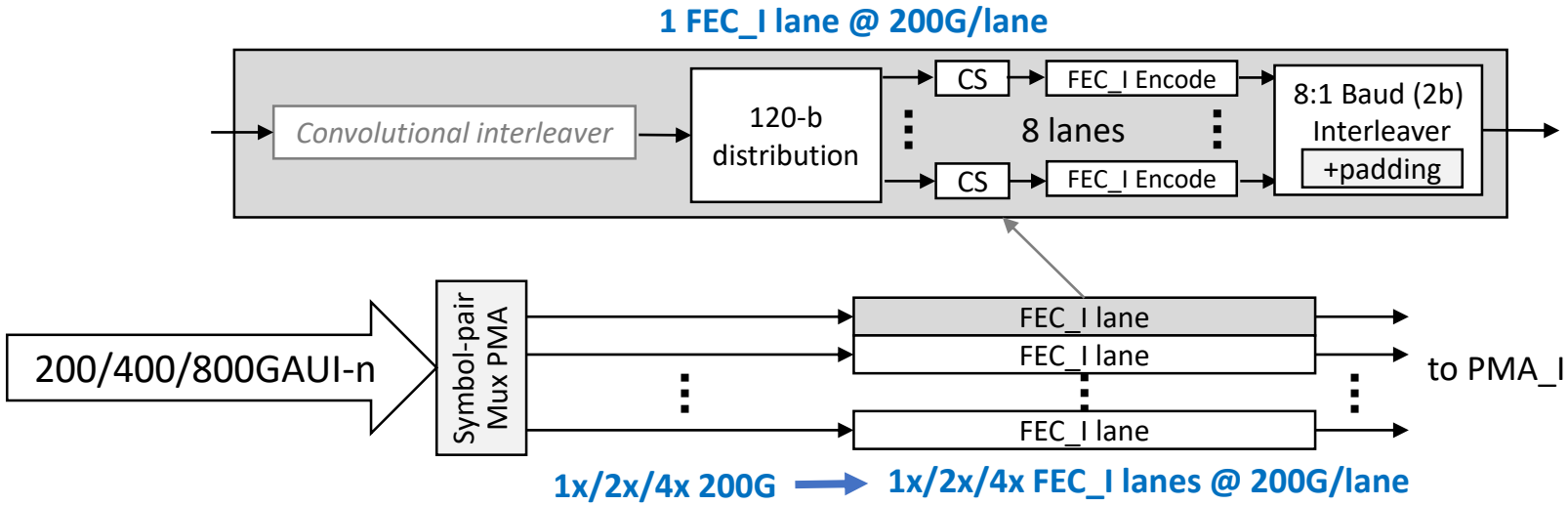
- Data from AUI is de-muxed to PCS lanes first, and deskewed to RS symbol-quartet (40b) boundary.
- FEC_I sublayer is based on 100G/lane.
  - For 1.6 TbE, each FEC_I lane takes the 100G/lane PCS input directly.
- 100G/lane design could also support 8:1 (or higher ratio) post-encoding Baud interleaver.
  - Circular shift function could be before or after FEC_I encoding.



***Highlighted boxes are rate-specific functions.**

200G/lane Design – 200 GbE, 400 GbE and 800 GbE

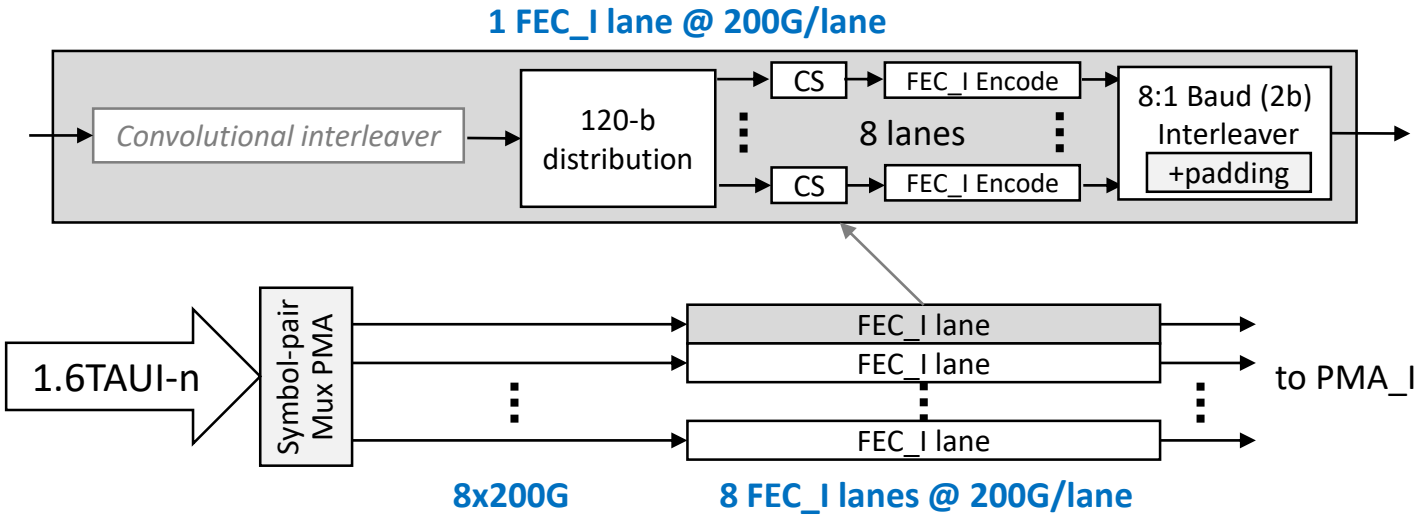
- Data from AUI is NOT required to be de-muxed to PCS lanes first.
  - Relying on the symbol-pair muxing PMA functions to establish FEC_I lane mapping.
- Maximizing the common functional blocks across different rates.
- 200G/lane design could also support 8:1 (or higher ratio) post-encoding Baud interleaver.
  - Circular shift function could be before or after FEC_I encoding.



***No rate-specific functions.**

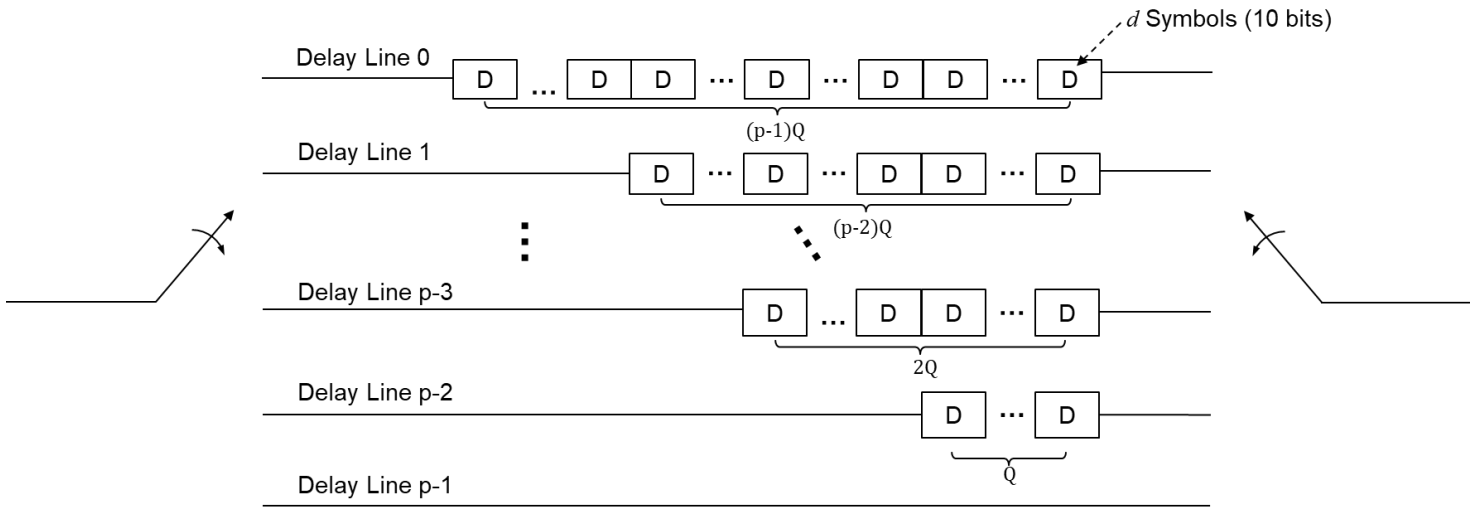
200G/lane Design – 1.6 TbE

- Data from AUI is NOT required to be de-muxed to PCS lanes first.
  - Relying on the symbol-pair muxing PMA functions to establish FEC_I lane mapping.
- Maximizing the common functional blocks across different rates.
- 200G/lane design could also support 8:1 (or higher ratio) post-encoding Baud interleaver.
  - Circular shift function could be before or after FEC_I encoding.



***No rate-specific functions.**

200G/lane Convolutional Interleaver Design



PCS	d (RS symbol)	P	Q	Depth
1.6TE	4	3	24	12x RS
800GE	4	3	46	12x RS
400GE	4	3	46	6x RS
	2	6	46	12x RS
200GE	4	3	92	6x RS
	2	6	92	12x RS

Summary

- The FEC_I lane rate does not affect the FEC performance.
  - However it needs to be defined clearly to ensure interop.
- FEC_I sublayer designing based on 200G/lane PMA lanes enables unified design across all rates that supports 200G/lane optical PMDs.
  - With a single FEC_I sublayer defined, it could be used to define all Ethernet rates using 200G/lane optics.

Thank you!