25G & 100G PCSL processing for Concatenated FEC

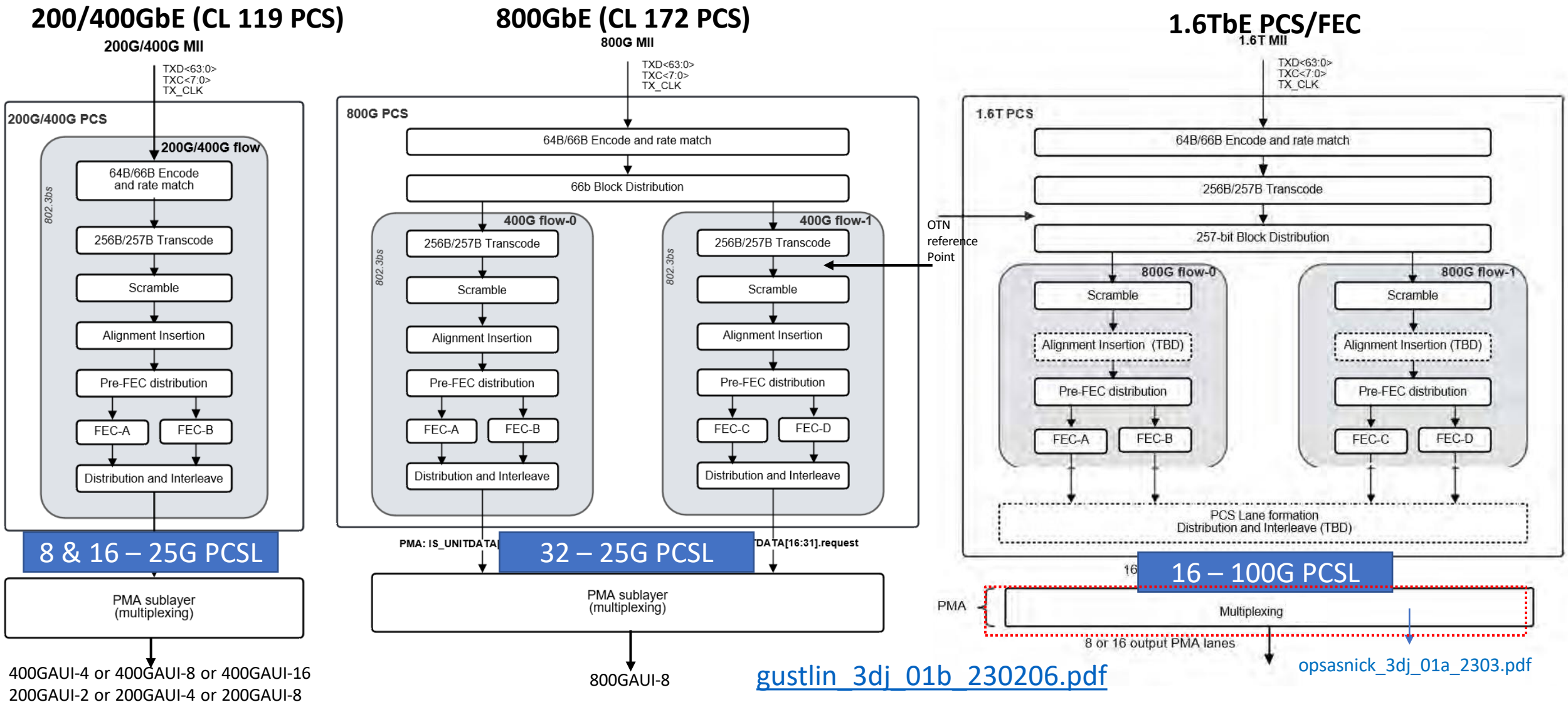
Co-Authors:

Lenin Patra, Marvell
Arash Farhood, Marvell
Vasu Parthasarathy, Broadcom
Sridhar Ramesh, Maxlinear
Henry Wong, Alphawave

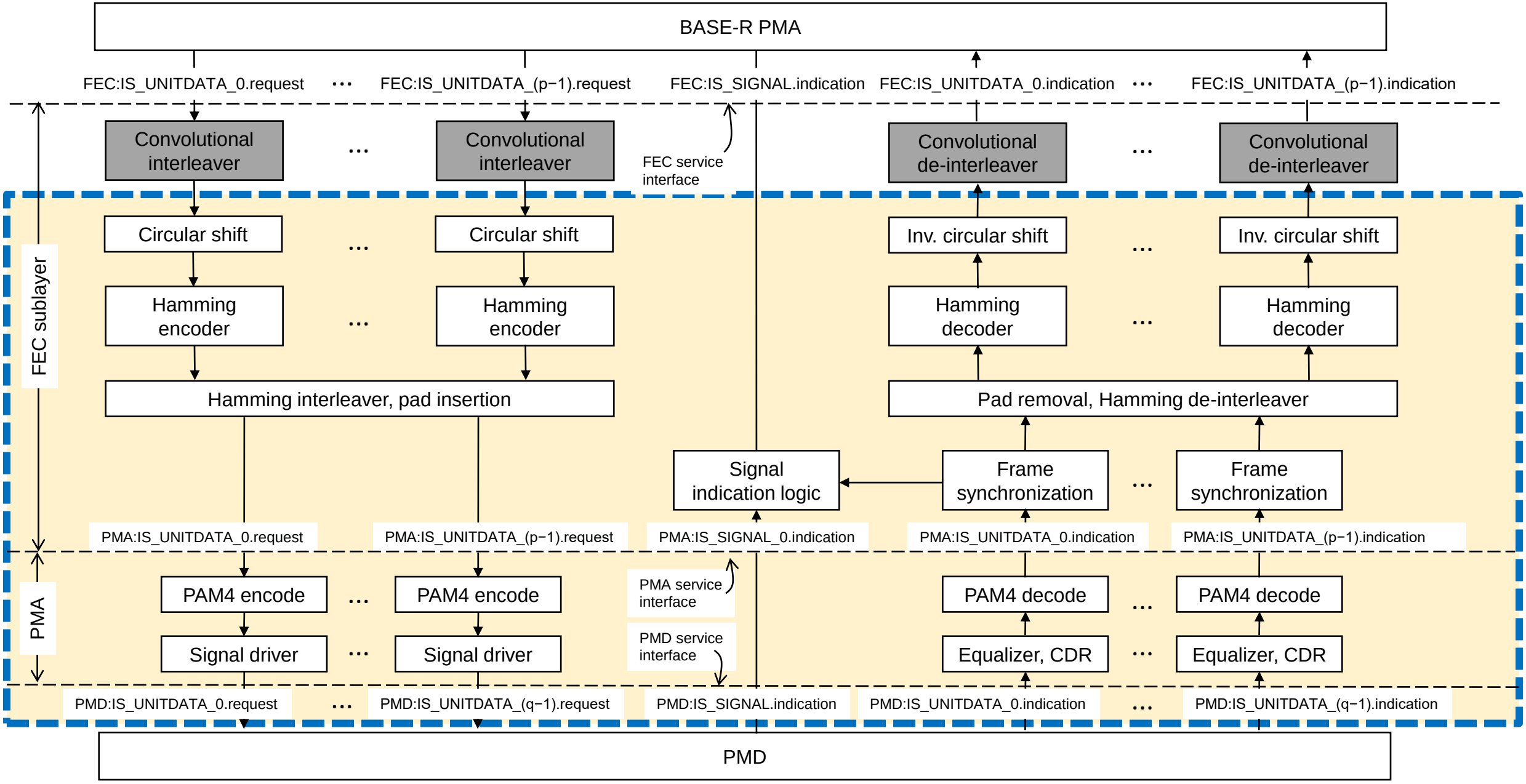
Goal of this Presentation

- This presentation describes a proposal for 25G and 100G PCSL processing of TX and RX data path with Inner code (128,120)

Recap Of Type of PCSL already adopted for 200G/400G/800G/1.6T in IEEE

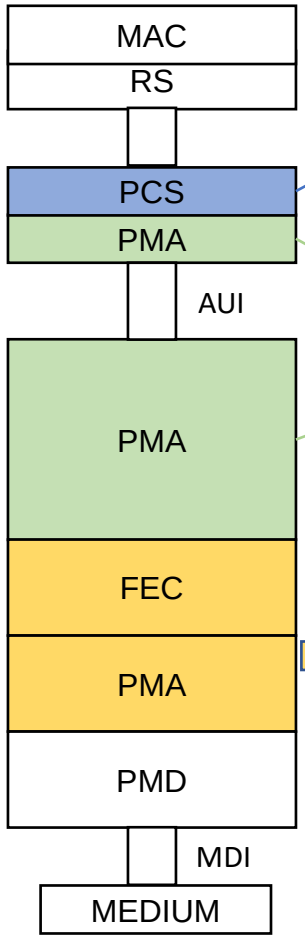


Recap of Adopted FEC sublayer highlighted in dotted Lines for 200G/400G/800G



patra_3dj_01b_2303.pdf parthasarathy_3dj_02a_2303.pdf

Status of Inner FEC Architecture & Work in Progress:



Type 2 scheme

200G, 400G, 800G, 1.6T PCS is adopted as per CL-119, CL-172 PCS

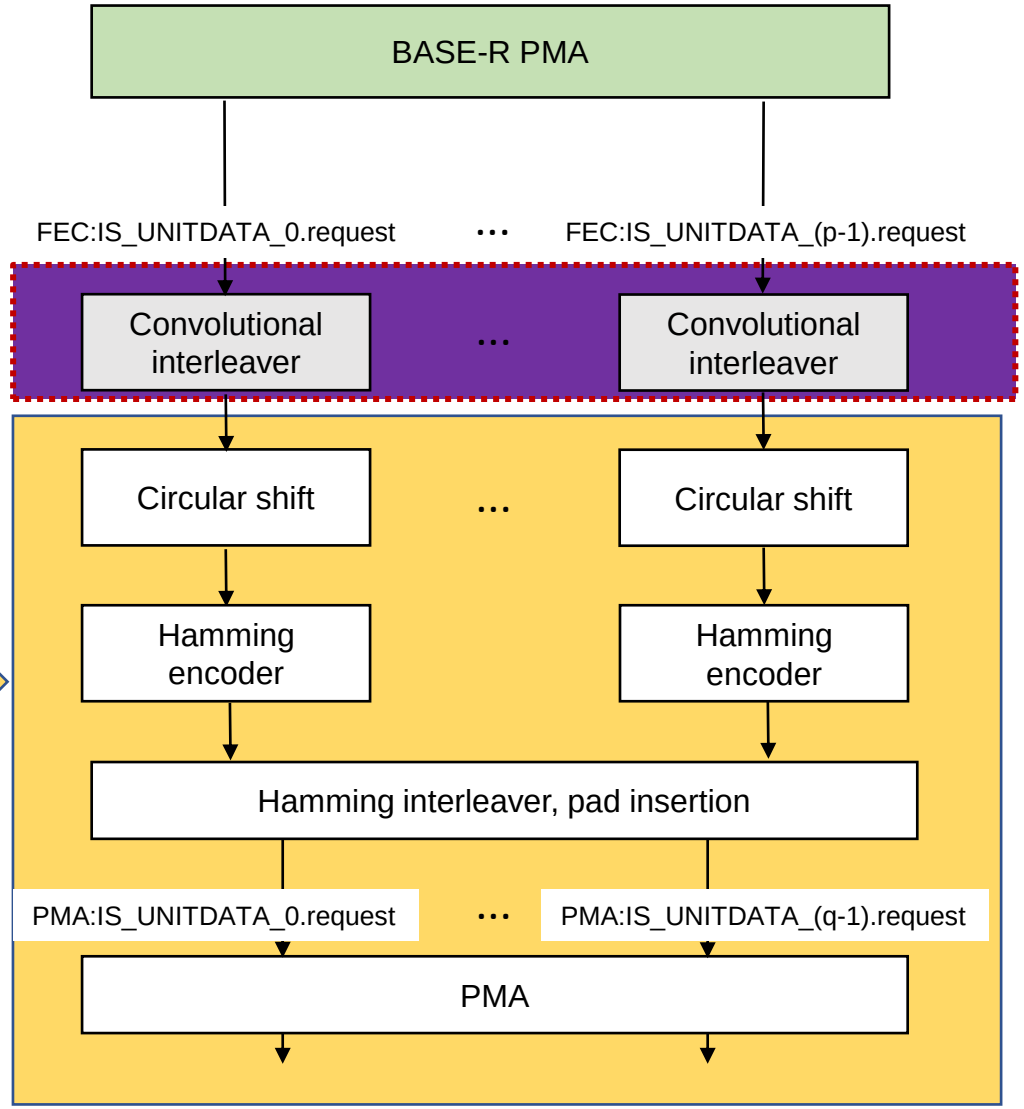
- Up to 800G – This is **25G PCSL** based
- For 1.6T - This is **100G PCSL** based

200G Symbol Muxing PMA Lane is adopted: ran_3dj_01a_2303.pdf

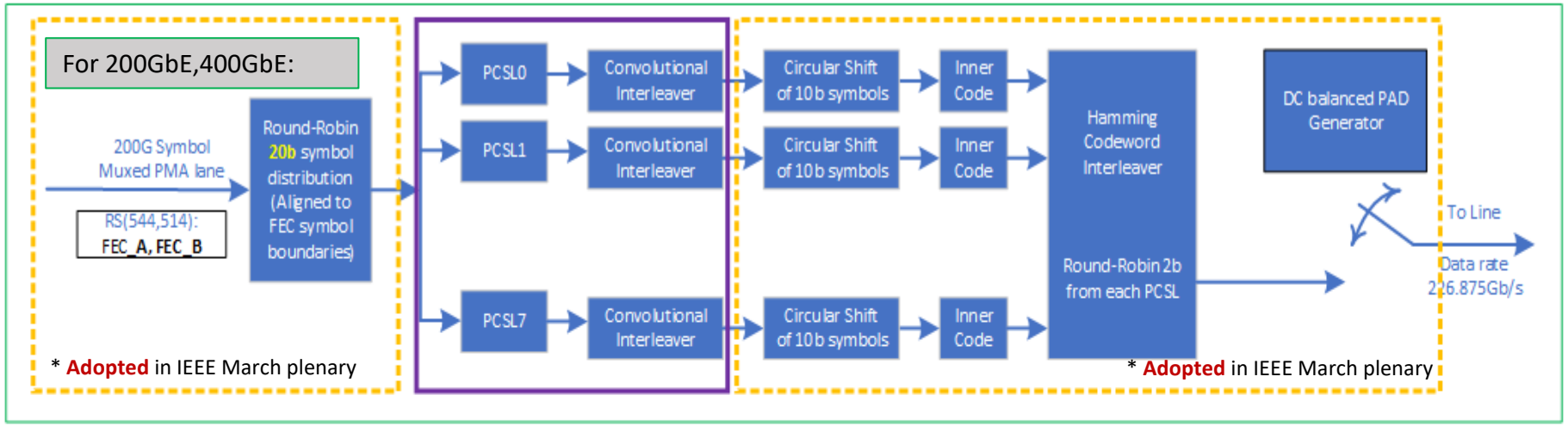
* Most of the Inner Code FEC sublayer is adopted except few blocks

Work in Progress:

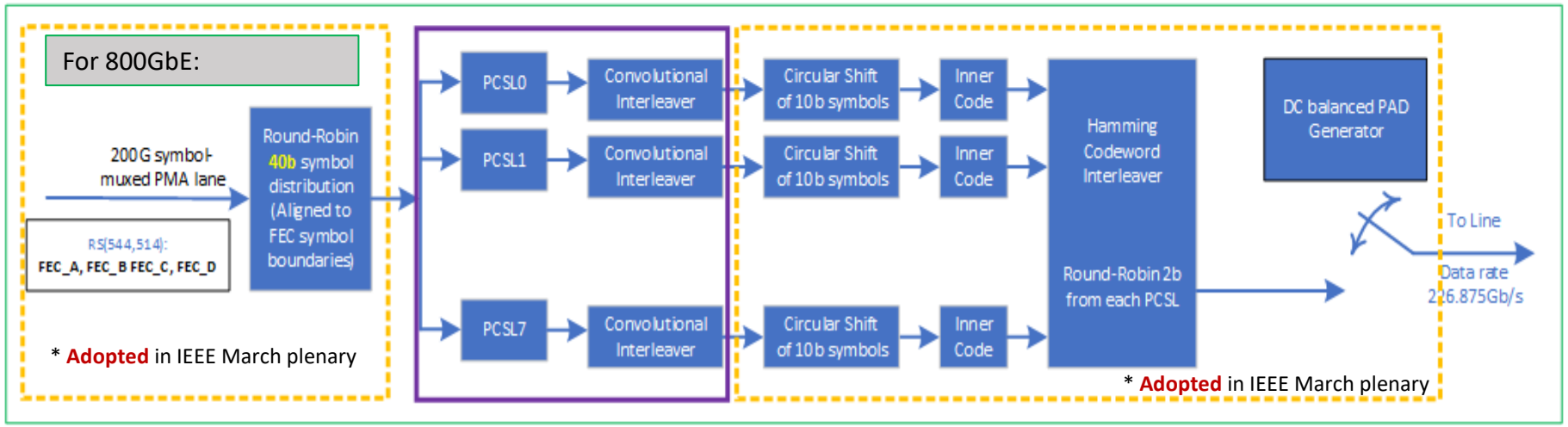
- **Rate of Convolutional Interleaver for 200G/400G/800GbE**
- **Inner FEC sublayer for 1.6TbE**



Representation of 25G PCSL processing of TX path with Inner code (128,120) based on 200G PMD

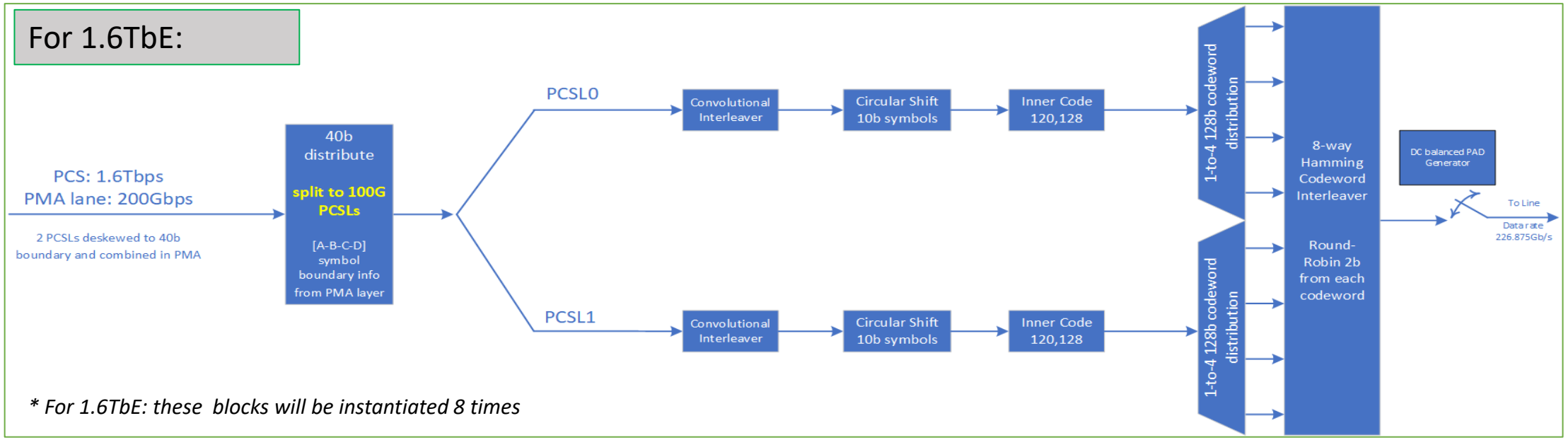


- 200G/400G – Building the **CI** (Convolutional Interleaver) based on 25G PCSL fits perfectly to the PCSL already defined for 200G/400GbE in IEEE
- 25G PCSL based CI also fits well to the already adopted 8-way Hamming inter-leaver for better System Performance with Inner code



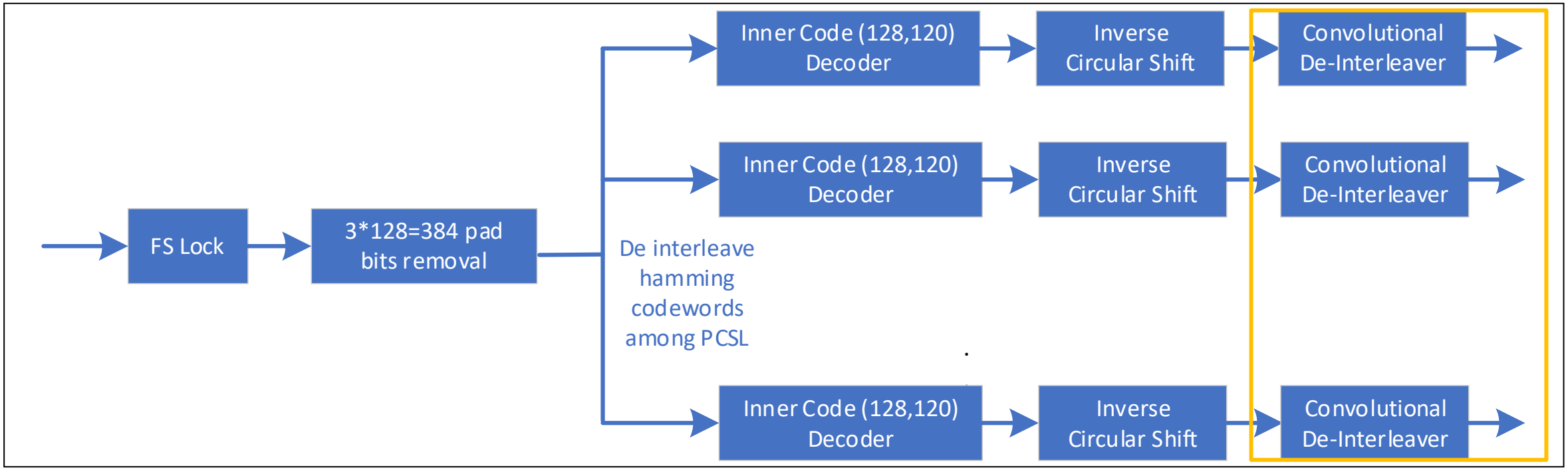
- 800G – Building the **CI** (Convolutional Interleaver) based on 25G PCSL also chimes well with 32 PCSL already defined for 800GbE
- Just like 200G/400G - 25G PCSL based CI also fits well to the already adopted 8-way Hamming inter-leaver for better System Performance with Inner code for 800GbE

Representation of 100G PCSL processing TX path with Inner code (128,120) based on 200G PMD



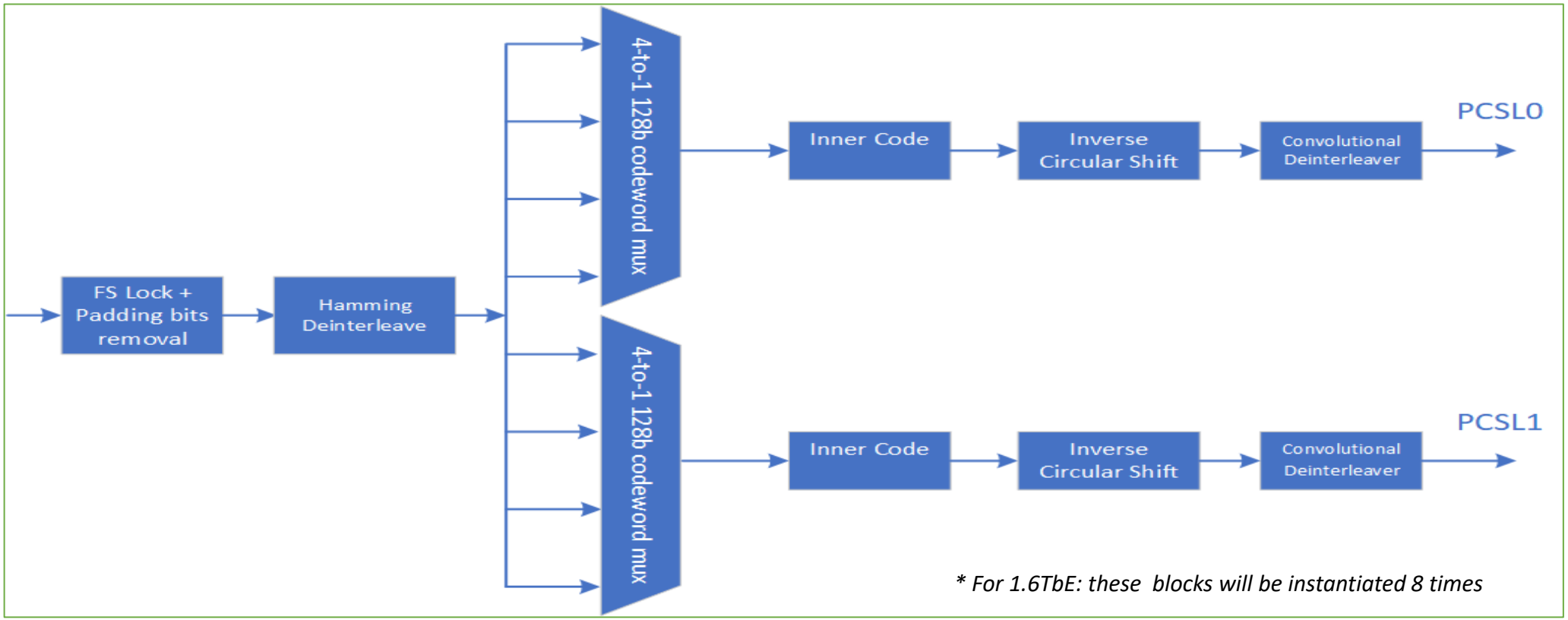
- 1.6Tbps PCS is based on 16 X 100G PCSL. So, a 200G PMA lane for such a scheme will consists of 2 X 100G PCS Lane
- As adopted in IEEE - 200Gbps PMA Lane is already formed by de-skewing 2x 100G PCS lanes to 40b boundary & followed by multiplexing any 2 PCS lanes (among 16) into FEC A/B/C/D boundary aligned to 40 boundary.
- 100G PCSL based 200G PMA can simply leverage the properties of 8-way Hamming Inter-leaver - which is already adopted for 200G/400G/800G
- Following blocks are needed to process it with 8 -way Hamming Interleaver
  a. Convert 200G PMA lane to 100G PCS lanes by distributing 40b blocks among 2 streams. The correct boundary of 40b blocks is already available from the PMA layer.
  b. Convolutional Interleaver and Inner code block and circular shift blocks operates at 100G PCSL rate.
  c. Inner code block output (128 bits) is passed through 1:4 codeword distribution DeMUX as an input to 8way Hamming inter-leaver
  d. Hamming interleaver and Padding processing is identical to 200G/400G/800GbE – as shown in the previous slide # 6

Detailed representation of 25G PCSL Processing of RX path with Inner code (128,120)



- FS Lock, Padding Removal Scheme, Hamming de-interleaver, Inverse circular shift has been adopted in IEEE March plenary
- Convolutional De-interleaver scheme is going to follow Convolutional Interleaver scheme as shown in 25G PCSL TX path.

Detailed representation of 100G PCSL Processing of RX path with Inner code (128,120)



- FS Lock, Padding Removal, Hamming de-interleaver processing is identical to as 200G/400G/800G processing scheme
- 4:1 Mux 128bit codeword distribution is analogous to the 1:4 DeMux for 128-bit codeword distribution in the TX path.
- Convolutional De-interleaver is going to follow the Convolutional Interleaver scheme in TX path – as shown in TX path slide to form 100G PCSL for 1.6T

Summary

- We presented a 25G & 100G PCSL processing proposal, which fits well to already adopted 200G/400G/800G/1.6T MAC configurations

- The Presented proposal also works well with adopted Inner code FEC Sub-layers and 200G Symbol Muxing PMA sublayers.

Thanks !