IEEE Std 802.3 Clause 90 Ethernet support for time synchronization protocols

David Law, Hewlett Packard Enterprise <dlaw@hpe.com>

Steve Gorshe , Microchip <steve.gorshe@microchip.com>

Marek Hajduczenia, Charter Communication <marek.hajduczenia@charter.com>

Richard Tse, Microchip <richard.tse@microchip.com>

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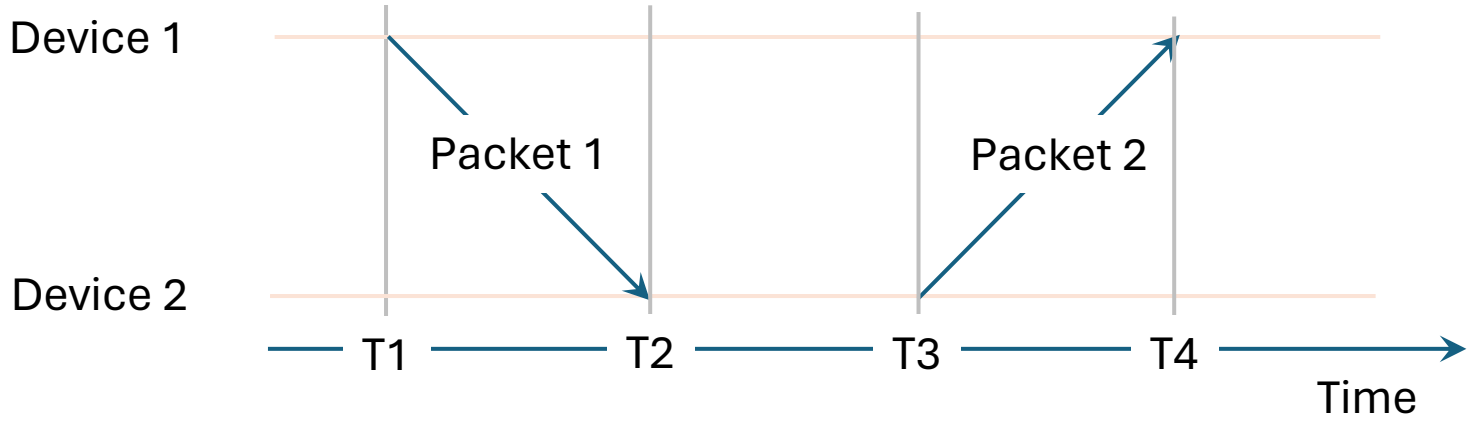
Problem statement

Time synchronization protocols needs to know media delay between devices



Delay in each direction assumed symmetrical and to have small and slowly time varying component

- Media delay between device 1 and device 2 = (T4 – T1 – (T3 – T2))/2
- Any asymmetry or variation in the packet propagation delay will impact accuracy

IEEE 802.3 needed to provide a PHY agnostic approach

- Capable of supporting existing and future 802.3 PHYs

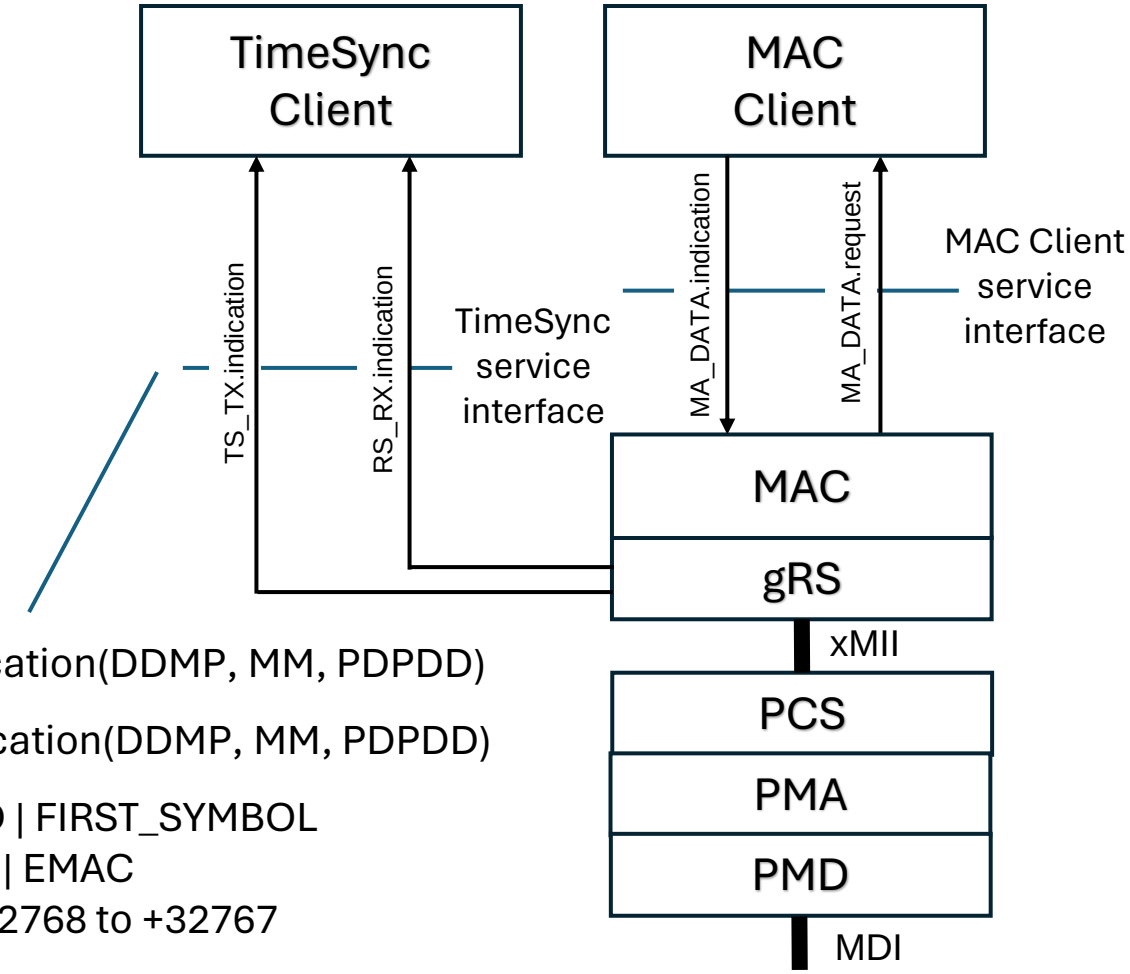
IEEE 802.3 needed to provide protocol agnostic approach for time synchronization

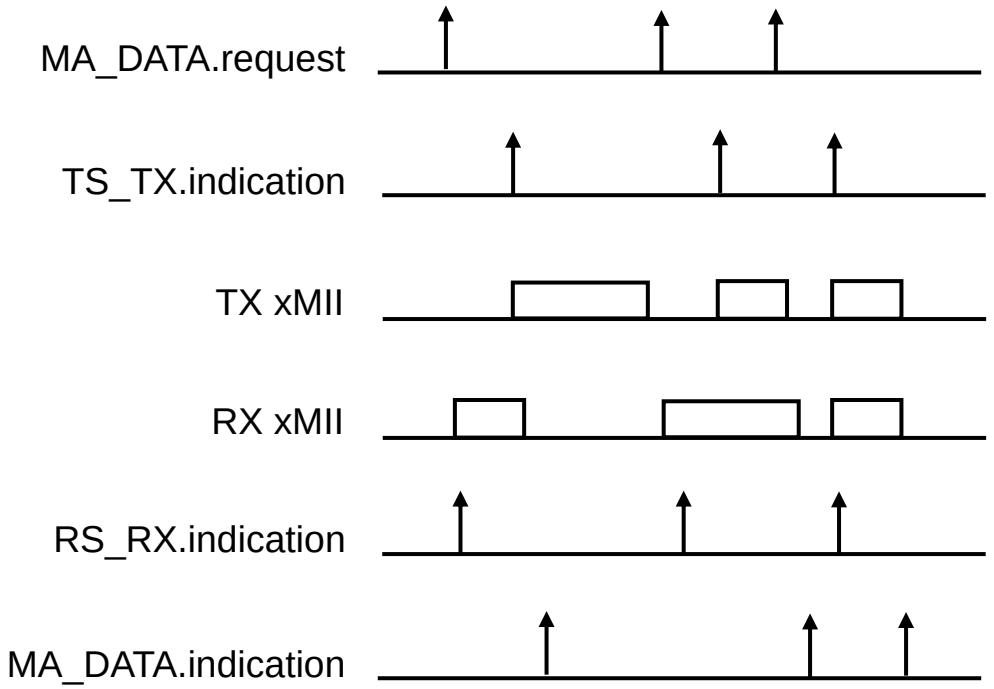
- IEEE Std 1588 is an example of a time synchronization protocol (see subclause 90.2)

Assumption and approach

- Assumption
  - Delay in each direction assumed symmetrical and to have small and slowly time varying component
    - System level timestamping accuracy is affected by multiple components/functions/subsystems where the IEEE 802.3 PHY is one
- Approach
  - IEEE 802.3 needed to provide protocol agnostic approach for time synchronization
    - IEEE 802.3 provides **support** for time synchronization protocols
    - Captures ingress/egress time of **every** packet
    - TimeSync Client with protocol knowledge **selects** ingress/egress times of packet of interest
    - The path data delay information is used to **adjust** this time to obtain MDI ingress/egress times
  - IEEE 802.3 needed to provide a PHY agnostic approach
    - Captures ingress/egress time at media (i.e., MAU/PHY) independent interface (e.g., AUI/xMII)
  - Path data delay in each direction through PHY unlikely to be symmetric
    - Specify a set of path data delay registers to calculate MDI ingress/egress time (see subclause 90.7)
    - Difference between min and max path data delay register provides MDI ingress/egress time accuracy
  - Path data delay through a PHY could vary over time, due to standardized functions or implementation choices
    - Use constant values for Tx and Rx functions (see 90.7.1) that have a constant accumulated path data delay
    - Provide dynamic path data delay (see subclause 90.5.3 and 90.5.4) for Tx and Rx functions that do not add to a constant accumulated path data delay
    - Provide implementation advice (see Annex 90A)

Measure ingress/egress at xMII





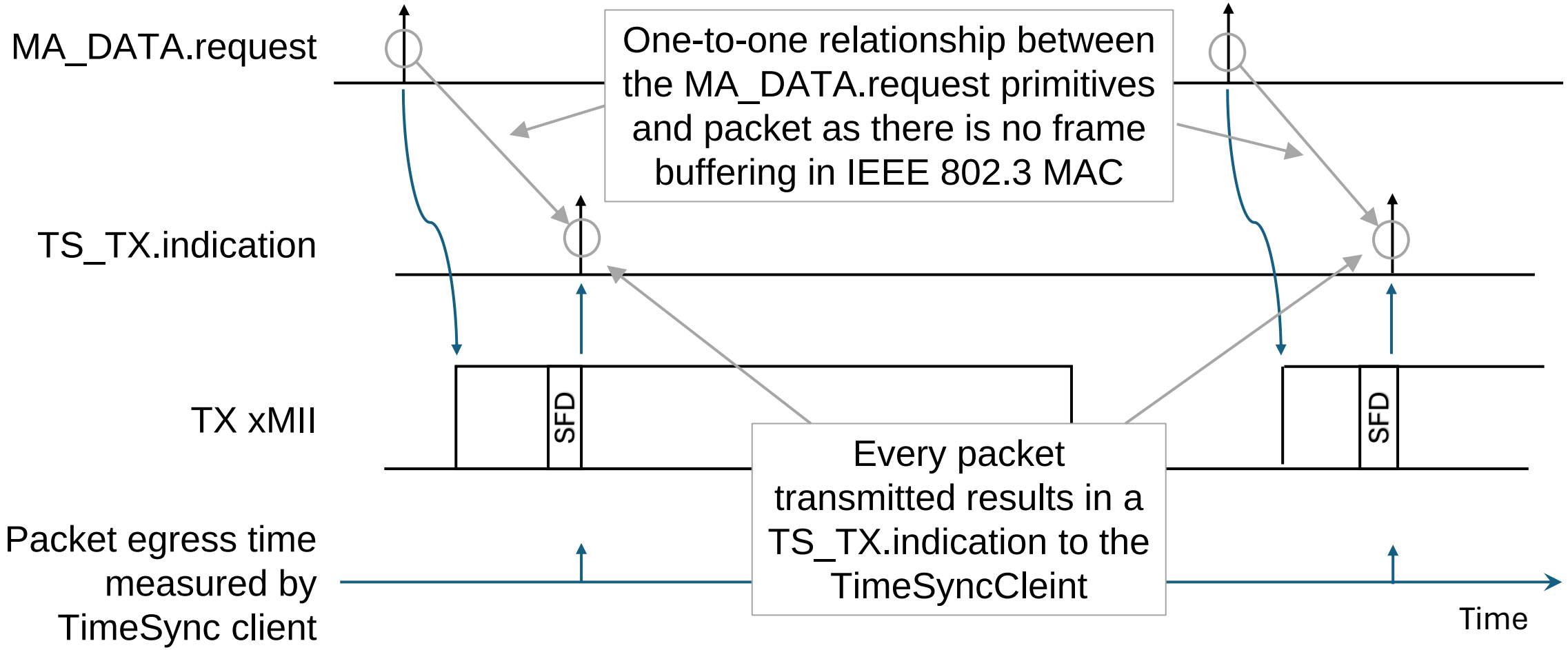
TS_TX.indication(DDMP, MM, PDPDD)

TS_RX.indication(DDMP, MM, PDPDD)

DDMP: SFD | FIRST_SYMBOL
MM: PMAC | EMAC
PDPDD : -32768 to +32767

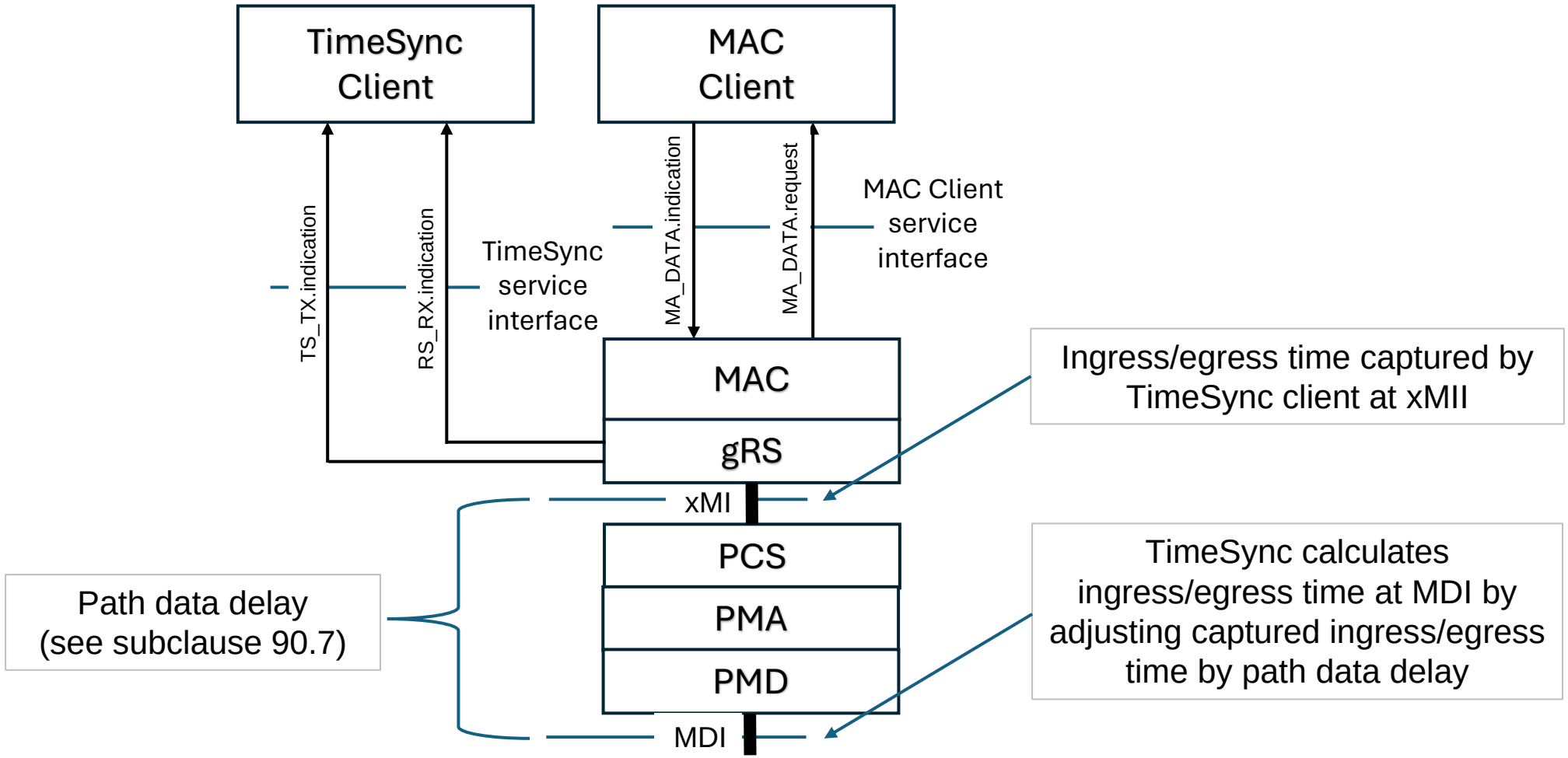
See subclause 90.4.3.1.1 and 90.4.3.2.1

Egress time example

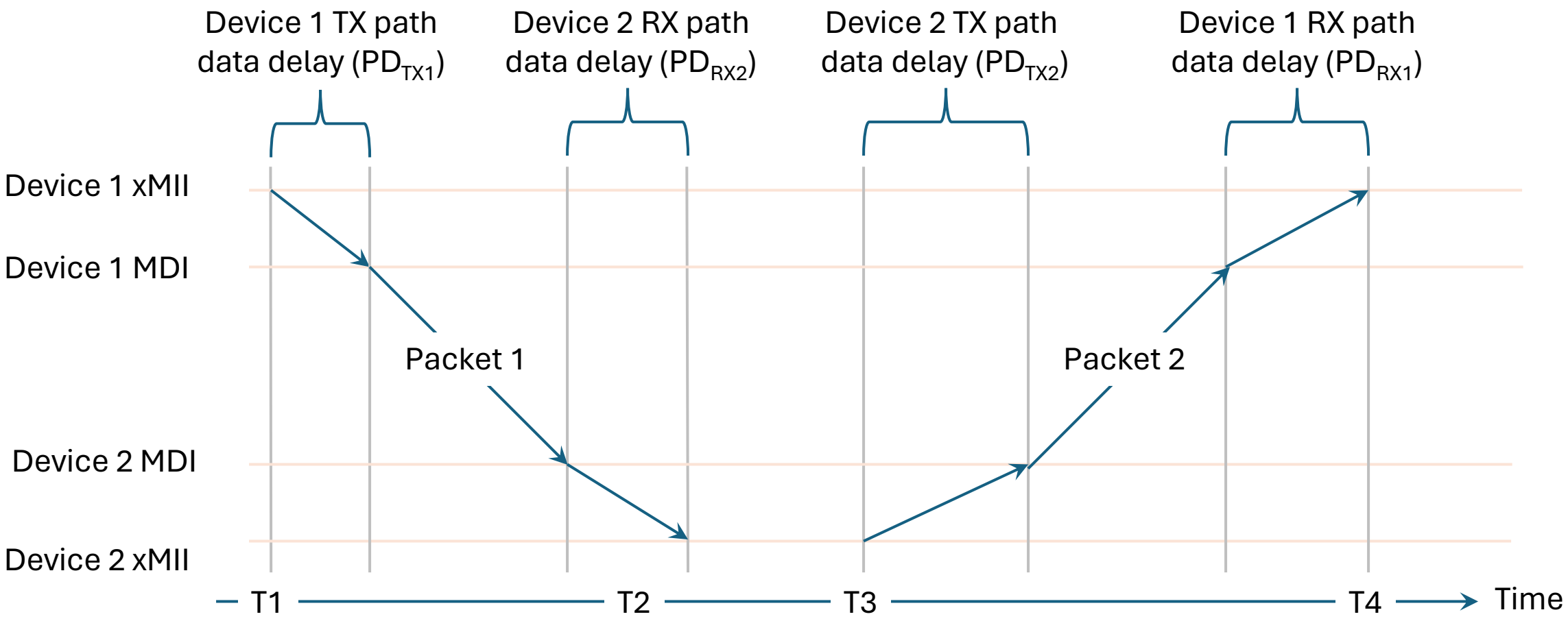


In this example the DDMP parameter would be FIRST_SYMBOL (beginning of the first symbol after an SFD)

Use path data delay to calculate ingress/egress at MDI



Use path data delay to calculate ingress/egress at MDI

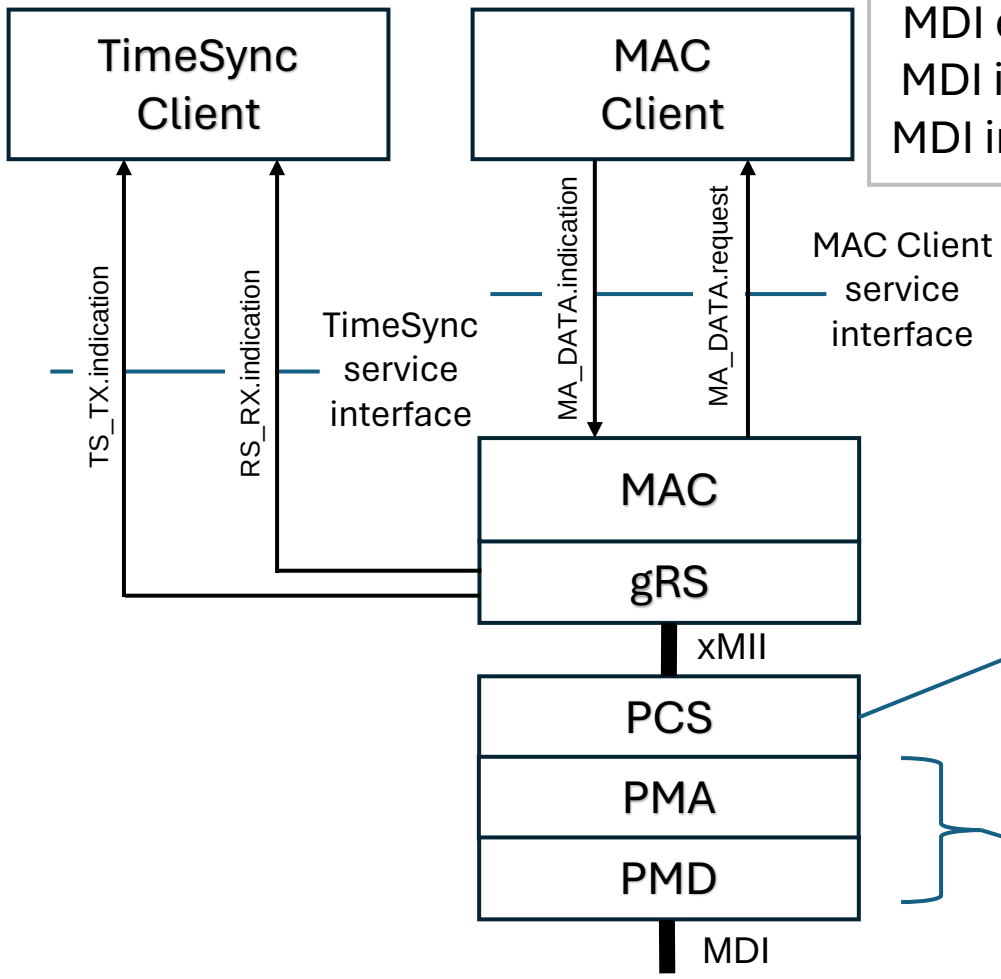


If forward and return delays over the media are symmetric:

One-way delay over media = $((T4 - PD_{RX1}) - (T1 + PD_{TX1}) – ((T3 + PD_{TX2}) - (T2 - PD_{RX2}))/2$

Use path data delay to calculate ingress/egress at MDI

MDI egress time min = xMII egress time + sum(TX path data delay min)
MDI egress time max = xMII egress time + sum(TX path data delay max)
MDI ingress time min = xMII ingress time - sum(RX path data delay min)
MDI ingress time max = xMII ingress time - sum(RX path data delay max)



Where a sublayer, or grouping of sublayers, is an individually manageable entity, it is known as an **MDIO Manageable Device (MMD)**.(See subclause 45.1.2)

PCS TimeSync registers (MMD 3)

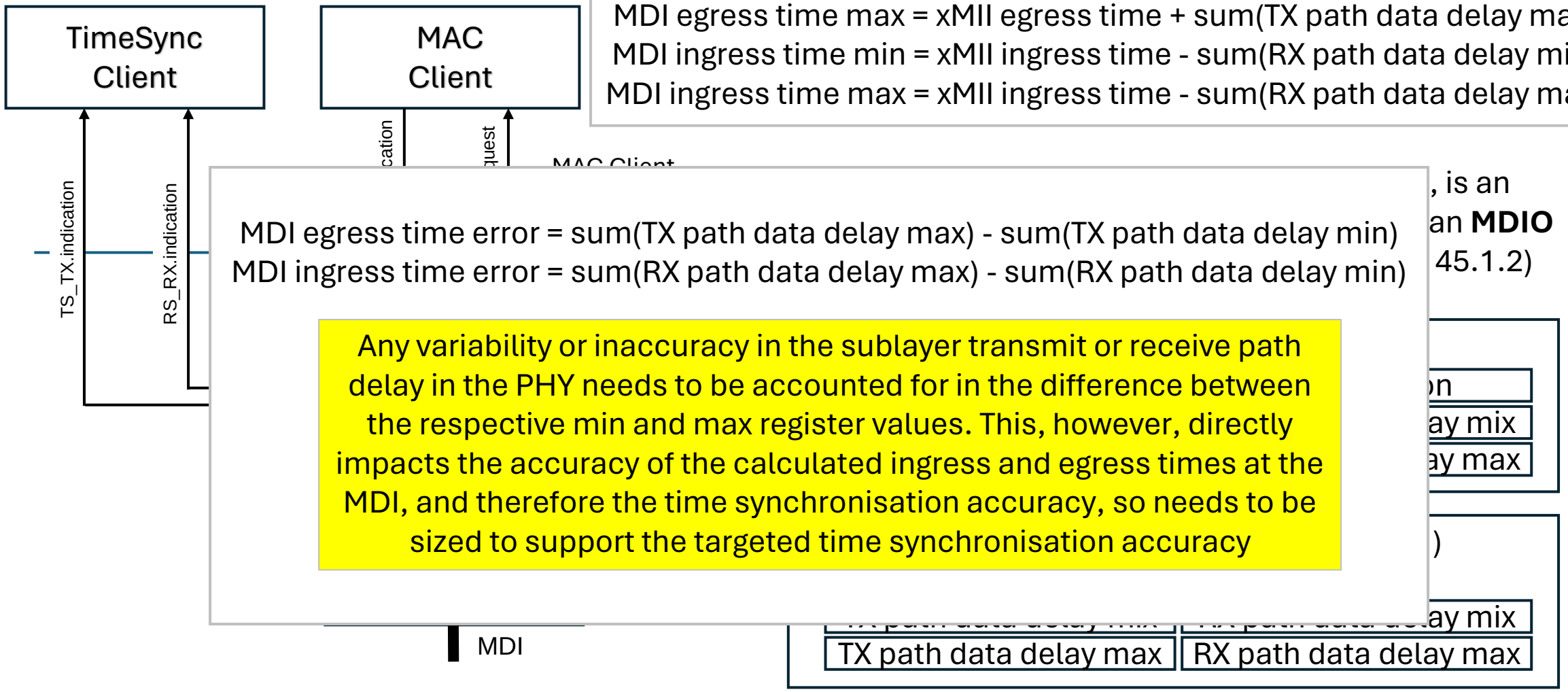
Capability	Configuration
TX path data delay mix	RX path data delay mix
TX path data delay max	RX path data delay max

PMA/PMD TimeSync registers (MMD 1)

Capability	
TX path data delay mix	RX path data delay mix
TX path data delay max	RX path data delay max

Use path data delay to calculate ingress/egress at MDI

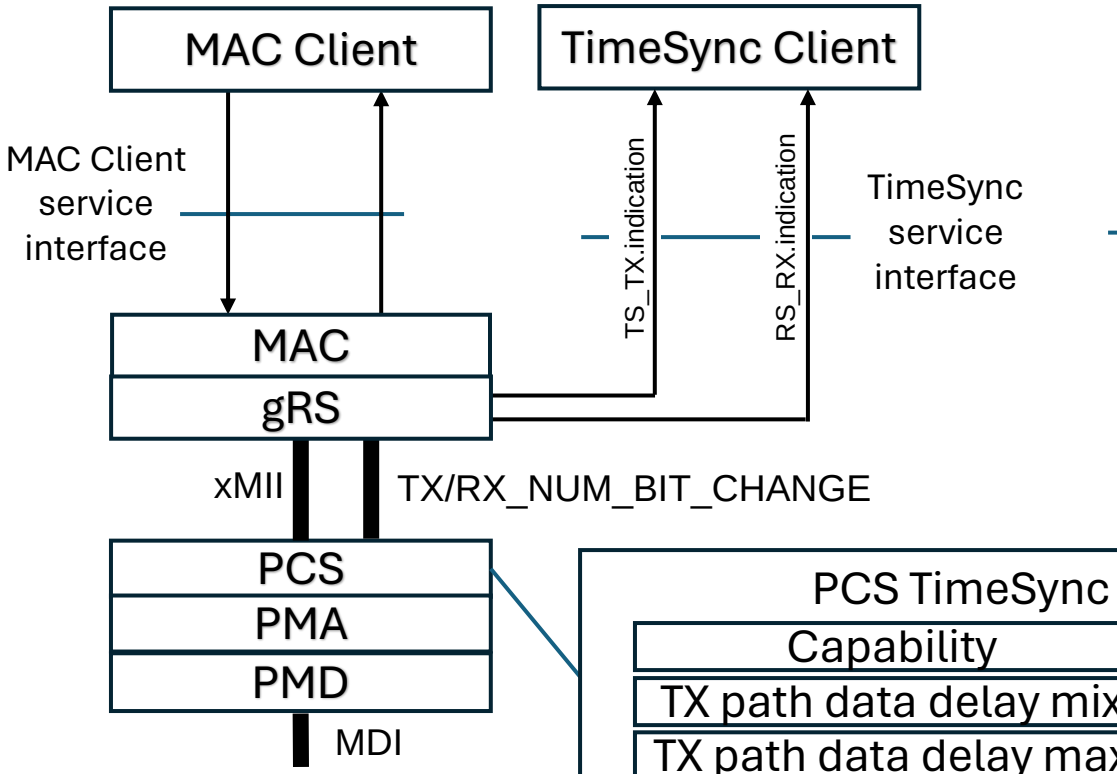
MDI egress time min = xMII egress time + sum(TX path data delay min)
MDI egress time max = xMII egress time + sum(TX path data delay max)
MDI ingress time min = xMII ingress time - sum(RX path data delay min)
MDI ingress time max = xMII ingress time - sum(RX path data delay max)



MDI egress time error = sum(TX path data delay max) - sum(TX path data delay min)
MDI ingress time error = sum(RX path data delay max) - sum(RX path data delay min)

Any variability or inaccuracy in the sublayer transmit or receive path delay in the PHY needs to be accounted for in the difference between the respective min and max register values. This, however, directly impacts the accuracy of the calculated ingress and egress times at the MDI, and therefore the time synchronisation accuracy, so needs to be sized to support the targeted time synchronisation accuracy

Dynamic path data delay (aka NUM_BIT_CHANGE)



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DDMP: SFD | FIRST_SYMBOL
MM: PMAC | EMAC
PDPDD : -32768 to +32767

PCS TimeSync registers

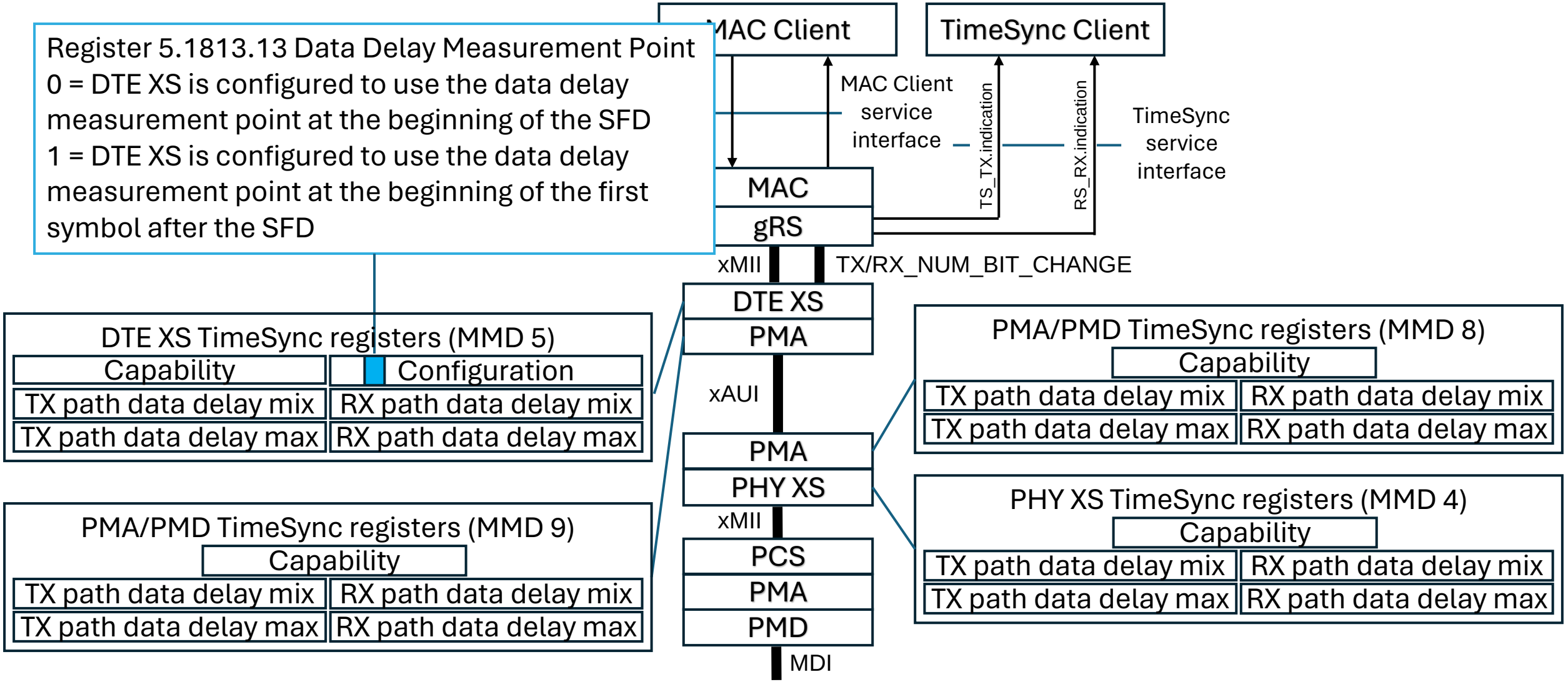
Capability	
TX path data delay mix	RX pa
TX path data delay max	RX pa

Register 3.1813.13 Data Delay Measurement Point
0 = Configures the PCS to use the data delay measurement point at the beginning of the SFD
1 = Configures the PCS to use the data delay measurement point at the beginning of the first symbol after the SFD

MDI egress time min = xMII egress time + PCS dynamic transmit path data delay + sum(TX path data delay min)
MDI egress time max = xMII egress time + PCS dynamic transmit path data delay + sum(TX path data delay max)
MDI ingress time min = xMII ingress time + PCS dynamic receive path data delay - sum(RX path data delay min)
MDI ingress time max = xMII ingress time + PCS dynamic receive path data delay - sum(RX path data delay max)

MII Extender

Register 5.1813.13 Data Delay Measurement Point
0 = DTE XS is configured to use the data delay measurement point at the beginning of the SFD
1 = DTE XS is configured to use the data delay measurement point at the beginning of the first symbol after the SFD



Suggested PHY and MII extender specification guidance

To provide IEEE 802.3 Clause 90 ‘Ethernet support for time synchronization protocols’, IEEE 802.3 PHYs and IEEE 802.3 MII extenders should not be specified in such a way that would prevent (a) a known path data delay (see IEEE 802.3 subclause 90.7) between the RS MII and the MDI, and vice versa, with variability **within the limits necessary to support the targeted time synchronization accuracy**, except that (b) dynamic variability within the PCS of the PHY, or the DTE XS if a MII extender is present, can optionally be accounted for using the PCS dynamic path data delay (PDPDD) information (aka NUM_BIT_CHANGE) provide across the TimeSync service interface (see IEEE 802.3 subclause 90.5.3 and 90.5.4).

Summary

Clause 90 is PHY and time synchronization protocol agnostic

Ingress/egress of all packets across xMII signalled to TimeSync Client

- Enables TimeSync Client to capture ingress/egress time of a packet at xMII

TimeSync Client uses time synchronization protocol knowledge (beyond the scope of the IEEE 802.3 standard) to capture ingress/egress time, at the xMII, of packets of interest passed across the MAC Client service interface

The TimeSync Client then uses the available path data delay information to calculate ingress/egress time of packets of interest at the MDI

- Any inaccuracy in path data delay information, for example to account for delay variability in the PHY transmit of receive path, impacts the accuracy of the calculated ingress/egress time at the MDI and therefore the supported time synchronization accuracy

How ingress/egress time is used for any particular time synchronization protocol is beyond the scope of the IEEE 802.3 standard