PMA with RS-FEC symbol multiplexing test vectors

Arnon Loewenthal– Alphawave Semi

Omri Levy – Alphawave Semi

Zvi Rechtman – NVIDIA

Amir Rubin - NVIDIA

Supporters

This presentation

- Provides PMA sublayer (CL176) interoperability test vectors

Background

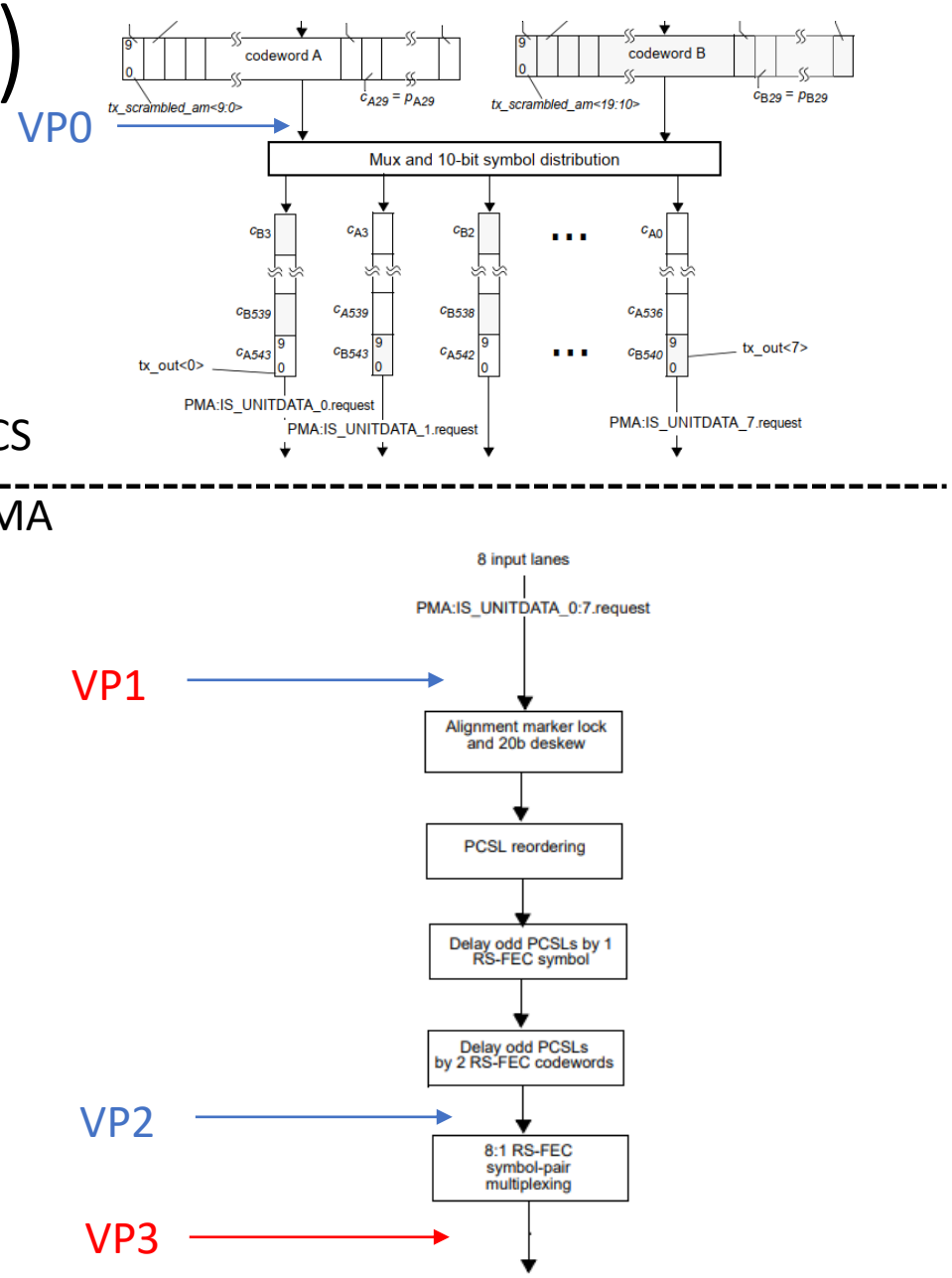
- Clause 176 PMA with RS-FEC symbol muxing was adopted for 200GBASE-R, 400GBASE-R, 800GBASE-R and 1.6TBASE-R using 200G/lane AUIs or PMDs
- RS-FEC symbol muxing (ran_3dj_01a_2303.pdf) was adopted (March 2023 Plenary, Motion #4).
- 4x RS-FEC codewords interleaving for 200GE and 400GE using 200G/lane AUIs or PMDs (he_3dj_02a_2307) was adopted (July 2023 Interim, Motion #10).

Test vectors - general

- The PMA test vectors can be used during development to check for interoperability.
- Test vectors input
  - Valid PCS data with AM which enables checking for interoperability with PCS.
  - The PCS data is with zero skew between PCS lanes, which can result from a direct connection to a PCS. This is an assumption for vectors generation, in practice other cases are also possible.
- Test vectors address following sections of CL176 (based on draft 1.0):
  - 200GBASE-R 8:1 (CL 176.5.1)
  - 400GBASE-R 16:2 (CL 176.6.1)
  - 800GBASE-R 32:4 (CL 176.7.1)
  - 1.6TBASE-R 16:8 (CL 176.8.1)
- Acronym VP (Vector Point) is used for reference points for which vectors are available.

Vector points (200GE/400GE)

- Test vectors are given for test points on the right.
  - VP1 and VP3 are required for interoperability.
  - VP0 and VP2 are given as a reference for debug.
- VP0 is identical to Annex 119A extended by 2 additional CWs.
- Assumptions are same as 802.3 Annex 119A:
  - First CW has AM block.
  - Constant transmission of Idle control characters.
  - Scrambler AM padding PRBS9 generator seed: P<0:8> = 0x100.
  - AM block tx_am_sf<2:0> = {0, 0, 0}.
  - Scrambler seed S<0:57> = 0x24E6959D0FA5DBD
- 8:1 symbol-pair mux for PMA lane ‘n’ is done between PCS lanes {n*8, n*8+1, .. , n*8+7}.



Graphic description – 200G BASE-R 8:1

VP1:

8 aligned PCS lanes

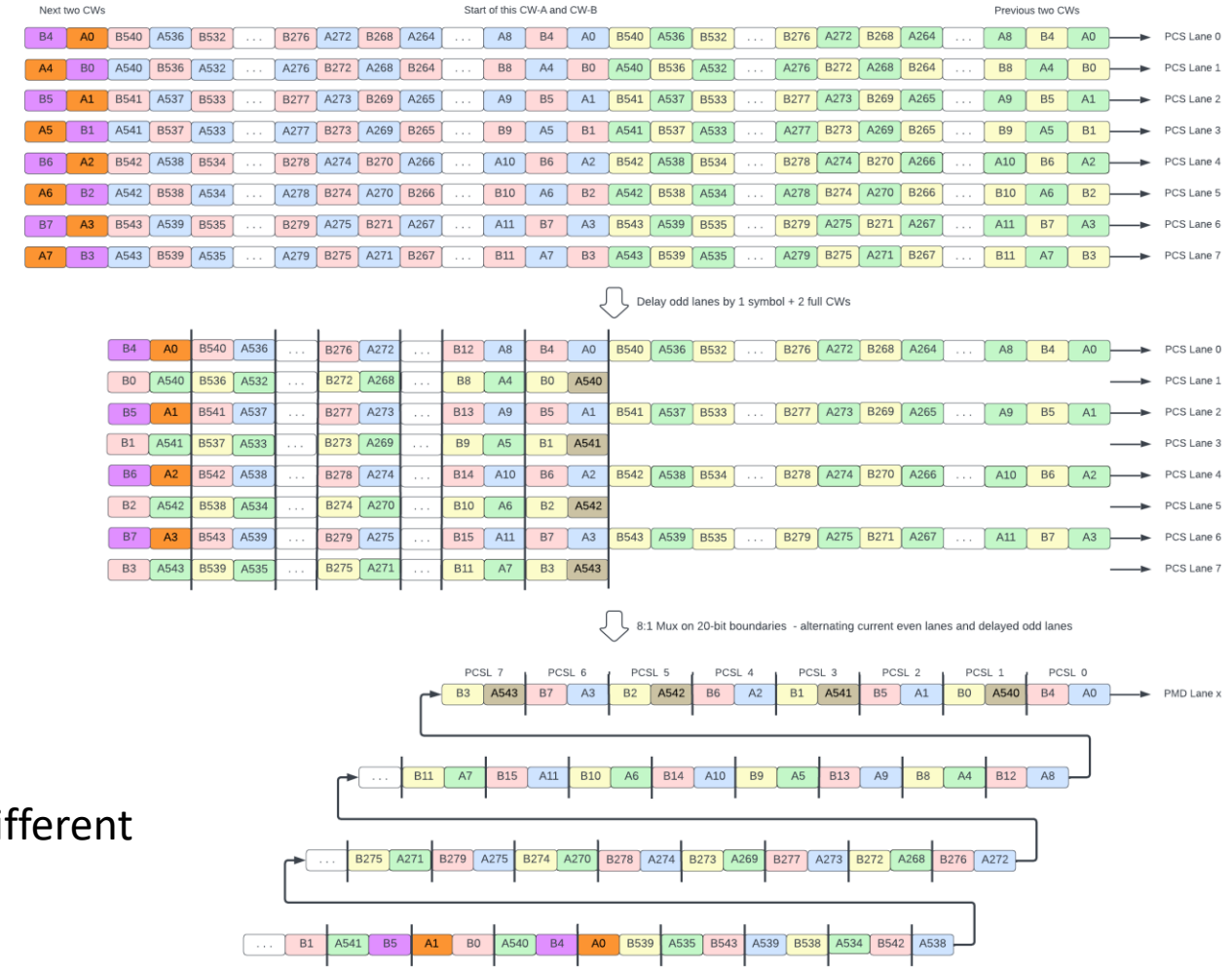
VP2:

Delay odd PCS lanes by 2 CWs + 1 RS-symbol.

VP3:

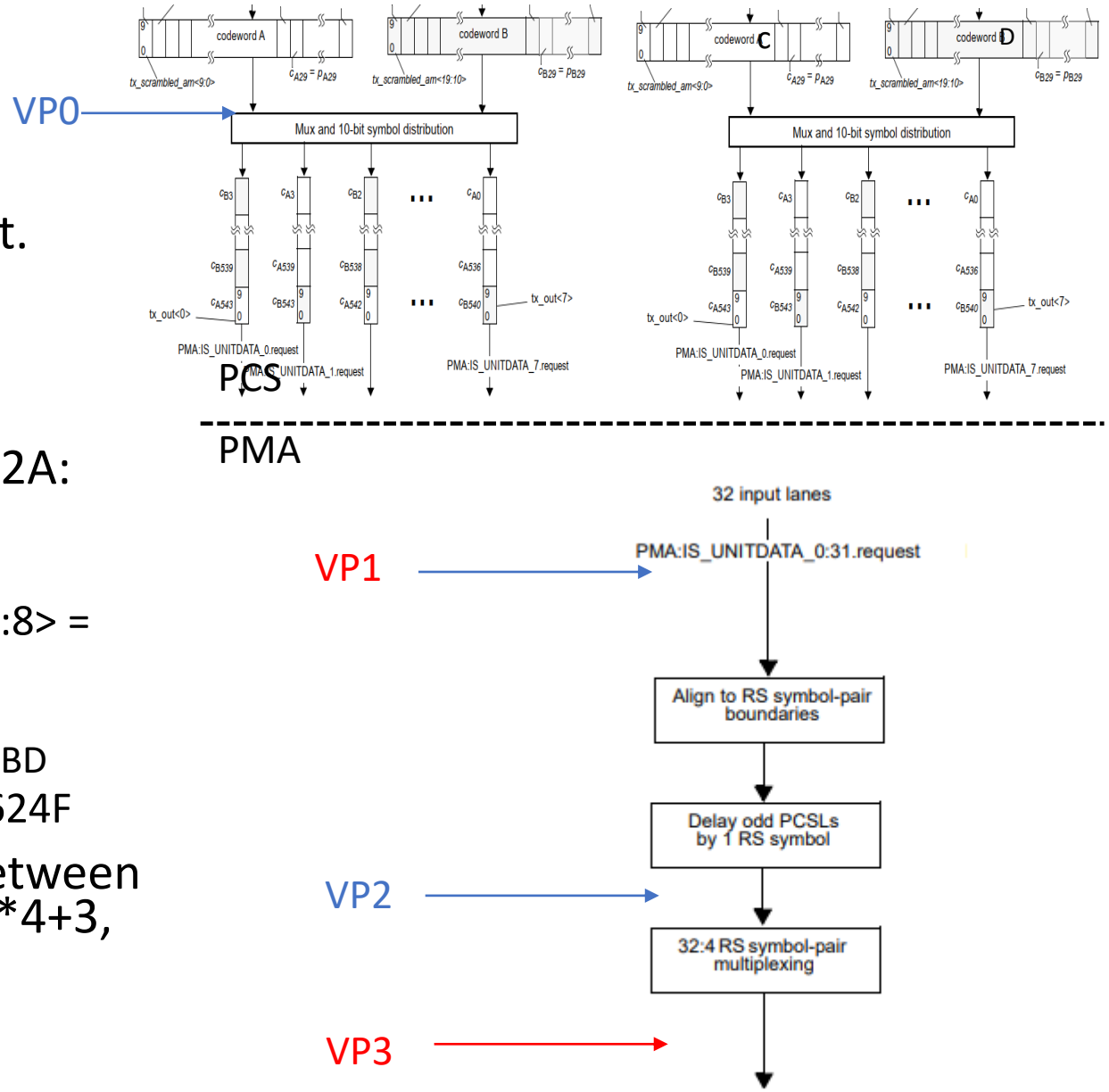
Symbol pair mux output.

Every consecutive 4 RS symbols belong to 4 different CWs.



Vector points (800GE)

- Test vectors are given for test points on the right.
  - VP1 and VP3 are required for interoperability.
  - VP0 and VP2 are given as a reference for debug.
- VP0 is identical to Annex 172A.
- VP0 assumptions are same as 802.3df Annex 172A:
  - First CW has AM block.
  - Constant transmission of Idle control characters.
  - Scrambler AM padding PRBS9 generator seed: P<0:8> = 0x100.
  - AM block tx_am_sf<2:0> = {0, 0, 0}.
  - Flow 0 scrambler seed S<0:57> = 0x24E6959D0FA5DBD
  - Flow 1 scrambler seed S<0:57> = 0x1FB58857D81624F
- 8:1 symbol-pair mux for PMA lane ‘n’ is done between PCS lanes {n*4, n*4+16, n*4+1, n*4+16+1 .., , n*4+3, n*4+16+3}.



Graphic description – 800G BASE-R 32:4

VP2:

Delay odd PCS lanes by 1 RS-symbol.

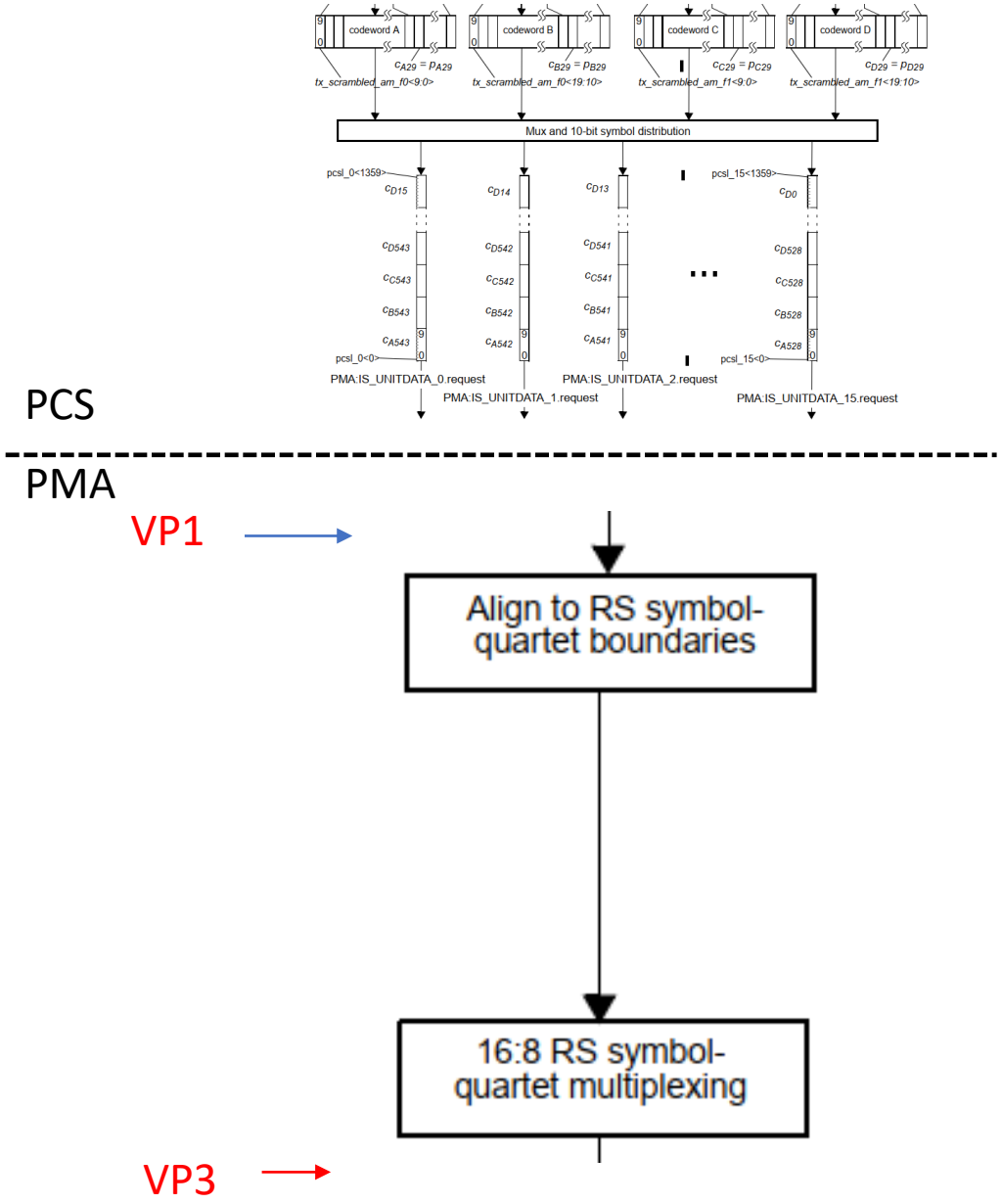
VP3:

Symbol pair mux output.

Every consecutive 4 RS symbols belong to 4 different CWs.

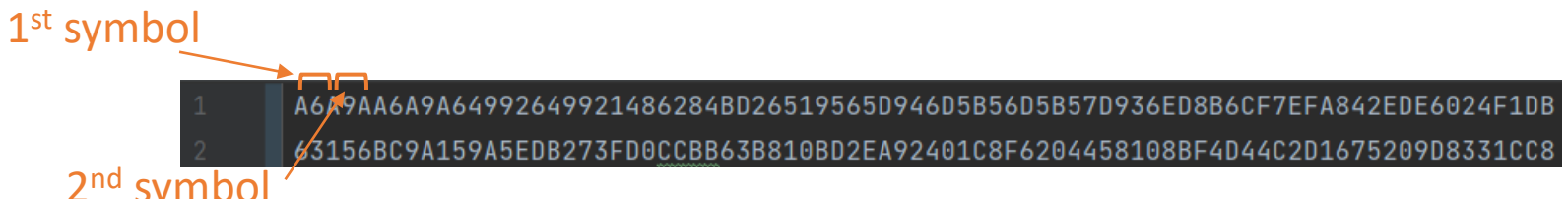
Vector points (1.6TE)

- Test vectors are given for test points on the right.
  - VP1 and VP3 are required for interoperability.
  - VP1 relies on 802.3dj draft 1.0 Annex 175A.
  - VP2 is not required since there is no odd lanes delay for 1.6T.
- 2:1 symbol-quartet mux for PMA lane ‘n’ is done between PCS lanes {n*2, n*2+1}.



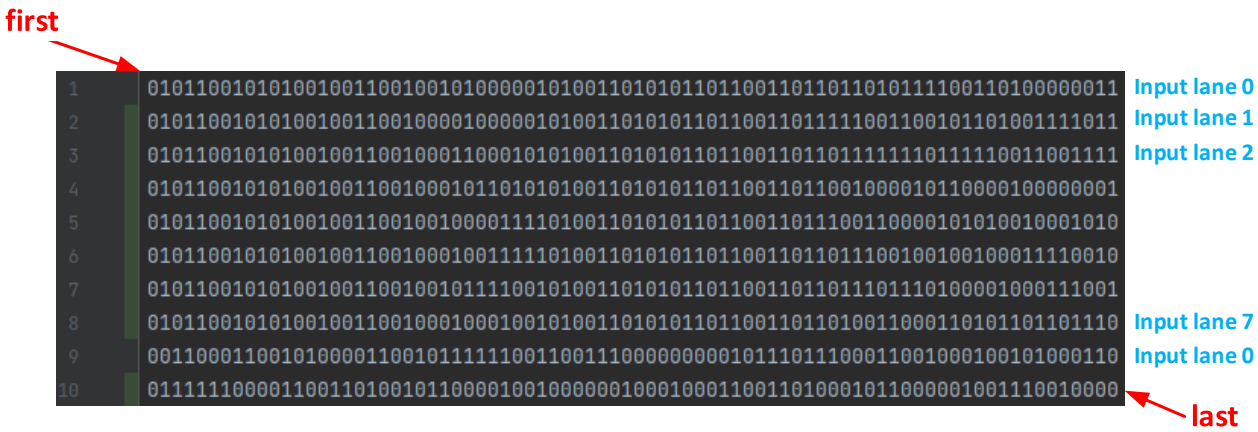
Test vector format

- For all VPs except VP0 transmission order inside a line is from left to right top to bottom.
- For VP0 bits ordering is same as in Annex119A. Inside a 10b symbol bits are transmitted from LSB to MSB, and 10b symbols are transmitted from left to right.
- **VP0**:
  - Same as defined in **Annex 119A (hex stream with 320 bits / 80 hex per line)**
  - Separate files for codeword A and codeword B (2 codewords per file, 34 lines)



- **VP1-2:**
  - Text file per PMA output lane.
  - Each line is 80 bits, binary form, belongs to each input PCS lane.
  - X is used for don't care, caused by adding delay on odd lanes.

Port		input lane 0	input lane 1	input lane 2	input lane 3	input lane 4	input lane 5	input lane 6	input lane 7
200GE	PMA lane 0	PCS lane 0	PCS lane 1	PCS lane 2	PCS lane 3	PCS lane 4	PCS lane 5	PCS lane 6	PCS lane 7
400GE	PMA lane 0	PCS lane 0	PCS lane 1	PCS lane 2	PCS lane 3	PCS lane 4	PCS lane 5	PCS lane 6	PCS lane 7
	PMA lane 1	PCS lane 8	PCS lane 9	PCS lane 10	PCS lane 11	PCS lane 12	PCS lane 13	PCS lane 14	PCS lane 15
800GE	PMA lane 0	PCS_lane0	PCS_lane16	PCS_lane1	PCS_lane17	PCS_lane2	PCS_lane18	PCS_lane3	PCS_lane19
	PMA lane 1	PCS_lane4	PCS_lane20	PCS_lane5	PCS_lane21	PCS_lane6	PCS_lane22	PCS_lane7	PCS_lane23
	PMA lane 2	PCS_lane8	PCS_lane24	PCS_lane9	PCS_lane25	PCS_lane10	PCS_lane26	PCS_lane11	PCS_lane27
	PMA lane 3	PCS_lane12	PCS_lane28	PCS_lane13	PCS_lane29	PCS_lane14	PCS_lane30	PCS_lane15	PCS_lane31
1.6TE	PMA lane 0	PCS lane 0	PCS lane 1						
	PMA lane 1	PCS lane 2	PCS lane 2						
	PMA lane 2	PCS lane 4	PCS lane 4						
	PMA lane 3	PCS lane 6	PCS lane 6						
	PMA lane 4	PCS lane 8	PCS lane 8						
	PMA lane 5	PCS lane 10	PCS lane 10						
	PMA lane 6	PCS lane 12	PCS lane 12						
	PMA lane 7	PCS lane 14	PCS lane 14						



Test vector format

- **VP3**
  - Text file per PMA lane
  - Each line is 160 bits
  - X is used for don’t care, caused by adding delay on odd lanes.

```
0101100101010010011xxxxxxxxxxxxxxxxxxxx0101100101010010011xxxxxxxxxxxxxxxxxxxx0101100101010010011xxxxxxxxxxxxxxxxxxxx0101100101010010011xxxxxxxxxxxxxxxxxxxx
0100101000001010011xxxxxxxxxxxxxxxxxxxx0100011000101010011xxxxxxxxxxxxxxxxxxxx0100100001111010011xxxxxxxxxxxxxxxxxxxx0100101111001010011xxxxxxxxxxxxxxxxxxxx
1010110110011011011xxxxxxxxxxxxxxxxxxxx1010110110011011011xxxxxxxxxxxxxxxxxxxx1010110110011011001xxxxxxxxxxxxxxxxxxxx1010110110011011011xxxxxxxxxxxxxxxxxxxx
1011110011010000011xxxxxxxxxxxxxxxxxxxx1111011111001100111xxxxxxxxxxxxxxxxxxxx1000010101001000101xxxxxxxxxxxxxxxxxxxx0111010000100011100xxxxxxxxxxxxxxxxxxxx
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Test vectors folder content

The test vectors is divided into 4 folders, each contains files as listed below.

- 200GBASE-R 8:1
  - vp0_cws_[a..b].txt
  - vp1_lane0.txt
  - vp2_lane0.txt
  - vp3_lane0.txt
- 400GBASE-R 16:2
  - vp0_cws_[a..b].txt
  - vp1_lane[0..1].txt
  - vp2_lane[0..1].txt
  - vp3_lane[0..1].txt
- 800GBASE-R 32:4
  - vp0_cws_[a..d].txt
  - vp1_lane[0..3].txt
  - vp2_lane[0..3].txt
  - vp3_lane[0..3].txt
- 1.6TBASE-R 16:8
  - vp1_lane[0..7].txt
  - vp3_lane[0..7].txt

Summary

- 200G per lane PMA (CL176) interoperability test vectors are proposed.