



# By-passing the DR/FR inner FEC code for 200G/Lane.

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# Introduction

- An inner code in addition to the RS (544,514) has been adopted for 200G/Lane DR and FR optical specifications in 802.3dj.
- This relaxes the requirements on the optical link as well as the chip to module links
- For some applications bypassing this inner code is desirable to reduce latency, and at the San Antonio meeting in May 2023 a straw poll indicated interest in looking at options to do this.
- This presentation proposes a method to achieve this without creating multiple different optical modules and specifications.

# Proposal.

- At start up all links come up with the inner code enabled.
- Once the link is established the inner hamming code corrected error rate for the optical link is determined by the DSP in the module.
- Based on a threshold inner code error rate that the host provides to the module the module uses the side-band communication link provided in the stuffing bits of the inner code to request that the link “by-passes the inner code”. (see [https://www.ieee802.org/3/dj/public/23\\_03/ramesh\\_3dj\\_01a\\_2303.pdf](https://www.ieee802.org/3/dj/public/23_03/ramesh_3dj_01a_2303.pdf))
- If both ends of the link agree that the inner code should be by-passed they change to “by-passed inner code mode”. The signal is transmitted without adding the inner code i.e. at 106.25GBaud with just the RS (544,514) FEC.
- If the link does not have adequate performance with the inner code bypassed the link is dropped and link-up re-started with the option to by-pass the inner code disabled.

# Advantages.

- Provides Ethernet plug and play.
  - No need to have different specifications or different modules.
  - No need to have two PMDs for the same objective.
- Host can determine what trade-off is wanted between latency and BER margin.
- Communication across the optical link is provided in a robust manner when the link is established.
- Due to variation in channels and module manufacturing variations many links are likely to be able to operate with the inner FEC bypassed without impacting manufacturing yields. i.e. worst case Tx with worst case Rx with worst case channel is not likely to be common.

# Variant of the proposal

- Instead of just using the inner hamming code error rate measured by the DSP in the module to determine whether “inner code bypass” is requested, the module would communicate this to the host ASIC which would use this and the uncorrected RS FEC symbol error ratio measured by the host ASIC (based on corrected RS codeword ratio) to determine whether the inner code bypass is requested.
- The “request inner code bypass” message would be passed from the host ASIC to the module to be transferred to the module at the other end of the link.
- Advantage of this variant is that if the host BER (C2M plus C2C (if used)) is better than the allocated worst case then the by-passed inner FEC mode can be used on somewhat worse optical links.