

1.6TbE alignment marker characteristics

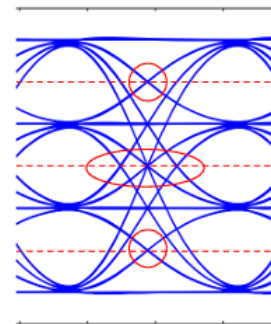
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IEEE 802.3dj

Introduction

- Baseline Wander
 - definition: the instantaneous offset (in %) in the signal generated by AC coupling at the Baud/10000
 - see p.4 of [anslow 01 1016 logic](#)
- Clock Content
 - definition: create a function which is a 1 for a transition and a 0 for no transition and then filter the resulting sequence with a corner frequency of Baud/13281
 - see p.5 of [anslow 01 1016 logic](#)

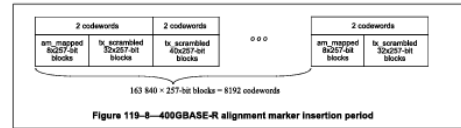


All transitions

1.6TbE Alignment Markers

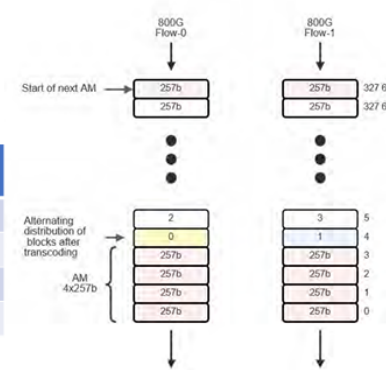
- From adopted baseline [gustlin 3dj 01b 230206](#)

Alignment Marker Insertion



- Markers inserted at consecutive 257b blocks across both 800G flows
- Uses 16 PCSL
 - Total size of markers is same as 400GbE
 - Increased spacing between markers to maintain frequency of arrival.

GbE	#PCSL	AM group size (x 257b)	Spacing (in CWs)	#PCSL flows	AM Spacing (in 257b per flow)
200	8	4	4k	1	81,920
400	16	8	8k	1	163,840
800	32	16	16k	2	163,840
1600	16	8	32k	2	327,680



Alignment Marker Encoding

- With 16 PCSL
- CM0-CM5 and UP0-UP2 are unchanged from 400GbE CL119
- UM0-UM5 are inverted from 400GbE
- Resulting UMs differ from 400GbE and 800GbE
- Clock Content and Baseline Wander Analysis – TBD
- UP and UM values can be adjusted if necessary
- Open issue: How to form the AMs in a coherent way so they appear correctly on physical lanes

PCSLane #	Encoding															
	CM0	CM1	CM2	UP0	CM3	CM4	CM5	UP1	UM0	UM1	UM2	UP2	UM3	UM4	UM5	
0	0x9A	0x4A	0x26	0x86	0x65	0x85	0xD9	0xD9	0xFE	0x8E	0xD0	0x26	0x01	0x71	0xF3	
1	0x9A	0x4A	0x26	0x04	0x65	0x85	0xD9	0x67	0xA5	0x21	0x81	0x98	0x5A	0xD0	0x7E	
2	0x9A	0x4A	0x26	0x46	0x65	0x85	0xD9	0xFE	0xC1	0xD0	0xA9	0x01	0x3E	0xF3	0x56	
3	0x9A	0x4A	0x26	0x5A	0x65	0x85	0xD9	0x84	0x79	0x7F	0x2F	0x78	0x86	0x80	0xD0	
4	0x9A	0x4A	0x26	0xE1	0x65	0x85	0xD9	0x19	0xD5	0xA0	0xD0	0xE6	0x2A	0x51	0xF2	
5	0x9A	0x4A	0x26	0xF2	0x65	0x85	0xD9	0x4E	0xED	0xB0	0x2E	0xB1	0x12	0x4F	0xD1	
6	0x9A	0x4A	0x26	0x3D	0x65	0x85	0xD9	0xEE	0xB0	0x63	0x5E	0x11	0x42	0x9C	0xA1	
7	0x9A	0x4A	0x26	0x22	0x65	0x85	0xD9	0x32	0x29	0x89	0xA4	0xCD	0xD6	0x76	0x5B	
8	0x9A	0x4A	0x26	0x60	0x65	0x85	0xD9	0x9F	0x1E	0xB0	0x9A	0x60	0xE1	0x73	0x75	
9	0x9A	0x4A	0x26	0x68	0x65	0x85	0xD9	0xA2	0xB0	0x38	0xC3	0x5D	0x71	0xC4	0x3C	
10	0x9A	0x4A	0x26	0xF4	0x65	0x85	0xD9	0x04	0x6A	0x14	0x27	0xF8	0x95	0xE8	0xD8	
11	0x9A	0x4A	0x26	0x6C	0x65	0x85	0xD9	0x71	0xDD	0x99	0xC7	0xB0	0x22	0x66	0x38	
12	0x9A	0x4A	0x26	0x18	0x65	0x85	0xD9	0x58	0x5D	0x09	0x6A	0xA4	0xA2	0xF6	0x95	
13	0x9A	0x4A	0x26	0x14	0x65	0x85	0xD9	0xCC	0xCE	0x68	0x3C	0x33	0x31	0x97	0xC3	
14	0x9A	0x4A	0x26	0xD0	0x65	0x85	0xD9	0xB1	0x35	0x04	0x59	0x4E	0xCA	0xFB	0xA6	
15	0x9A	0x4A	0x26	0xB4	0x65	0x85	0xD9	0x56	0x59	0x45	0xB6	0xA9	0xA6	0x8A	0x79	

Note: in table above, bolded text indicates inverted values from CL 119 AM values

1.6TbE AM Insertion

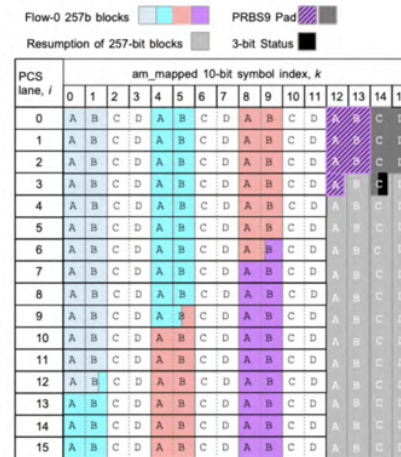
- From PCS lane info and AM insertion [opsasnick 3dj 01a 2303](https://www.etsi.org/deliver/etsi_ts/138900/138903_01a/138903_01a2303.pdf)

1.6TbE AM pattern across PCS lanes

- AM data is eight 257-bit blocks
 - 4x257b inserted by each flow
- 120-bit AM marker per PCS lane

In figure to right:

 - Symbols 0-11 of each lane are defined AM values
 - 257-bit AM blocks inserted by Flow-0 (CW-A and CW-B) highlighted in color
 - Padding in PCSLs 0-3, Symbols 12-15
 - 68-bits padding in Flow-0
 - 65-bits padding + 3-bit status in Flow-1
 - PRBS9 padding data in each flow is independently generated per flow.
 - Each flow should use different seeds for the PRBS9 pattern
 - TX AM status Field (tx_am_sf<2:0>)
 - Only at end of padding in Flow-1
 - Status is based on all 4 CWs



1.6TBASE-R Alignment marking mapping to PCS lanes

1.6TbE AM Insertion

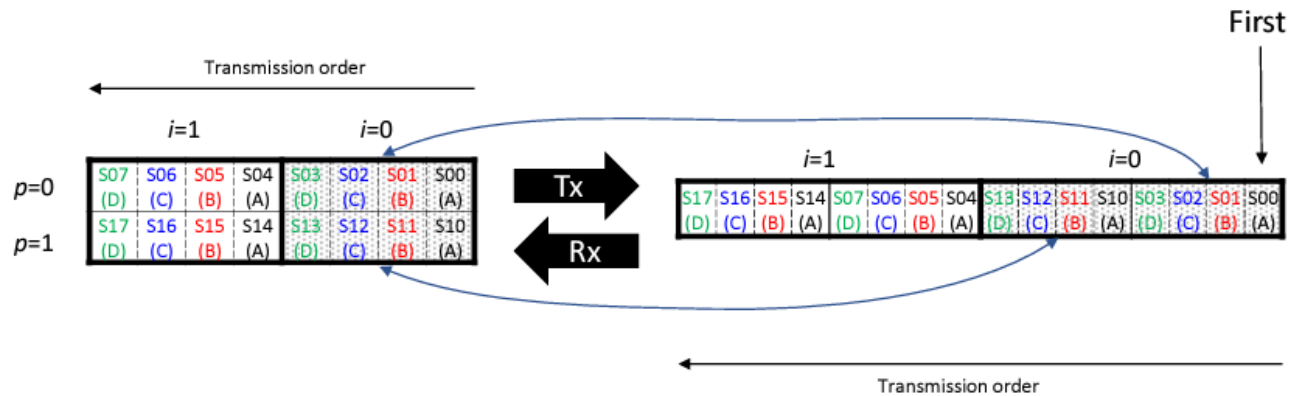
- Each flow requires a unique insertion pattern definition to make the AMs appear on the PCS lanes correctly since all 4 CWs are inserted into each PCS lane.
- For each of the sixteen 120-bit AMs:
 - AM bits 0-19, 40-59 and 80-99 come from Flow-0
 - AM bits 20-39, 60-79 and 100-119 come from Flow-1
 - Plus additional padding is added to align to a 257b boundary

1.6TbE Symbol-quartet multiplexing

- From PMAs with 200G signaling [ran 3dj 01a 2303](#)

Symbol-quartet multiplexing illustration
PMA(16:8) – 1.6T PHYs

(1 out of 8 lanes illustrated)

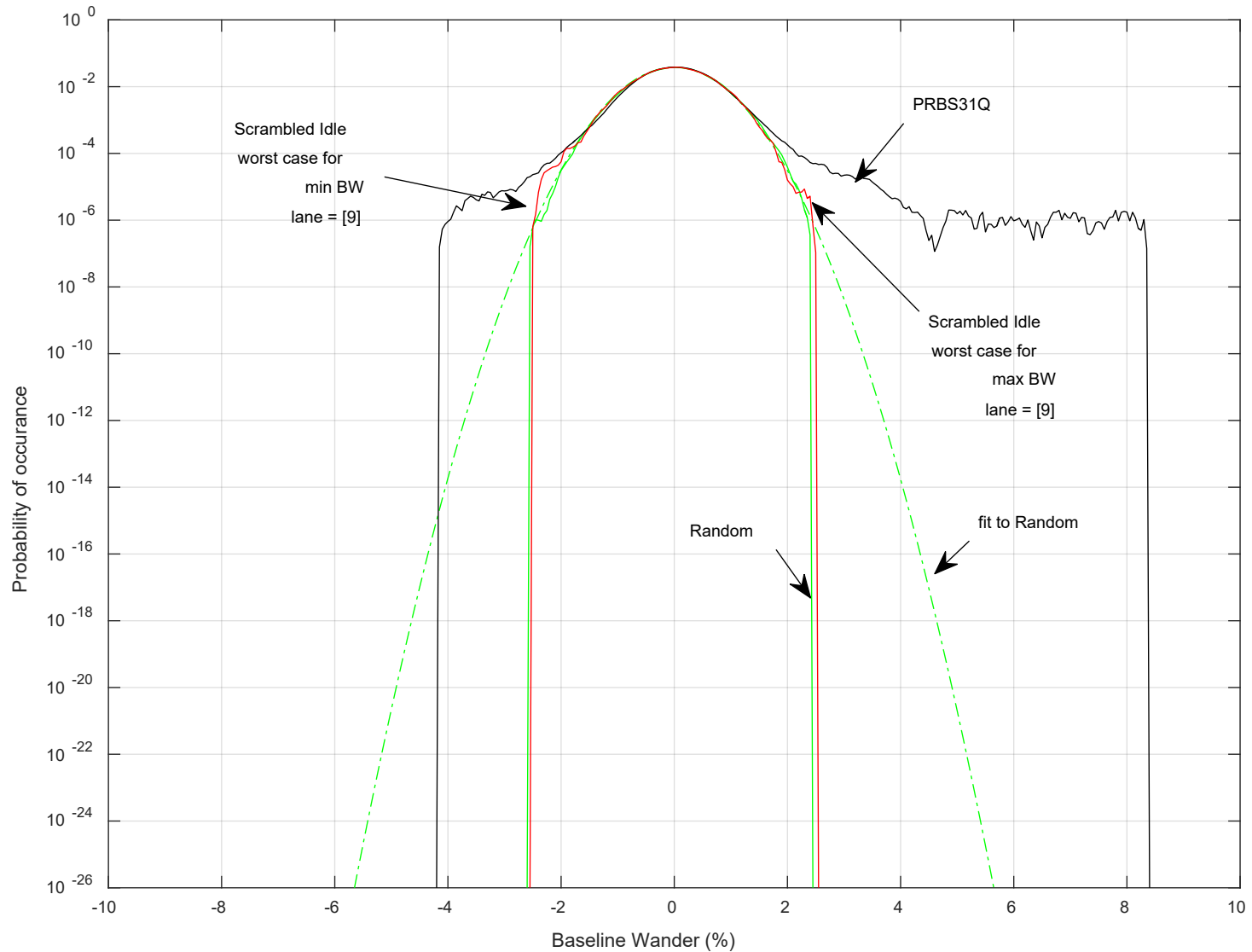


S_{pq} denotes the 10-bit symbol with index q on the PCSL with index p within the set of 2 PCSLs, after alignment to 40-bit boundary relative to the AM

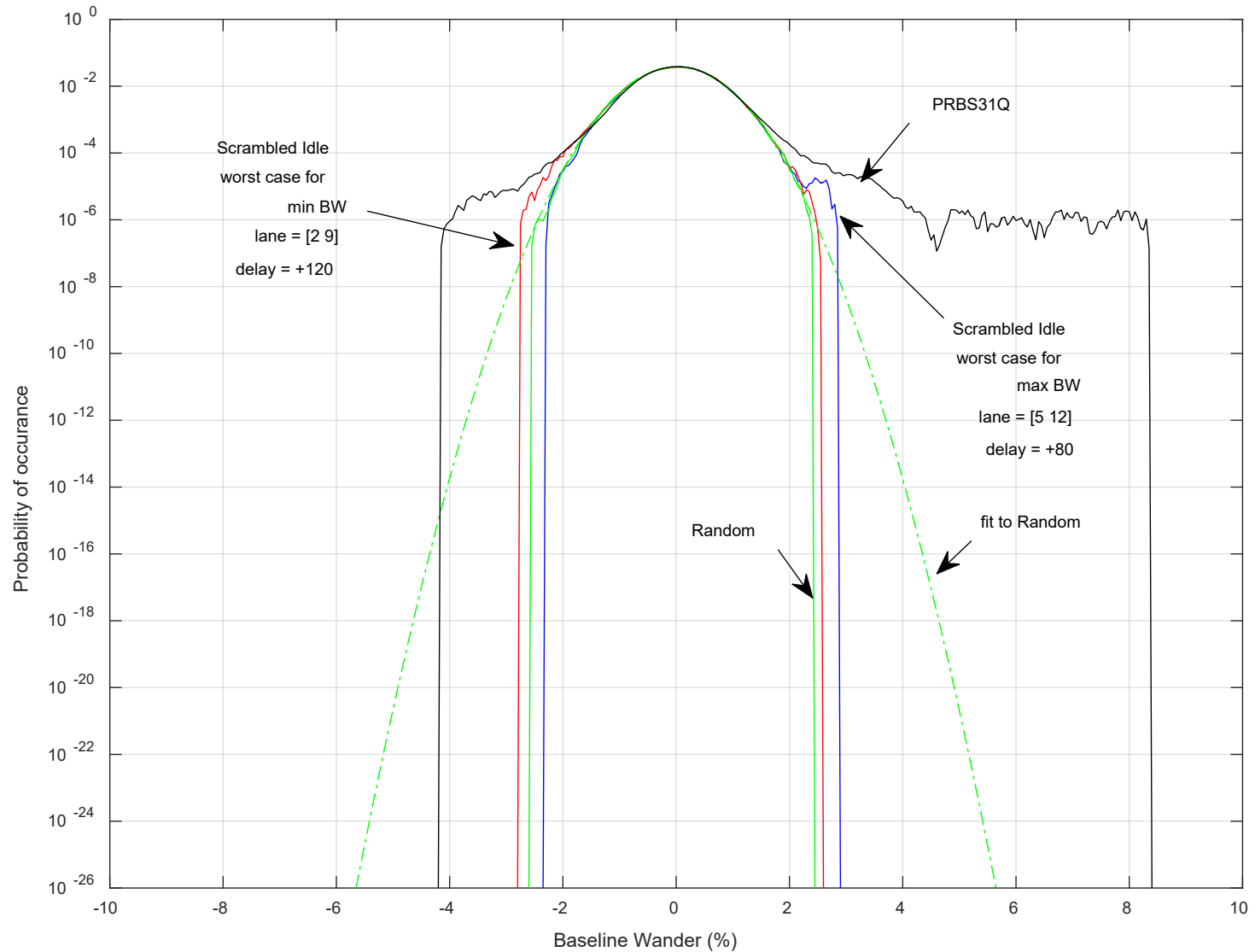
Simulations

- All sixteen 1.6TbE scrambled idle 100Gb/s lanes were analyzed to find the worst cases for Baseline Wander and Clock Content after Gray coding to PAM4 symbols.
- All possible 2:1 combinations of PCS lanes for symbol quarter multiplexing for 1.6TbE scrambled idle 200Gb/s lanes were analyzed to find the worst cases for Baseline Wander and Clock Content after Gray coding to PAM4 symbols. These searches included lane delays of (-160, -120, -80, -40, 0, +40, +80, +120, +160) bits, which are multiples of 40 bits.

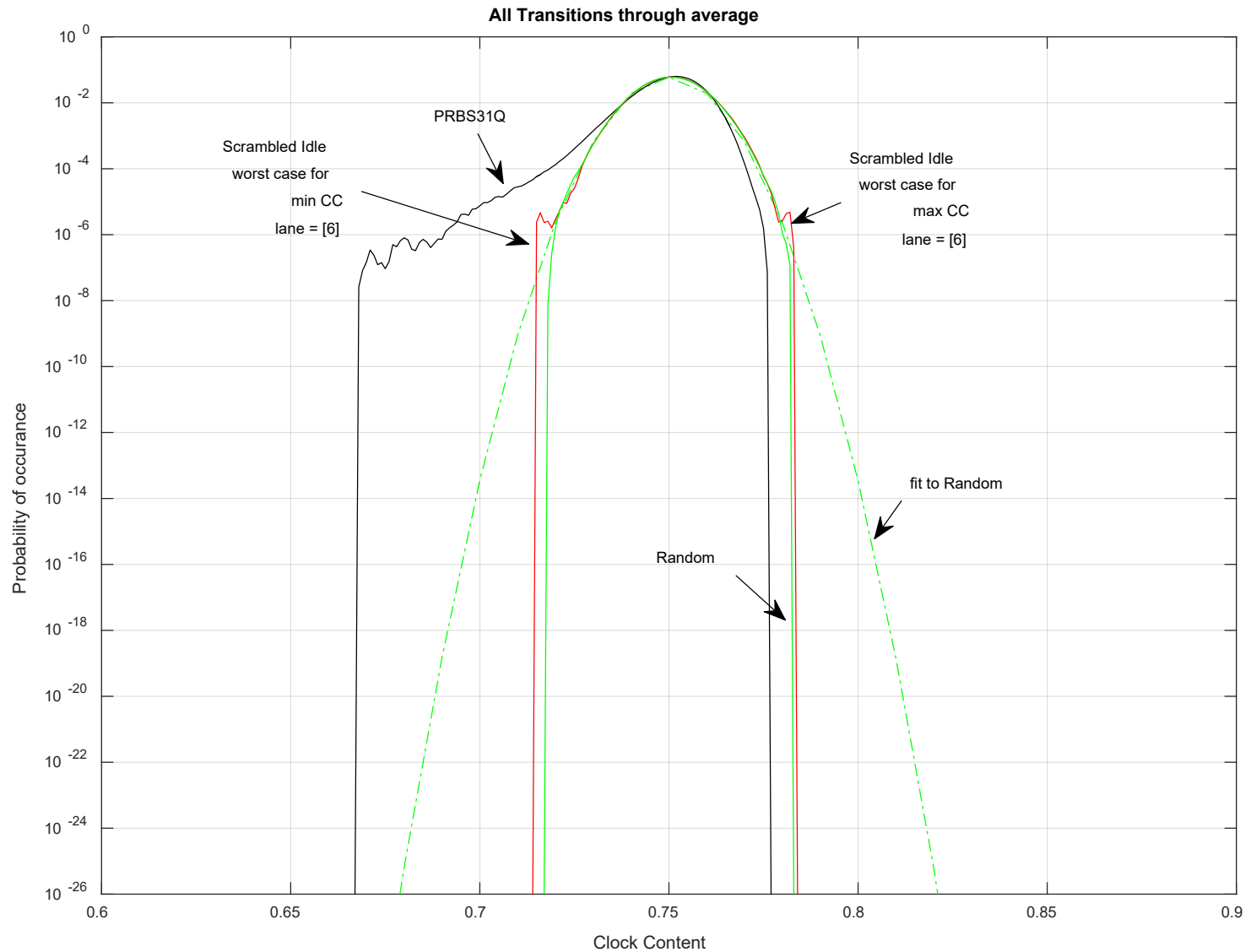
Baseline Wander, 100G lanes, 1.6T markers



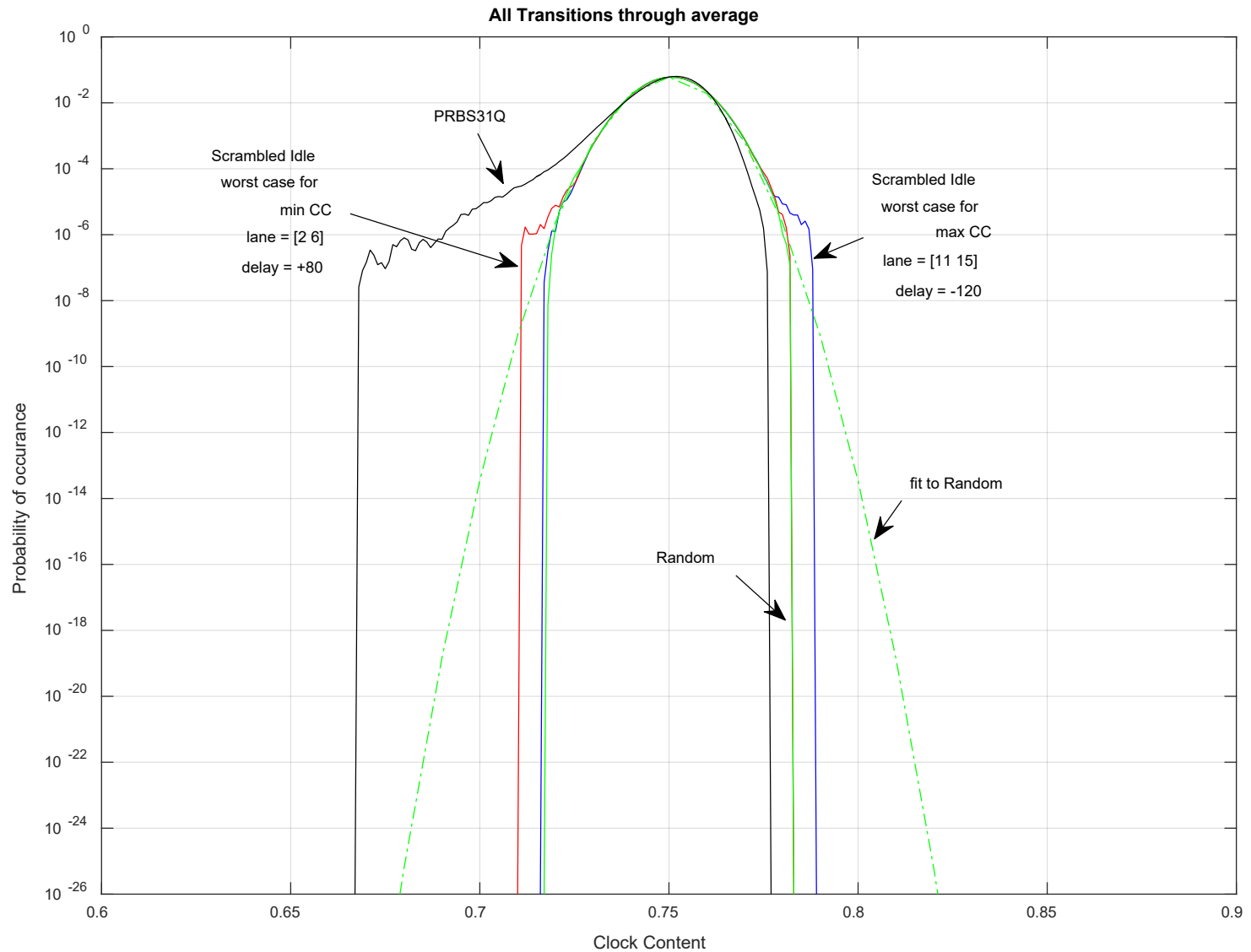
Baseline Wander, 200G lanes, 1.6T markers



Clock Content, 100G lanes, 1.6T markers



Clock Content, 200G lanes, 1.6T markers



Summary

- The baseline wander and clock content for the 1.6TbE alignment markers show a slightly worse “shoulder” on some combinations, but they remain within the “mask” obtained by the PRBS31Q test pattern.
- No shift of clock content, i.e. reduction in PAM4 transition density, were found.

THANK YOU