Considering “FEC Bypass”

IEEE P802.3dj Task Force
Joint Optics / Logic Ad Hoc
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Introduction

- Key Motions & Strawpolls related to "FEC Bypass"
  - Mar 2023 – Motion #5
    - A concatenated FEC approach (see patra_3dj_01b_2303) has been adopted for DRx, DRx-2, FR4, and LR4 for relevant objectives @ 200 GbE, 400 GbE, 800 GbE, and 1.6 TbE.
  - July 2023 - Motion #9
    - Adopted direction to "adding an option to support only RS544 FEC (aka Bypass Inner FEC) for the single wavelength 500m and 2km optical PMDs"
      - Note – does not state the reach in this mode
  - 15 Aug 2023 Strawpoll Results

    I would support adding objectives to support physical layer specifications based on only RS544 FEC for:

    1. Single wavelength 500m and 2km optical PMDs :
       - 200GBASE-DR1, 400GBASE-DR2, 800GBASE-DR4, and 1.6TBASE-DR8
       - 200GBASE-FR1, 400GBASE-DR2-2, 800GBASE-DR4-2, and 1.6TBASE-DR8-2
    2. Four wavelength 2km optical PMD
       - 800GBASE-FR4

    Results:

    Q1 (y/n/a): 30/26/16
    Q2 (y/n/a): 20/34/18

- This presentation will consider the implications of implementing "FEC Bypass" by continuing forward with current objectives.
- This presentation builds on https://www.ieee802.org/3/dj/public/adhoc/optics/0823_OPTX/dambrosia_3dj_optx_01b_230815.pdf

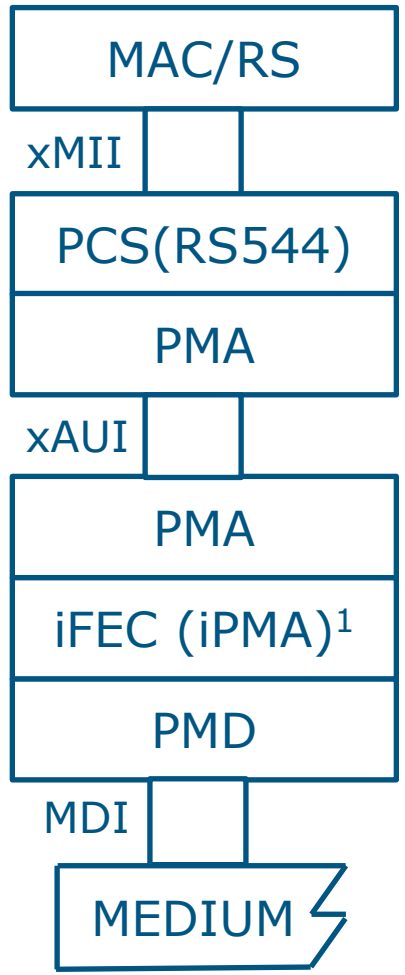
Observations

- The following motion has created the potential for individual interpretation
  - July 2023 - Motion #9
    - Adopted direction to "adding an option to support only RS544 FEC (aka Bypass Inner FEC) for the single wavelength 500m and 2km optical PMDs"
- This motion is causing a lot of confusion and can be interpreted in multiple ways
  - "only RS544 FEC"
    - Only need to implement RS544 (not inner FEC)?
    - One of two modes? Which are mandatory to implement?
    - A single PHY or two different PHYs?
  - for the single wavelength 500m and 2km optical PMDs
    - What is the reach? The stated objective? Reduced reach? Other?
      - There are no objectives for reduced reach –DRx / -DRx-2 PHYs
- Clarification of "FEC Bypass" is necessary

- This presentation explores the concept "FEC Bypass" to explore what needs clarification

“FEC Bypass” Proposal Summary

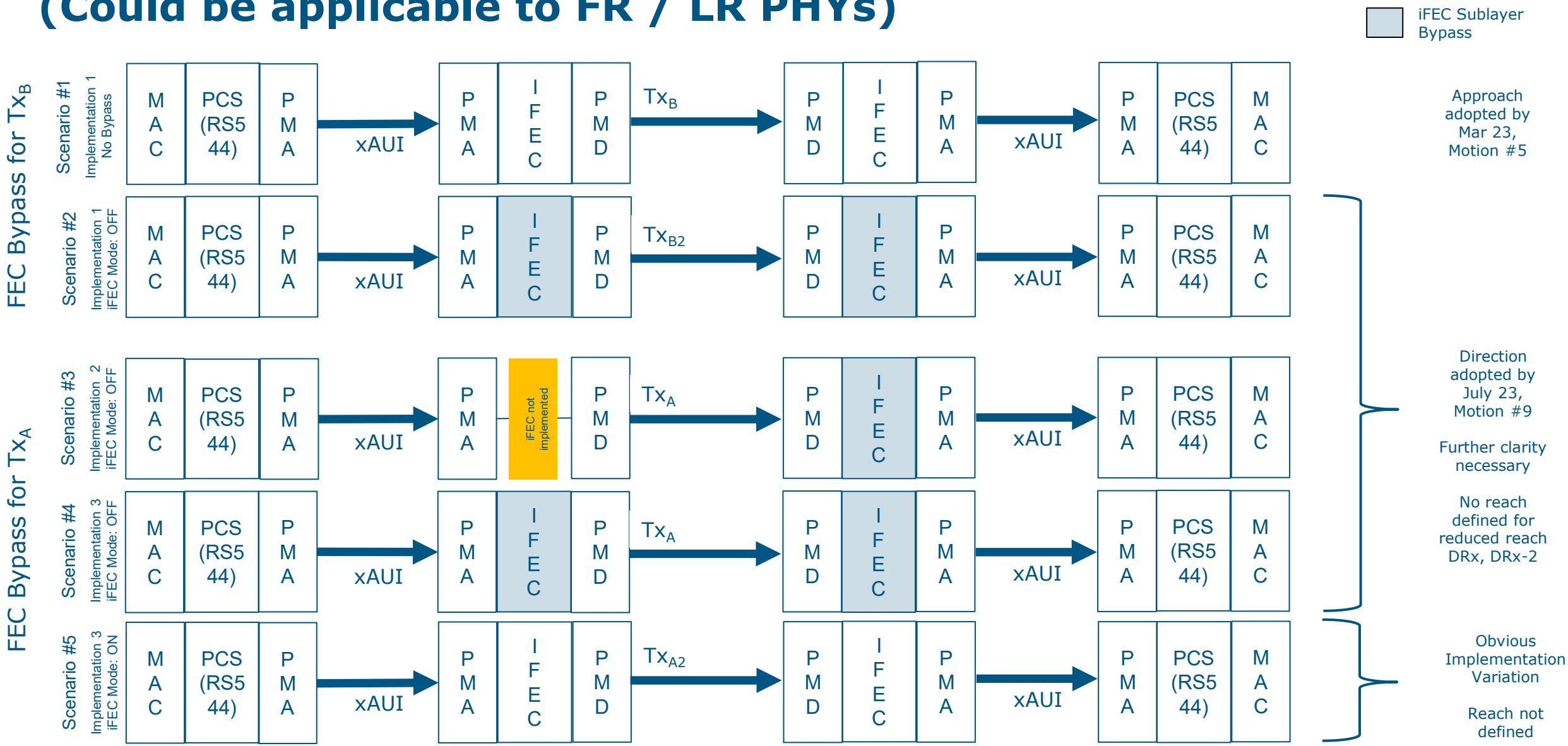
- Inner-FEC bypass is an option for latency sensitive applications
- Transmitter
  - Two classes of transmitters (different specifications, including bit rate)
    - Tx_A – inner FEC OFF (106.25 +/- 50 ppm GBd)
      - Tx_{A2} is Tx_A run at 113.4357 if FEC ON
    - Tx_B – inner FEC ON (113.4375 +/- 50 ppm GBd)
      - Tx_{B2} is Tx_B run at 106.25 if FEC OFF
  - No stated requirement to support both classes of transmitters
  - No stated requirement whether support of inner FEC is mandatory
- Common receiver that accommodates both transmitters
  - Receivers must support RS544 and RS544+inner code mode
  - Requirement for the approach to be single PHY
- PMD BER
  - For Tx_A: 2.4x10-4
  - For Tx_B: 3.0x10-3
- How will PHY modes be switched between?
  - For this presentation “Auto negotiation” is not being assumed



xBASE-DRx
xBASE-DRx-2
800GBASE-FR4

Note 1 – Conditional based on PHY mode and implementation

DR / DR-2 Implementation Considerations (single direction only) (Could be applicable to FR / LR PHYs)



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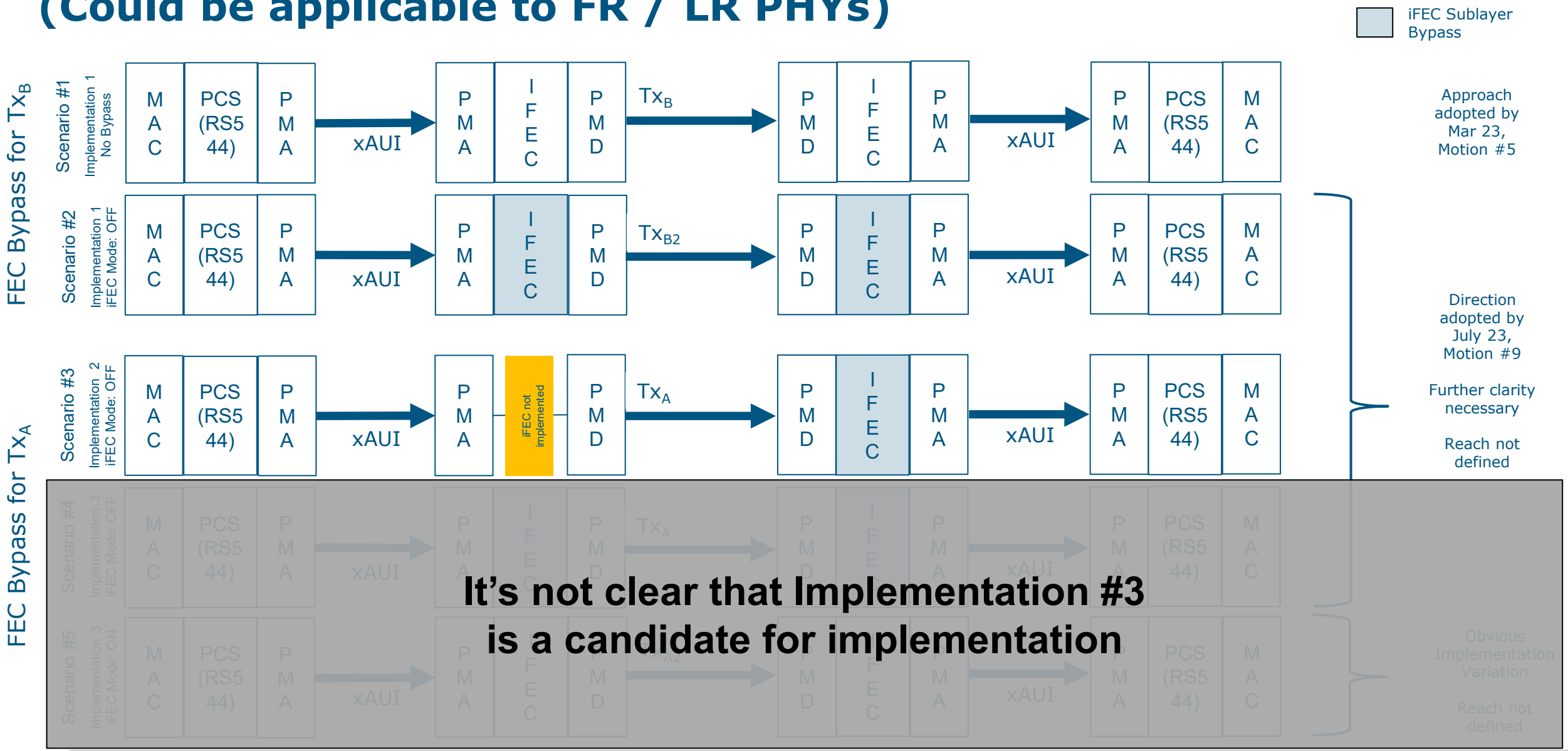

Summary Table

Scenario	Implementation	iFEC Mode	Tx Class	Comments
1	1	On	Tx_B	• Adopted by Motion to meet reach objective requirements
2	1	Off	Tx_{B2}	• Meets RS544 only directional motion • An approach to meet a shorter (TBD) reach requirement without inner FEC (Note – no supporting project objective) • TxB (FEC off) is not the same as TxA
3	2	n/a	Tx_A	• Meets RS544 only directional motion • Interpreted as alternative approach to meet reach requirement without inner FEC
4	3	Off	Tx_A	• Candidate for implementation? • Meets RS544 only directional motion • Interpreted as alternative approach to meet reach requirement without inner FEC
5	3	On	Tx_{A2}	• Candidate for implementation? • An opportunity to meet a reach > the objective with a Tx better than TxB and inner FEC

Questions Still to be Answered

- Clarify of what was intended by term “FEC Bypass”
- Will the market accept this single PHY dual mode approach?
  - “Low-latency” approach will not be ensured by all solutions meeting the standard
- How will users identify “lower latency” PHYs?
  - Will market accept a standard that doesn’t differentiate PHYs and having to go to “data sheets” if a PHY is lower latency?
- Will all future optical transmitters meet Tx_A requirements i.e. no inner FEC necessary
- Will an optimized low latency only PHY (no inner FEC) be desired?

The Concept of “FEC Bypass” Terminology

- Potential interpretations of “FEC Bypass”
  - From a standards development perspective –
    - “FEC Bypass” implies that the inner FEC is mandatory to implement and discretionary to be turned on / off
  - Other
    - “FEC Bypass” was loosely used and
      - 1)inner FEC may be implemented and is not turned ON
      - Or 2) is not implemented
- Is FEC (mandatory / not applicable) to do in Tx, but mandatory to do in Rx
- “FEC modes” as used in 25GBASEKR / KR-S and 25GBASECR / CR-S could be used instead of “FEC BYPASS”

Summary

- Upon further review Motion #9 from July 2023 Plenary is unclear and can be interpreted to mean multiple things
- A well-defined baseline regarding the definition of a dual mode PHY is needed
- There are still questions regarding the market acceptance of a dual mode PHY approach that should be considered
- The use of the term “FEC Bypass” should be revisited
  - “FEC modes” as used in 25GBASEKR / KR-S and 25GBASECR / CR-S could be used instead of “FEC BYPASS”