Specifying BER in PMD clauses

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Outline

- This presentation addresses performance specifications in PMDs that are used with an inner FEC sublayer within optical modules.
  - Electrical PMDs (assumed not to use an inner FEC) and optical PMDS without inner FEC (“bypass”) are not discussed here.
- Questions:
  - At what point should module performance (e.g., BER) be specified?
  - Should performance be specified as BER or another metric?

Background – existing PMD specifications

- Existing PMD clauses in 802.3 have a BER specification with a common format.
  - BER is specified as "less than 2.4e-4" after processing by the PMA (clause 120 or clause 173)
    - Effectively this can be measured at the module's CDR (in the receive direction) or with an MCB
  - Errors are assumed to be "sufficiently random" to result in low enough FLR, otherwise a lower BER is required
    - FLR < 1.7e-12 (with 2-way interleaved FEC)
    - FLR < 3.4e-12 (with 4-way interleaved FEC)
  - Additional errors in other components of the Physical Layer (1e-5 per AUI) are accounted for.
- Clause 124 (as amended by P802.3df D3.0) is shown as an example.

124.1.1 Bit error ratio

Change the first paragraph of 124.1.1 as follows:

The bit error ratio (BER) for 400GBASE-DR4 and 400GBASE-DR4-2 PMDs, when processed according to Clause 120, shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap when processed according to Clause 120 and then Clause 119. ~~For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-11} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.~~

The bit error ratio (BER) for 800GBASE-DR8 and 800GBASE-DR8-2 PMDs, when processed according to Clause 173, shall be less than 2.4×10^{-4} provided that the error statistics are sufficiently random that this results in a frame loss ratio (see 1.4.344) of less than 3.4×10^{-12} for 64-octet frames with minimum interpacket gap when processed according to Clause 173 and then Clause 172.

For a complete Physical Layer, the frame loss ratio may be degraded to 6.2×10^{-11} for 64-octet frames with minimum interpacket gap due to additional errors from the electrical interfaces.

If the error statistics are not sufficiently random to meet this requirement, then the BER shall be less than that required to give a frame loss ratio of less than 1.7×10^{-12} for 64-octet frames with minimum interpacket gap.

What effect does this BER specification have?

- In TDECQ, the “target SER” parameter is assumed to be twice the BER
  - Clause 124 refers to Clause 121, where 121.8.5.3 has “4.8e-4”.
  - TECQ (124.8.5a) is defined with reference to TDECQ.
- In stressed received sensitivity (SRS)
  - Clause 124 refers to the definition in 121.8.10, which has “The BER is required to be met for the lane under test on its own”.
  - The stressed input is calibrated using SECQ – similar to TECQ.
- Therefore, SRS, TDECQ, and TECQ all depend implicitly on the BER specification.

What's new in 802.3dj?

- Inner FEC has been adopted for use in optical modules
  - Architecturally positioned above a PMA above the PMD – but practically inseperable
- The inner FEC assumes soft-input decoding…
  - The output of the PMD and the adjacent PMA in the receive direction cannot be defined as bits or symbols.
  - Using 802.3cw as an example, these will likely be defined using analog signals and their sampled values.
  - BER isn't well-defined before processing by the inner FEC.
- The error rate at the inner FEC decoder output depends on implementation and on the characteristics of the input signal.
  - Analysis of specific decoders can be found in literature, with simplistic assumptions (e.g., AWGN channel).
  - Models for realistic applications (optical channel, specific DSP and decoder) have not been presented or adopted in P802.3dj.
  - Even if pre-FEC decisions are made to enable pre-FEC BER measurement, it does not predict the statistics of post-FEC errors.

Recent relevant work

- Many contributions to P802.3dj discussed BER before the inner FEC decoder (“raw” or “pre-FEC” BER)
  - Several of these are quoted in dawe_3dj_01a_2303
  - More recent contributions include parthasarathy_3dj_01_2303, riani_3dj_01a_2303, patra_3dj_01b_2305, he_3dj_02_2305; There are likely others that I’ve missed
  - More recently, welch_3dj_01a_2307 has proposed text for BER requirements with and without the inner FEC (slide 4)
  - The language is “The BER of the PMD link”, different from existing specifications, and suggesting pre-FEC BER, though it is stated that “pre-FEC BER level is not finalized”
  - mi_3dj_01a_2307 discussed optical PMD specs focusing on testing; it assumed that testing is done for pre-FEC BER limits (see slide 5)
- Additionally…
  - In leyba_3dj_optx_01a_230629 it was indicated that with high target SER (matching the suggested pre-FEC BER), TDECQ resolution is lost and all transmitters look similar
    - This does not mean that the post-FEC receiver performance will also be similar
  - In ran_3dj_logic_01_230629 I showed that even post-FEC BER can’t predict the FLR on its own
    - Because errors are correlated, and the effect of RS-FEC depends strongly on the interleaving level
  - This presentation highlights additional issues with pre-FEC BER.
- Note that none of the proposals for coherent PMDs mentions any pre-FEC BER specifications.

Problem statement

- The effect of the module-to-module link errors (with inner FEC) on RS-FEC performance and FLR is complicated.
  - It cannot be predicted by looking at the output of the PMD or its adjacent PMA – because
    - PMD output is assumed to be “soft”
    - Different noise statistics at the PMD output are possible for the same “raw BER”
    - Different inner FEC decoder implementations can have different performance.
  - It cannot be predicted by the average BER at the module output – because
    - The “random error” model is invalid – errors at the output of the FEC decoder are correlated
    - There is a strong dependence on interleaving level
    - Even for given interleaving, different module implementations may affect the error distribution.
- Pre-inner-FEC BER is not meaningful for specification.
- What can we do?

Proposed direction

- BER for modules with inner FEC should be specified **where it is directly measurable with no assumptions** – at the output of the module (BASE-R PMA in the receive direction)
  - Consistent with how BER is specified in existing PMDs.
- The FLR for the module-to-module link (with inner FEC) must be no worse than it is with existing modules (without inner FEC)
  - Because the same RS-FEC is used, and the same additional BER should be allowed with 100 Gb/s per lane AUIs
  - In the BER specification subclause, we could use the existing “BER budget” of 2.4e-4 **assuming random errors** (although in practice this assumption is void)
  - However, the actual specification is a maximum FLR for the module-to-module link (1.7e-12 for 200G and 400G, 3.4e-12 for 800G and 1.6T). This can be specified explicitly.
  - Alternatively, we can specify that with additional random BER of 4e-5 (from other segments in a full link), the errors shall enable FLR lower than 6.2e-11.

More details

- How would receiver specifications be affected?
  - Formally, there is no change: for SRS, BER is required to be met (i.e., be low enough to meet the maximum FLR)
  - Test equipment with RS-FEC and inner FEC functionality may be used, and measure/predict FLR
  - Alternatively, a simpler PRBS-based test may be performed, measuring the module output raw BER, with limit based on interleaving level (e.g., see ran_3dj_logic_01_230629)
    - This has been done in AUI-C2C specifications, e.g., 120D.3.2.1
    - Note that for this method, the test pattern generator must create PRBS encoded by the inner FEC
- How would transmitter specifications be affected?
  - A possible conclusion from leyba_3dj_optx_01a_230629 is that TDECQ is inadequate for high SER values, and we may need another method
  - Can we define TDECQ to include the effect of an inner FEC soft-decision decoder, and keep the SER low?
  - This requires further discussion.

Summary

- Should we specify PMD performance (BER) before processing by the inner FEC (internal to the module) or after (at an observable point)?
  - For receiver specification – obviously after the inner FEC
  - For transmitter (TDECQ) – preferably after the inner FEC, but more work is required
- Should we keep the specification as “BER with random errors” or move to FLR or equivalent?
  - It is suggested that FLR or equivalent be stated as the normative requirement.
  - Alternative test methods using PRBS may be included.

That’s all

Questions? Discussion?