Enablement of multiple FEC modes for single-wavelength 200 Gb/s per lane 500 m and 2 km PMDs

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Overview

- There is a clear desire for an option to support single-wavelength 500 m and 2 km optical PMDs that operate without the Hamming(128, 120) inner code
  - Principal motivation is to provide a lower latency solution
  - See Motion #9 at the July meeting
    - Motion passed to add “an option to support only RS544 FEC (aka Bypass Inner FEC) for the single wavelength 500m and 2km optical PMDs“
- This presentation does not impact July Motion #9. FECo and FECi mode should be mandatory at the logical layer.
- This presentation makes a recommendation to specify two FEC modes at the PMD level:
  - Mode_FECi (mandatory)
  - Mode_FECo (optional)

Definitions

- **Mode_FECo**: Optical link runs with RS(544,514) FEC protection

- **Mode_FECi**: Optical link runs with RS(544,514) FEC protection operating as an outer code, supplemented by Hamming(128,120) FEC protection operating as an inner code

Option A: Define mandatory Mode_FECi and optional Mode_FECo

- Two FEC modes are defined
  - A mandatory specification based on Mode_FECi
  - An optional specification based on Mode_FECo
- Pros
  - No ambiguity that the standard requires the Hamming(128, 120) inner code
  - All modules will be inter-operable
  - However, the potential for lower latency implementations is supported by means of the optional Mode_FECo
  - No objective changes required
- Cons
  - No significant cons, some additional work to include the optional Mode_FECo specification tables
  - For future LPO or CPO, ASIC may need to include inner FEC

Option B: Define mandatory Mode_FECi. Mode_FECo PMD is unspecified

- Two FEC modes are defined
  - A mandatory specification based on Mode_FECi
  - A specification based on Mode_FECo is not provided
- Pros
  - No ambiguity that the standard requires the Hamming(128, 120) inner code
  - All modules will be inter-operable
  - However, the potential for lower latency implementations is not blocked by the standard because Mode_FECo exists at the logical layer.
  - No objective changes required
- Cons
  - No significant cons
  - For future LPO or CPO, ASIC may need to include inner FEC

Example Specification (Based on Option A)

Proposed Transmitter Specifications

- Mode_FECi (mandatory)

Description	200GBASE-DR1 400GBASE-DR2 800GBASE-DR4 1.6TBASE-DR8	200GBASE-FR1 400GBASE-DR2-2 800GBASE-DR4-2 1.6TBASE-DR8-2	Unit
Signaling rate, each lane (range)	113.4375 ± 50 ppm	113.4375 ± 50 ppm	GBd
Modulation Format	PAM4	PAM4	
Lane wavelengths (range)	1304.5 to 1317.5	1304.5 to 1317.5	nm
Side-mode suppression ratio (SMSR), (min)	30	30	dB
Average launch power, each lane (max)	4	4	dBm
Average launch power, each lane (min)	-2.8	-2.1	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane(max)	4.2	4.2	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane(min) for TDECQ < 1.4 dB for 1.4 dB ≤ TDECQ ≤ TDECQ (max)	 0.2 -1.2 + TDECQ	 0.9 -0.5 + TDECQ	 dBm dBm
Transmitter and dispersion eye closure (TDECQ), each lane (max)	TBD[a]	TBD[a]	dB
TECQ (max)	TBD[a]	TBD[a]	dB
|TDECQ - TECQ| (max)	TBD[a]	TBD[a]	dB
Average launch power of OFF transmitter, each lane (max)	-15	-15	dBm
Extinction ratio, each lane, (min)	3.5	3.5	dB
Transmitter transition time (max)	8	8	ps
Transmitter over/under-shoot (max)	22	22	%
$RIN_x OMA$ (max)	-139	-139	dB/Hz
Optical return loss tolerance (max)	21.4 (15.5 for DR1)	21.4 (17.1 for FR1)	dB
Transmitter reflectance (max)	-26	-26	dB

[a] Measured with FFETBD reference equalizer with SER = TBD

Proposed Receiver Specifications

- Mode_FECi (mandatory)

Description	200GBASE-DR1 400GBASE-DR2 800GBASE-DR4 1.6TBASE-DR8	200GBASE-FR1 400GBASE-DR2-2 800GBASE-DR4-2 1.6TBASE-DR8-2	Unit
Signaling rate, each lane (range)	113.4375 ± 50 ppm	113.4375 ± 50 ppm	GBd
Modulation Format	PAM4	PAM4	
Lane wavelengths (range)	1304.5 to 1317.5	1304.5 to 1317.5	nm
Damage threshold, each lane	5	5	dBm
Average receive power, each lane (max)	4	4	dBm
Average receive power, each lane (min)	-5.8	-6.1	dBm
Receive power, each lane (OMA_{outer}) (max)	4.2	4.2	dBm
Receiver reflectance (max)	-26	-26	dB
Receiver sensitivity (OMA_{outer}), each lane (max) for TECQ < 1.4 dB for 1.4 dB ≤ TECQ ≤ SECQ	 -2.9 -4.3 + TECQ	 -3.5 -4.9 + TECQ	 dBm dBm
Stressed receiver sensitivity (OMA_{outer}), each lane (max)	TBD[a]	TBD[a]	dBm
Conditions of stressed receiver sensitivity test:			
SECQ	TBD[a]	TBD[a]	dB
OMA_{outer} of each aggressor lane[b]	4.2	4.2	dBm

[a] Measured with FFETBD reference equalizer with SER = TBD
[b] No aggressors needed for 200GBASE-DR1 or 200GBASE-FR1

Proposed Link Budget

- Mode_FECi (mandatory)

Description	200GBASE-DR1 400GBASE-DR2 800GBASE-DR4 1.6TBASE-DR8	200GBASE-FR1 400GBASE-DR2-2 800GBASE-DR4-2 1.6TBASE-DR8-2	Unit
Power budget (for max TDECQ)	TBD	TBD	dB
Operating distance	500	2000	m
Channel insertion loss	3	4	dB
Maximum discrete reflectance	-35	-35	dB
Allocation for penalties (for max TDECQ)	TBD	TBD	dB
Additional insertion loss allowed	0	0	dB

Proposed Transmitter Specifications

- Mode_FECo (optional)

Description	200GBASE-DR1 400GBASE-DR2 800GBASE-DR4 1.6TBASE-DR8	200GBASE-FR1 400GBASE-DR2-2 800GBASE-DR4-2 1.6TBASE-DR8-2	Unit
Signaling rate, each lane (range)	106.25 ± 50 ppm	106.25 ± 50 ppm	GBd
Modulation Format	PAM4	PAM4	
Lane wavelengths (range)	1304.5 to 1317.5	1304.5 to 1317.5	nm
Side-mode suppression ratio (SMSR), (min)	30	30	dB
Average launch power, each lane (max)	4	4	dBm
Average launch power, each lane (min)	-2.8	-2.1	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane(max)	4.2	4.2	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), each lane(min) for TDECQ < 1.4 dB for 1.4 dB ≤ TDECQ ≤ TDECQ (max)	 0.2 -1.2 + TDECQ	 0.9 -0.5 + TDECQ	 dBm dBm
Transmitter and dispersion eye closure (TDECQ), each lane (max)	3.4[a]	3.4[a]	dB
TECQ (max)	3.4[a]	3.4[a]	dB
|TDECQ - TECQ| (max)	2.5[a]	2.5[a]	dB
Average launch power of OFF transmitter, each lane (max)	-15	-15	dBm
Extinction ratio, each lane, (min)	3.5	3.5	dB
Transmitter transition time (max)	8	8	ps
Transmitter over/under-shoot (max)	22	22	%
RIN_xOMA (max)	-139	-139	dB/Hz
Optical return loss tolerance (max)	21.4 (15.5 for DR1)	21.4 (17.1 for FR1)	dB
Transmitter reflectance (max)	-26	-26	dB

[a] Measured with FFETBD reference equalizer with SER = TBD

Note: As per Option B, this page will not exist in the final 802.3dj draft

Proposed Receiver Specifications

- Mode_FECo (optional)

Description	200GBASE-DR1 400GBASE-DR2 800GBASE-DR4 1.6TBASE-DR8	200GBASE-FR1 400GBASE-DR2-2 800GBASE-DR4-2 1.6TBASE-DR8-2	Unit
Signaling rate, each lane (range)	106.25 ± 50 ppm	106.25 ± 50 ppm	GBd
Modulation Format	PAM4	PAM4	
Lane wavelengths (range)	1304.5 to 1317.5	1304.5 to 1317.5	nm
Damage threshold, each lane	5	5	dBm
Average receive power, each lane (max)	4	4	dBm
Average receive power, each lane (min)	-5.8	-6.1	dBm
Receive power, each lane (OMA_{outer}) (max)	4.2	4.2	dBm
Receiver reflectance (max)	-26	-26	dB
Receiver sensitivity (OMA_{outer}), each lane (max) for TECQ < 1.4 dB for 1.4 dB ≤ TECQ ≤ SECQ	 -2.9 -4.3 + TECQ	 -3.5 -4.9 + TECQ	 dBm dBm
Stressed receiver sensitivity (OMA_{outer}), each lane (max)	-0.9[a]	-1.5[a]	dBm
Conditions of stressed receiver sensitivity test:			
SECQ	3.4[a]	3.4[a]	dB
OMA_{outer} of each aggressor lane[b]	4.2	4.2	dBm

[a] Measured with FFETBD reference equalizer with SER = 4.8e-4
[b] No aggressors needed for 200GBASE-DR1 or 200GBASE-FR1

Note: As per Option B, this page will not exist in the final 802.3dj draft

Proposed Link Budget

- Mode_FECo (optional)

Description	200GBASE-DR1 400GBASE-DR2 800GBASE-DR4 1.6TBASE-DR8	200GBASE-FR1 400GBASE-DR2-2 800GBASE-DR4-2 1.6TBASE-DR8-2	Unit
Power budget (for max TDECQ)	6.5	7.8	dB
Operating distance	500	2000	m
Channel insertion loss	3	4	dB
Maximum discrete reflectance	-35	-35	dB
Allocation for penalties (for max TDECQ)	3.5	3.8	dB
Additional insertion loss allowed	0	0	dB

Note: As per Option B, this page will not exist in the final 802.3dj draft

Recommendation

- A mandatory Mode_FECi and an optional Mode_FECo are defined for the PMD.
- Logic layer requires implementation of both Mode_FECi mode and Mode_FECo mode.
- This approach meets the desire to support an option for low latency applications, via Mode_FECo
- However, the vast majority of end users would be expected to use Mode_FECi
- FECo PMD specification table may be included in the 803.3dj draft or left to the end-user to engineer.
- Shared technology base amongst end users and industries

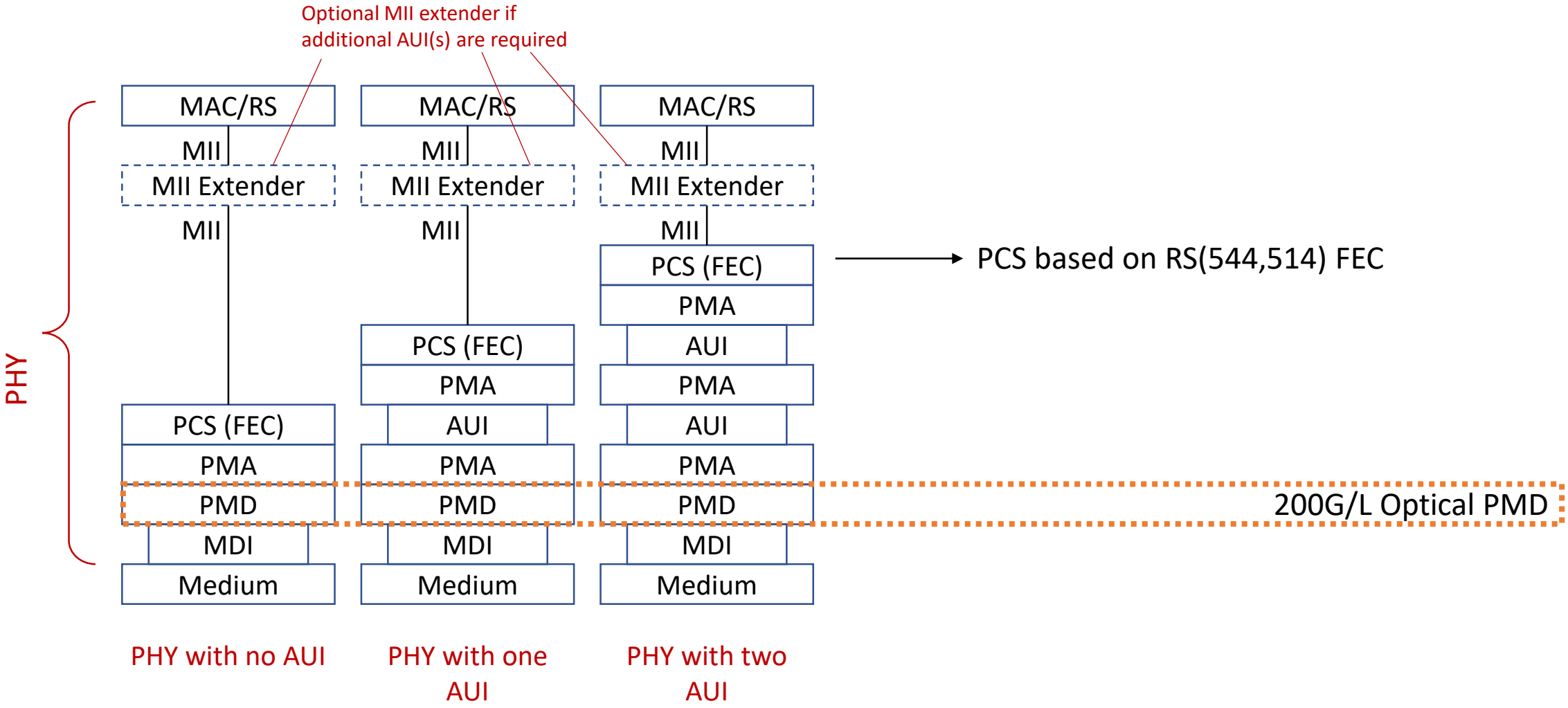
Comments

- This recommendation covers module-based application. Link budgets are based on a link to module BER as per defined by the electrical ad hoc.
- A broader look and contribution are needed to address CPO applications. CPO impacts on all aspects of 802.3dj, including Logic, Electrical and Optical ad hocs.
- This recommendation does not preclude PMD objectives that target CPO applications, for example at shorter reaches than 500 m. Such PMDs might operate exclusively in Mode_FECo.
- The recommendation applies only to single-wavelength PMDs. In particular, 800GBASE-FR4 is excluded and is expected to be supported only by use of the Hamming(128, 120) inner code.

Thank You

& Backup

Location in Ethernet Stack: Mode_FECo



Location in Ethernet Stack: Mode_FECi