CommentID	CommenterName	CommenterCo	Clause	Subclause	Page	Line	CommentType	Comment	SuggestedRemedy	Topic
221	Pandey, Sujan	Velinktech	FM	FM	3	4	ER	automotive Ethernet, 100M+2.5GMBASE-T1	automotive Ethernet, 100M+2.5GBASE-T1	EZ
222	Pandey, Sujan	Velinktech	FM	FM	3	7	ER	2.5G+100MBASE-V1, 100M+5GMBASE-V1	2.5G+100MBASE-V1, 100M+5GBASE-V1	EZ
155	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	1	1.4	31	19	E	The terms to be defined should be in bold, including the colon.	Format terms to be defined at each header in bold.	EZ
152	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	1	1.4.88	31	21	T	Definition for XGMII could be read as implying all 3 rates.	Change "with these rates" to "with one of these rates"	EZ
153	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	1	1.4.248	31	24	E	Definition for coaxial cable is OK as is.	No change to text, delete 1.4.248 from the draft	EZ
154	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	1	1.4.249	31	27	T	Definition for coaxial cable interface unnecessarily states that te medium is shared. It applies as well to point to point, unshared medium. I have reviewed all the existing uses, and they are specific to clause 11 and should be uneffected by the change.	Insert editing instruction to "Change 1.4.249 as shown:" Mark "shared" in strikeout, showing deletion.	EZ
156	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	1	1.4.250	31	31	T	it is unlikely we will use the definition of coaxial cable section, as it is a subset of the link segment. Furhter, the definition, as is, is quite specific with regards to connectors, and the use in clause 10…	Delete 1.4.250 from the draft.	EZ
157	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	1	1.4.251	31	35	T	The term coaxial cable segment is specific to a shared medium segment with terminators on each end (separate from the MDIs). It is unlikely we will have use for it, and if we do, we would need a different definition - so better to have a new term.	Delete 1.4.251 from the draft	EZ
158	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	30	30.3.2.1.2	32	14	T	This is the first place that the draft needs to address the question of do we have one PHY or two, and how they might be differentiated. Suggest we draft text for each proposal in 30.3.2. Note this will eventually need to be done in 30.5., but isn't quite as complicated.	Add Editor's note to 30.3.2.1.2: "Editor's Note (to be removed prior to initial Working Group Ballot): 802.3dm will either define one PHY type or will differentiate clauses 201 and 202 to meet distinct identity. Both PHY type options are shown here. When a choice is made, this section needs to be updated." Duplicate each reference to "Clause 200..." to read "Clause 201 ... 100 Mb/s DME ...ACT" or "Clause 202 ... 100 Mb/s PAM 2... TDD" in 30.3.2 subsections (the 6 pairs on page 32).	Duplexing Method
1	Lasry, Ariel	Qualcomm Technologies Inc.	30	30.5.1.1.2	33	22	E	Typo "/" used instead of "+"	replace "5G/100M" with "5G+100M"	EZ
2	Lasry, Ariel	Qualcomm Technologies Inc.	30	30.5.1.1.2	33	24	E	Typo "/" used instead of "+"	replace "5G/100M" with "5G+100M"	EZ
3	Lasry, Ariel	Qualcomm Technologies Inc.	30	30.5.1.1.2	33	31	E	Typo "/" used instead of "+"	replace "10G/100M" with "10G+100M"	EZ
159	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	30	30.6.1.1.5	33	33	T	Clause 202 does not appear to use auto-negotiation (clause 98 or otherwise), and hence the Auto-Negotiation attributes are specific to clause 201.	Change "as specified in Clause 200" to "as specified in Clause 201" at Page 33, lines 48 through 52, Page 34 Lines 5 through 8, and Page 34 Lines 15 through 18 (3 sets of 4 instances each)	ACT Autonegotiation
4	Lasry, Ariel	Qualcomm Technologies Inc.	30	30.5.1.1.2	33	33	E	Typo "/" used instead of "+"	replace "10G/100M" with "10G+100M"	EZ

166	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	45	45.2.1.7.4	35	28	E	Editing instruction appears to be in italics as header… (font is sans & too large)	Reformat instructions at P35 L28, P35 L50 using "Editing Instruction" type.	EZ
160	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	45	45.2.1.7.4	35	37	T	Clause 202 does not appear to specify use of transmit/ receive fault. Therefore these TBDs can be assigned to clause 201. (if clause 202 adds transmit/receive fault, suggest adding both the clause 201 references here, as well as the clause 202 references - that way we will have them)	Change TBD at page 35, line 35 to an external cross reference to 149.4.2.2 Change TBD at page 35, line 41 to 201.6.2.2 Change TBD at page 36, line 6 to 201.6.2.3 Change TBD at page 36, line 10 to an external cross reference to 149.4.2.3	EZ
5	Lasry, Ariel	Qualcomm Technologies Inc.	45	45.2.1.7.4	35	41	E	Typo "M" in "2.5GMBASE-T1" is too much	replace "2.5GMBASE-T1" with "2.5GBASE-T1"	EZ
223	Pandey, Sujan	Velinktech	45	45.2.1.7.4	35	41	ER	100M+2.5GMBASE-T1, ...	100M+2.5GBASE-T1, ...	EZ
6	Lasry, Ariel	Qualcomm Technologies Inc.	45	45.2.1.7.4	35	43	E	Typo "M" in "5GMBASE-V1" is too much	replace "5GMBASE-V1" with "5GBASE-V1"	EZ
224	Pandey, Sujan	Velinktech	45	45.2.1.7.4	35	43	ER	100M+5GMBASE-T1, ...	100M+5GBASE-T1, ...	EZ
7	Lasry, Ariel	Qualcomm Technologies Inc.	45	45.2.1.7.5	36	10	E	Typo "M" in "2.5GMBASE-T1" is too much	replace "2.5GMBASE-T1" with "2.5GBASE-T1"	EZ
225	Pandey, Sujan	Velinktech	45	45.2.1.7.5	36	10	ER	2.5GMBASE-T1	2.5GBASE-T1	EZ
226	Pandey, Sujan	Velinktech	45	45.2.1.7.5	36	12	ER	2.5GMBASE-T1	2.5GBASE-T1	EZ
8	Lasry, Ariel	Qualcomm Technologies Inc.	45	45.2.1.7.5	36	12	E	Typo "M" in "5GMBASE-V1" is too much	replace "5GMBASE-V1" with "5GBASE-V1"	EZ
9	Lasry, Ariel	Qualcomm Technologies Inc.	45	45.2.1.60f.1	37	24	E	Typo only "PMA type" is mentionned, where this applies also to PMD. This is different than the style used in 45.2.1.32.1 to 45.2.1.33.6 Similar issue is also on lines 27, 32, 35, 40, 43, 48, 51. And on page 38 lines: 4, 7, 12, 16, 20, 23, 28, 31, 36, 39, 44, 47, 52. And on Page 39 lines: 2, 7, 10	replace "PMA type" with "PMA/PMD type"	EZ
10	Lasry, Ariel	Qualcomm Technologies Inc.	45	45.2.1.60f.2	37	29	E	Typo in sub-section title. It cannot be both T1 and V1.	replace "100M+10GBASE-T1/V1" with "100M+10GBASE-V1"	EZ
11	Lasry, Ariel	Qualcomm Technologies Inc.	45	45.2.1.214	40	7	E	Title of Table includes only BASE-T1 type, while content also include BASE-V1 type	Replace "T1" with "T1/V1"	EZ

12	Lasry, Ariel	Qualcomm Technologies Inc.	45	45.2.1.214.2	40	39	E	Not only the first sentence need to change. Since there is one more bit added the whole description of 45.2.1.214.2 needs to be updated with more bits and include the corresponding text for the newely defined modes.	are set to 00000, the mode of operation is 100BASE-T1. When these bits are set to 00001, the mode of operation is 1000BASE-T1. When these bits are set to 00010, the mode of operation is 10BASE-T1L. When these bits are set to 00011, the mode of operation is 10BASE-T1S. When these bits are set to 00100, the mode of operation is 2.5GBASE-T1. When these bits are set to 00101, the mode of operation is 5GBASE-T1. When these bits are set to 00110, the mode of operation is 10GBASE-T1. When these bits are set to 00111, the mode of operation is 25GBASE-T1. When these bits are set to 01000, the mode of operation is 10BASE-T1M. When these bits are set to 10000, the mode of operation is 100M+2.5GBASE-T1. When these bits are set to 10001, the mode of operation is 2.5G+100MBASE-T1. When these bits are set to 10010, the mode of operation is 100M+2.5GBASE-V1. When these bits are set to 10011, the mode of operation is 2.5G+100MBASE-V1. When these bits are set to 10100, the mode of operation is 100M+5GBASE-T1. When these bits are set to 10101, the mode of operation is 5G+100MBASE-T1. When these bits are set to 10110, the mode of operation is	EZ
167	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	46	46.1	41	19	T	Inserted language could be interpreted to mean that the asymmetric phys have 'all of these rates' in one direction. Note that the same change is not needed in 46.1.3, where a diferent change is needed.	Change "with these rates in one direction" to "with at least one of these rates in one direction" at P41 L19, P41 L34.	EZ
13	Lasry, Ariel	Qualcomm Technologies Inc.	46	46.1.2	41	34	E	The text gives the "BASE" name of the PHYs only for the symmetric PHYs and not for the Asymmetric PHYs.	replace: "2.5GBASE, 5GBASE, and 10GBASE PHY types (including asymmetric PHYs with these rates in one direction and 100 Mb/s in the reverse direction)" with: "2.5GBASE, 100M+2.5GBASE, 2.5G+100MBASE, 5GBASE, 100M+5GBASE, 5G+100MBASE, 10GBASE, 100M+10GBASE and 10G+100MBASE PHY types"	Asymmetric

168	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	46	46.1.3	41	41	T	The text here isn't speaking about PHY types but rather about MAC data rates, so the added text doesn't make sense as written.	At P41 L41, delete "(including asymmetric PHYs with these rates in one direction and 100 Mb/s in the reverse direction)" inserted text, and implement the change (with marks inserted - sorry , it just became a mess...) to read: The XGMII supports MAC data rates of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s as defined within this clause. A compliant device may implement any subset of these rates in at least one direction. Symmetric operation at 10 Mb/s and 100 Mb/s is supported by the MII defined in Clause 22 and operation at 1000 Mb/s by the GMII defined in Clause 35. Asymmetric operation is supported at 100 Mb/s in one direction when at least one of specified multigigabit rates is used in the other direction.	Asymmetric
62	Kleinwaechter, Mathias	in-tech	46	46.3.2.1	42	18	E	The sentence could be improved stilistically.	The frequency of RX_CLK may be derived from the received data or it may correspond to a nominal clock (e.g., TX_CLK).	EZ
102	Wienckowski, Natalie	IVN Solutions LLC	46	46.6.1	42	27	E	delete as it is not needed	Delete: 46.6.1 Introduction	EZ
103	Wienckowski, Natalie	IVN Solutions LLC	46	46.6.2	42	29	E	delete as it is not needed	Delete: 46.6.2 Identification	EZ
169	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	46	46.6.3.1	42	34	T	A new option is needed for asymmetric PHYs, the existing text that was edited relates to MAC data rates, not PHYs, and hence isn't quite right..	the draft Insert new row at end of table (unchanged rows not shown): Item: ASYM Feature: Support of Asymmetric Multigigabit PHYs Subclause 46.1.2 Value/comment: (blank) Status: O Support: Yes[] No[] In 46.6.3.1: Add editing instruction: Change PICs items G1, G2, and G3, and insert new row G3a after row G3, as shown (unchanged rows not shown): Add table showing addition of "in at least one direction" to Value/Comment for G1, G2, and G3. (general row format is: Item: Gn Feature: PHY support of x Gb/s MAC data rate Subclause: 46.1.3 Value/Comment: Support of MAC data rate of x Gb/s /UL in at least one direction /UL Status: PHY: O.1 Support: Yes [] N/A [] Insert new row after row for G3 in 46.6.3.1:	Asymmetric

187	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	98	98	43	50	E	Big Ticket Items - PHY relationships & Auto-Neg. If we intend to have multiple PHY types, we need a method to select between them. That means a separate sublayer above the PMA/PCS. Clause 201 uses Clause 98 auto-neg (at least partly). Even if we don't use auto-neg, but have fixed selections, we still need control from that external sub-layer and a way to select. It is reasonable that they should be able to auto-negotiate and we could solve some of the problems and enable wider Ethernet compatibility by bringing clause 98 into the text. Clause 98 is mentioned in clause 201, and there is some work needed to bring a new PHY type into it. If we take another approach work similar to creating an auto-neg sublayer/protocol with priority resolution and ability to select between PHY types in other clauses is needed.	Bring clause 98 into the draft. Add editor's note (to be removed prior to Working Group Ballot): Contributor's to consider whether autonegotiation should be extended to include V1 PHYs. At the moment it only applies to T1 PHYs. Bring 98.5.1 State diagram variables into the draft, add variables: 2.5Gig+100MT1 represents that 2.5G+100MBASE PMA is the signal source 5Gig+100MT1 represents that 5G+100MBASE PMA is the signal source 10Gig+100MT1 represents that 10G+100MBASE PMA is the signal source Bring 98B in the draft, with the following Editor's Note: (to be removed prior to Working Group ballot): Contributions encouraged to resolve priority resolution for MultiGig+100MBASE-T1 PHYs.	ACT Autonegotiation
189	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	104	104	43	52	T	Big Ticket Items - Powering If we want to support clause 104 powering, this is where it would go. Clause 104 will require mention of the new PHY type. It may also be worth considering using clause 189's powering protocol rather than clause 104. Additionally, we need to consider how far we want to go in specifying PoC	Insert clause 104 (104.1.3) into the draft, including Table 104-a from IEEE P802.3dg D2.3, with eidtiing instruction: "Change Table 104-a (inserted by IEEE Std 802.3dg-202x) as follows (unchanged rows not shown) Show row for Type F PSE/PD, and add 2.5G+100MBASE-T1, 5G+100MBASE-T1, 10G+100MBASE-T1, and the 100M+xG... counterparts to the Compatible PHYs column. Add Editor's Note (to be removed prior to Working Group Ballot): Need to consider whether power detection and classification is desired for Power over Coax, and whether to extend clause 104 (or 189) to support PoC.	Power
14	Lasry, Ariel	Qualcomm Technologies Inc.	200	200	44	5	E	Typo "100M+2.5GMBASE-T1" 1 "M" too much after the "G"	replace "100M+2.5GMBASE-T1" with: 100M+2.5GBASE-T1"	EZ
295	Razavi, Alireza	Infineon	200	200	44	9	E	mis-spelling (extra M after G) : "5GMBASE" should be replaced by 5GBASE	see comment	EZ
15	Lasry, Ariel	Qualcomm Technologies Inc.	200	200	44	9	E	Typo "100M+5GMBASE-V1" 1 "M" too much after the "G"	replace "100M+5GMBASE-V1" with "100M+5GBASE-V1"	EZ
64	Kleinwaechter, Mathias	in-tech	200	200	44	9	ER	typo	100M+5GBASE-V1	EZ
104	Wienckowski, Natalie	IVN Solutions LLC	200	200.1.1	44	34	T	missing text	Change: PHY_S HS_TX to PHY_D To: PHY_S HS_TX to PHY_D HS_RX Make the same change in 201.1.1 and 202.1.1	EZ

105	Wienckowski, Natalie	IVN Solutions LLC	200	200.1.2	45	16	E	The PHY/PMD types should be part of the Nomenclature subclause.	Delete: 200.1.2 PHY/PMD types Change italicized text to: The following table depicts the characterisitics of each of the 12 PHY types, x+y depicts the transmit and recieve speeds, where x is the transmit speed and y is the receive speed T1 - single shielded balanced pair of conductors (SBP) V1 - single coaxial cable (Coax) Delete all italicized text below the table. Make the same change in 201.1.2 and 202.1.2.	EZ
171	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	200	200.1.2	45	25	T	We don't specify the cable type, but we do specify the transmission medium. Further, "SBP" isn't a defined abbreviation, neither is Coax". It also doesn't make sense to define them - the PHY doesn't care whether the medium is constructed coaxially, with or without a shield. It cares about the fact that the medium is differential or unbalanced. these PHYs could be used on balanced or unbalanced board traces as well. Same comment applies to Table 201-2 and 202-2.	Change "Cable Type" to "Medium" at P45 L26 (Table 200-2), P73 L41 (Table 201-2), and P144 L43, (Table 202-2) In all relevant entries for Table 200-2, 201-2, and 202-2, Change "SBP" to "100 Ohm Balanced differential pair" and Change "Coax" to "Unbalanced medium"	EZ
16	Lasry, Ariel	Qualcomm Technologies Inc.	200	200.1.2	45	40	E	Typo "100M+5GMBASE-V1" 1 "M" too much after the "G"	replace "100M+5GMBASE-V1" with "100M+5GBASE-V1"	EZ
170	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	200	200.1.2	45	47	E	The note (italicized text) after Table 200-1 is already in the draft in 200.1.1	Delete P45 L46 through P46 L2	EZ
17	Lasry, Ariel	Qualcomm Technologies Inc.	200	200.1.2	45	48	E	Lines 48 to 54 and Line 1 of page 46 are duplicates of lines 1-12	remove Lines 48 to 54 and Line 1 of page 46	EZ
172	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	200	200.1.4.1	46	14	E	It seems that some edits to the draft from the new nomenclature remain in the clean copy.	Delete struck-out Red text, (and "1" on P46 29), and remove underline and green color to new text on P46, 47, 51, 52, 55, 58. 60	EZ
18	Lasry, Ariel	Qualcomm Technologies Inc.	200	200.1.4.4	46	30	E	Typo: "1" at the end of the line is too much	replace "(LS_PATH)1" with "(LS_PATH)"	EZ
19	Lasry, Ariel	Qualcomm Technologies Inc.	200	200.1.5	46	44	E	Typo	replace "pathS_PATH)" with "path (HS_PATH)"	EZ
106	Wienckowski, Natalie	IVN Solutions LLC	200	200.1.5	46	44	E	typo	change: high speed pathS_PATH) To: high speed path (HS_PATH)	EZ
63	Kleinwaechter, Mathias	in-tech	200	200.13.2.1	49	17	ER	The sentence has a grammatical issue. "characteristic is impedance" -> the "is" must be deleted.	For balanced cabling, a nominal differential characteristic impedance of 100 ? is used, and for coaxial cabling a nominal characteristic impedance of 50 ? is used.	EZ
65	Kleinwaechter, Mathias	in-tech	200	200.17	52	3	ER	typo	100M+.25GBASE-V1	EZ
66	Kleinwaechter, Mathias	in-tech	200	200.17	52	5	ER	typo	100M+5GBASE-V1	EZ
67	Kleinwaechter, Mathias	in-tech	200	200.17.2.2	53	25	ER	typo	100M+.25GBASE-V1	EZ
68	Kleinwaechter, Mathias	in-tech	200	200.17.2.2	53	28	ER	typo	100M+5GBASE-V1	EZ

69	Kleinwaechter, Mathias	in-tech	200	200.17.3	53	53	ER	typo	100M+.25GBASE-V1	EZ
70	Kleinwaechter, Mathias	in-tech	200	200.17.3	54	1	ER	typo	100M+5GBASE-V1	EZ
328	Johnson, Samuel	Infineon	200	200.4.2.2.17	54	38	T	Mapping of logic0 -> +1 and logic1 -> -1 seems non-intuitive	If this is used by PAM2 in other standards, then leave unchanged. Otherwide, propose Logic0 -> -1 Logic1 -> +1	EZ
20	Lasry, Ariel	Qualcomm Technologies Inc.	200	200.5.1	55	50	E	I assume "MII" is editorial typo, as the group agreed to use XGMII for both directions	replace "MII" with "XGMII"	EZ
165	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	200	200.11	64	15	E	The term link segment used in clauses 200, 201, and 202 either refers to balanced pairs or to an unbalanced coax link segment. The section should say "used in this subclause", or, better yet, just delete the sentence - it adds little value.	Delete the sentence "The term link segment used in this clause…" from the first paragraph of 200.11, 200.12, 201.11, 201.12, 202.7, and 202.8.	EZ
227	Pandey, Sujan	Velinktech	200	200.11.1	64	21	ER	Parameters The transmission ...	The transmission ...	EZ
173	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	200	200.11.1	64	21	E	There is an extra word hanging at the front of the sentence.	Delete "Parameters "	EZ
174	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	200	200.12.2	65	44	E	The notion of crosstalk is independent of the medium type, and will generally come at ganged connector interfaces even on shielded media. The titles appear to be appropriate for coax as well as differential paired media.	Delete note at P65 L44	EZ
164	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	200	200.13.	66	1	T	Clauses 201 & 202 each have this same form, but different approaches to the upper frequency. If we have one PHY or the other, we can just copy from that clause. If we have 2 PHYs they will have different specifications for this. Suggest there is no value having this specification in clause 200.	Delete 200.13 content (and subclause) in its entirety. (leave placeholder)	EZ
228	Pandey, Sujan	Velinktech	200	200.13.2.1	66	15	ER	The differential impedence at the MDI for each transmit/receiver channel ...	The differential impedence at the MDI for each transmit/receive channel ...	EZ
175	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	200	200.13.2.1	66	18	T	It isn't reasonable to include coaxial cabling in a section where you are talking about the T1 interface (even though later the coax sectioin references this). Technically, the interface to the medium in a coax, unbalanced case will be different than it is for a differential balanced case - in addition to the simple fact that the return loss is a 50 ohm impedance for coax, and needs to be specified separately. Separating the two will force the task force to discuss the technical principles.	Change the second sentence of 200.13.2.1 to "For the -T1 PMD, a nominal differential characteristic is impedance of 100 O is used." Copy 200.13.2.1 to 200.14.2.1 (including the plot), replacing "The MDI return loss for coax cables is as specified in 200.13.2.1.", changing "T1" to "V1" in the 2nd and third paragraphs, and changing the second sentence of the first paragraph to "For the -V1 PMD, a nominal characteristic impedance of 50 O is used."	EZ
161	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	200	200.13.2.1	66	35	E	The Note regarding Fmax should be an editor's note. I note that clauses 201 and 202 each have this same equation, and 201 scales with Fmax, but 202 does not - suggesting there is no agreement on this point	replace "Note… established." at line 35 with "Editor's Note (to be removed prior to Working Group Ballot): Commenters to consider what Fmax should be, and whether it should scale. See clauses 201 and 202 for differences."	EZ
21	Lasry, Ariel	Qualcomm Technologies Inc.	200	200.17	69	3	E	Typo "100M+2.5GMBASE-T1" 1 "M" too much after the "G"	replace "100M+2.5GMBASE-T1" with: 100M+2.5GBASE-T1"	EZ

22	Lasry, Ariel	Qualcomm Technologies Inc.	200	200.17	69	5	E	Typo "100M+5GMBASE-V1" 1 "M" too much after the "G"	replace "100M+5GMBASE-V1" with "100M+5GBASE-V1"	EZ
23	Lasry, Ariel	Qualcomm Technologies Inc.	200	200.17.1	69	13	E	Typo "100M+2.5GMBASE-T1" 1 "M" too much after the "G"	replace "100M+2.5GMBASE-T1" with: 100M+2.5GBASE-T1"	EZ
24	Lasry, Ariel	Qualcomm Technologies Inc.	200	200.17.1	69	15	E	Typo "100M+5GMBASE-V1" 1 "M" too much after the "G"	replace "100M+5GMBASE-V1" with "100M+5GBASE-V1"	EZ
25	Lasry, Ariel	Qualcomm Technologies Inc.	200	200.17.2.2	70	25	E	Typo "100M+2.5GMBASE-T1" 1 "M" too much after the "G"	replace "100M+2.5GMBASE-T1" with: 100M+2.5GBASE-T1"	EZ
26	Lasry, Ariel	Qualcomm Technologies Inc.	200	200.17.2.2	70	28	E	Typo "100M+5GMBASE-V1" 1 "M" too much after the "G"	replace "100M+5GMBASE-V1" with "100M+5GBASE-V1"	EZ
27	Lasry, Ariel	Qualcomm Technologies Inc.	200	200.17.4	70	53	E	Typo "100M+2.5GMBASE-T1" 1 "M" too much after the "G"	replace "100M+2.5GMBASE-T1" with: 100M+2.5GBASE-T1"	EZ
28	Lasry, Ariel	Qualcomm Technologies Inc.	200	200.17.4	71	1	E	Typo "100M+5GMBASE-V1" 1 "M" too much after the "G"	replace "100M+5GMBASE-V1" with "100M+5GBASE-V1"	EZ
29	Lasry, Ariel	Qualcomm Technologies Inc.	201	201	72	3	E	Typo "100M+2.5GMBASE-T1" 1 "M" too much after the "G"	replace "100M+2.5GMBASE-T1" with: 100M+2.5GBASE-T1"	EZ
30	Lasry, Ariel	Qualcomm Technologies Inc.	201	201	72	6	E	Typo "100M+5GMBASE-V1" 1 "M" too much after the "G"	replace "100M+5GMBASE-V1" with "100M+5GBASE-V1"	EZ
229	Pandey, Sujan	Velinktech	201	201.1.1	72	39	ER	speed, where x+y indicates the PHY transmits at “x” speed at receives at “y” speed	speed, where x+y indicates the PHY transmits at “x” speed and receives at “y” speed	EZ
298	Razavi, Alireza	Infineon	201	201.1.1	72	39	E	"at receives at y speed" should be replaced by " and recieves at y speed"; grammatical error.	see comment	EZ
299	Razavi, Alireza	Infineon	201	201.1.1	72	42	E	HS_RX' is missing after 'PHY_D'	see comment	EZ
297	Razavi, Alireza	Infineon	201	201.1.1	72	48	E	PHY_D and PHY_S notations are not self-descriptive.	PHY_D is replaced by LSHS, and PHY_S is replaced by HSLS	ACT Nomenclature
176	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	201	201.1.1	73	12	T	inappropriate use of "shall" - requirement on the reader.	Change the second sentence of the paragraph starting on line 11 (Additionally…) to "When incorporating Clause 149 requirements which use the scaling factor "S" by reference, refer to Table 201-1 rather than Table 149-1."	EZ
182	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	201	201.1.4	74	22	T	The requirement that optional autoneg shall meet clause 98 is missing - but autoneg is included elsewhere in clause 201. In clause 149 it went in this section.	Add text to 201.1.4: Auto-Negotiation (Clause 98) may optionally be used by MultiG+100M/100M+MultiGBASE-T1/V1 devices to detect the abilities (modes of operation) supported by the device at the other end of a link segment, determine common abilities, and configure for normal operation. Auto-Negotiation is performed upon link startup through the use of half-duplex differential Manchester encoding. The implementation of the Auto-Negotiation function is optional. If Auto-Negotiation is implemented, it shall meet the requirements of Clause 98.	ACT Autonegotiation

183	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	201	201.1.4	74	23	T	The description of leader/follower negotiation formerly went here.	Add the following text (after the autoneg text if the previous comment is implemented): A MultiG+100M/100M+MultiGBASE-T1/V1 PHY shall be capable of operating as LEADER or FOLLOWER, per runtime configuration. A LEADER PHY uses a local clock to determine the timing of transmitter operations. A FOLLOWER PHY recovers the clock from the received signal and uses it to determine the timing of transmitter operations. When Auto-Negotiation is used, the LEADER-FOLLOWER relationship between two devices sharing a link segment is established during Auto-Negotiation (see Clause 98). If Auto-Negotiation is not used, a LEADER-FOLLOWER relationship shall be established by management or hardware configuration of the PHYs, and the LEADER and FOLLOWER are synchronized by the PHY Link Synchronization function in the PHY (see 201.7.3). NOTE—Annex K describes that the optional alternative terminology "leader" "follower" was formerly known as “master” and “slave”.	ACT Autonegotiation
300	Razavi, Alireza	Infineon	201	201.1.4	75	7	E	From figure 201-1, tx_lpi_active to be remobed as EEE is not defined yet	see comment	ACT EEE
207	Abedinzadeh, Bizhan	Infineon	201	201.1.4	75	7	E	Quiet-refresh signaling is not needed for non-echo-cancelled PHYs	delete tx_lpi_active signal from Figure 201-1	ACT EEE
343	Jonsson, Ragnar	Infineon	201	201.1.4	75	32	T	Missing LSS Tx path	Add LSS Tx Path	PHY_S
31	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.1.4	75	49	E	Typo missing "HS_TX" before "PMA TRANSMIT"	add "HS_TX " before "PMA TRANSMIT"	EZ
177	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	201	201.1.4	75	49	E	typo. "received clock signal back the PMA TRANSMIT" - same typo on NOTE 1 on Figure 201-1 and 201-2 (note - these are also clause 149 errors)	Change "back" to "by" in NOTE 1 on Figures 201-1 and 201-2.	EZ
179	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	201	201.1.4	75	50	T	NOTE 2 is incorrect and misleading. There are no functions shown with dashed lines, and the signals are required if EEE is provided - they aren't optional in and of themselves. (note - these are also clause 149 errors)	Change NOTE 2 to read: "rx_lpi_active and alert_detect are only required when optional EEE capability is implemented."	ACT EEE
301	Razavi, Alireza	Infineon	201	201.1.4	76	33	E	From figure 201-2, rx_lpi_active, aleret_detect to be remobed as EEE is not defined yet	see comment	ACT EEE
208	Abedinzadeh, Bizhan	Infineon	201	201.1.4	76	33	E	Quiet-refresh signaling is not needed for non-echo-cancelled PHYs	delete rx_lpi_active and alert_detect signals from Figure 201-2	ACT EEE
344	Jonsson, Ragnar	Infineon	201	201.1.4	76	41	T	Clock recovery is optional for leader	Mark "Clock Recovery" optional	ACT XTAL-less
32	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.1.4	76	49	E	Typo missing "LS_TX" before "PMA TRANSMIT"	add "LS_TX " before "PMA TRANSMIT"	EZ
178	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	201	201.1.4	76	50	T	NOTE 2 is incorrect and misleading. There is only one signal shown with a dashed line, and it is required if EEE is provided - it isn't optional in and of itself. (note - these are also clause 149 errors)	Change NOTE 2 to read: "tx_lpi_active is only required when optional EEE capability is implemented."	ACT EEE

401	Muma, Scott	Microchip	201	201.1.4.1	77	4	T	I would recommend describing the PCS layer from the PHY_D/PHY_S perspective rather than HS_PATH/LS_PATH. The wording in this paragraphs shows how challenging it is to talk about a PCS from a path perspective, but then to say it contains a management interface, and XGMII interface, etc. when this is referring to 2 different interfaces in separate PHY instances.	Describe the PHY_S PCS sublayer which has an XGMII interface, a single management interface, a PMA interface, etc. Describe the data format of the PHY_S Tx referring to 149.3 of the HS_TX as desired. Add any specifics needed for LS_RX.	ACT PCS
191	van Dyck, Peter	Infineon	201	201.1.4.1	77	11	E	Not a proper sentence	The HS_PATH contains the PCS functions as specified in 149.3,…	EZ
33	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.1.4.2	77	16	T	Missing text similar to the first paragraph of 201.1.4.1. Needed to identify the coupling to XGMII also with the other PHYs	Add as first paragraph of 201.1.4.2: "For the low speed path, the LS_TX and LS_RX PCS couples a 10 Gigabit Media Independent Interface (XGMII), as specified in Clause 46, to the 100M+2.5GBASE-T1/V1, 100M+5GBASE-T1/V1, or 100M+10GBASE-T1/V1 Physical Medium Attachment (PMA) sublayer. In addition to the normal mode of operation, the PCS supports a training mode. Furthermore, the PCS contains a management interface. The LS_TX PCS is in the PHY_D and the LS_RX PCS is in the PHY_S."	EZ
402	Muma, Scott	Microchip	201	201.1.4.2	77	17	T	I would recommend describing the PCS layer from the PHY_D/PHY_S perspective rather than HS_PATH/LS_PATH. The wording in this paragraphs shows how challenging it is to talk about a PCS from a path perspective, but then to say it contains a management interface, and XGMII interface, etc. when this is referring to 2 different interfaces in separate PHY instances.	Describe the PHY_D PCS sublayer which has an XGMII interface, a single management interface, a PMA interface, etc. Describe the data format of the PHY_D Tx as the LS_TX and add any specifics needed for HS_RX.	ACT PCS
108	Wang, Frank	Realtek Semiconductor Corp.	201	201.1.4.2	77	18	E	grammar	change "TXD<31:0>, TXC<3:0>" to "TXD<31:0> and TXC<3:0>"	EZ
109	Wang, Frank	Realtek Semiconductor Corp.	201	201.1.4.2	77	23	E	typo	change "Reserved" to "reserved"	EZ
72	Maguire, Valerie	Copperopolis; aff'l w/ CME Consulting, Microchip, and NXP	201	201.1.4.2	77	24	E	There are two different ways that RS-FEC encoding is referenced throughout the draft, parent document, and related published amendments. I believe the encoding should be structured as RS-FEC(x,y,z) - witth no space between 'FEC' and '('. Editor may additionally wish to consider submitting a Maintenance Request to harmonize usage across all documents.	Grant Editorial license to replace occurrences of RS-FEC (x,y,etc.) with RS-FEC(x,y,etc.) throughout the draft.	EZ
302	Razavi, Alireza	Infineon	201	201.1.4.2	77	25	E	word Finally should be removed	see comment	EZ
110	Wang, Frank	Realtek Semiconductor Corp.	201	201.1.4.2	77	26	E	wording	change "low data rate direction" to "low speed path" or "LS_PATH"	EZ
34	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.1.4.2	77	27	E	wrong cross reference. Low data rate PCS transmit functions are described in 201.4.2.2	replace cross reference to "201.2.2.2" with a cross reference to "201.4.2.2"	EZ
345	Jonsson, Ragnar	Infineon	201	201.1.4.2	77	39	T	EEE should be removed	Remove all reference to EEE	ACT EEE

192	van Dyck, Peter	Infineon	201	201.1.4.2	77	39	E	Wrong reference: (see 201.3.5.2)	(see 201.4.5)	EZ
276	Razavi, Alireza	Infineon	201	201.1.4.2	77	40	E	remove EEE, as it is not defined		ACT EEE
193	van Dyck, Peter	Infineon	201	201.1.4.2	77	40	T	"such as EEE and OAM" EEE should be removed	Replace with "such as OAM"	ACT EEE
111	Wang, Frank	Realtek Semiconductor Corp.	201	201.1.4.3	77	48	E	wording: insert "shielded" between "single" and "balanced" If this comment is accepted, many places need to be inserted.	change "a single balanced pair of conductors" to "a single shielded balanced pair of conductors"	EZ
403	Muma, Scott	Microchip	201	201.1.4.3	77	52	T	This paragraphs switches from the PMA being a sublayer to being 2 ends of the path. The PMA is a sublayer, so talking about an HS_PATH PMA or LS_PATH PMA makes it challenging to maintain clarity. The following paragraphs on PHY Control switches back to sublayer since the PHY control would control an HS_TX/LS_RX PMA, not an HS_PATH PMA.	Change this paragraph to: The PMA provides full duplex communications at 117.1875 MBd in one direction and 5625 x S MBd in the other direction. See Table 201–1 for the definition of S.	ACT PCS
112	Wang, Frank	Realtek Semiconductor Corp.	201	201.1.4.3	77	52	E	typo: check how many spaces are there between "provides" and "communications"	change "provides communications" to "provides communications"	EZ
113	Wang, Frank	Realtek Semiconductor Corp.	201	201.1.4.3	77	52	E	typo	change "x" to "×"	EZ
346	Jonsson, Ragnar	Infineon	201	201.1.4.3	78	2	E	Autoneg is optional	Clarify that Autoneg is optional, by putting the word "optional" before Autoneg	ACT Autonegotiation
114	Wang, Frank	Realtek Semiconductor Corp.	201	201.1.4.3	78	3	E	wording: When talking about all PHYs, regardless of transmit speed or cable type, use: MultiG+100M/100M+MultiGBASE-T1/V1	change "PHY" to "MultiG+100M/100M+MultiGBASE-T1/V1"	EZ
347	Jonsson, Ragnar	Infineon	201	201.1.4.4	78	18	T	EEE should be removed	Remove all reference to EEE	ACT EEE
348	Jonsson, Ragnar	Infineon	201	201.1.4.5	78	28	E	Link Syncronization is not half-duplex	Remove text about Link Sync beeing half-duplex	ACT Link Sync
349	Jonsson, Ragnar	Infineon	201	201.1.5	78	49	T	EEE should be removed	Remove item "i)" from the list	ACT EEE
194	van Dyck, Peter	Infineon	201	201.1.5	78	50	T	Non echo-cancelled PHY doesn't need quiet-refresh signaling to be energy efficient	Delete item i) (P78 L50)	ACT EEE
277	Razavi, Alireza	Infineon	201	201.1.5	78	51	T	LPI mode is not defined in Clause 201, so PHY has 2 basic modes not 3 basic modes	Remove optional LPI signaling objective, or add full normative definition of LPI operation for these PHYs.	ACT EEE
350	Jonsson, Ragnar	Infineon	201	201.1.5	78	52	T	EEE should be removed	Only two modes and remove LPI reference	ACT EEE
195	van Dyck, Peter	Infineon	201	201.1.5	78	52	T	Non echo-cancelled PHY doesn't need quiet-refresh signaling to be energy efficient	Change "The PHY may operate in three basic modes: the normal data mode, the training mode, or an optional LPI mode." to read "The PHY may operate in two basic modes: the normal data mode or the training mode."	ACT EEE
268	Lo, William	Axonne Inc	201	201.1.6	79	26	T	No need to have a figure and it is going to be difficult and not instructive even with a drawing showing the RS-Frame encoded as DME. The stream of DME symbols will be self evident with a combination of 201.4.2.2.16, Figure 201-16, and the output of the data path in Figure 201-11	Remove (See Figure <REF>)	EZ
278	Razavi, Alireza	Infineon	201	201.1.6	79	26	E	remove this pharase '(See Figure <REF>)'	see comment	EZ
351	Jonsson, Ragnar	Infineon	201	201.1.6	79	26	E	Missing figre	Add figure referenced in this line	EZ
115	Wang, Frank	Realtek Semiconductor Corp.	201	201.2	79	48	E	wording	change "PHY_S and PHY_D" to "MultiG+100M/100M+MultiGBASE-T1/V1"	ACT Nomenclature

116	Wang, Frank	Realtek Semiconductor Corp.	201	201.2	79	50	E	wording	change "PHY_S and PHY_D" to "MultiG+100M/100M+MultiGBASE-T1/V1 transfer"	ACT Nomenclature
35	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.2.1.1.3	80	41	E	Is the PMA Link Monitor function reference to 149.4.2.5 correct? There is a specific Link Monitor function under 201.7.2 which is specific for ACT	change the reference to "201.7.2"	ACT Link Monitor
36	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.2.1.2.1	81	8	E	"US_TX" is not defined.	change to "MultiG+100M/100+MultiGBASE-T1/V1"	ACT Nomenclature
196	van Dyck, Peter	Infineon	201	201.2.1.2.1	81	8	E	"US_TX link is established"	Replace with "PHY link is established"	ACT Nomenclature
117	Wang, Frank	Realtek Semiconductor Corp.	201	201.2.2	81	24	E	wording: these service primitives are not only for LS_PATH	change "The low speed path" to "MultiG+100M/100M+MultiGBASE-T1/V1"	ACT Nomenclature
37	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.2.2	81	41	E	Missing text for optional EEE related primitives which are shown in Figures 201-3 and 201-4. Also visible in Figures 201-1 and 201-2	Copy missing lines from 149.2.2	ACT EEE
352	Jonsson, Ragnar	Infineon	201	201.2.2	82	3	E	PMA_LINK signals are optional	Mark PMA_LINK.request and indication optional	ACT PMA
279	Razavi, Alireza	Infineon	201	201.2.2	82	24	E	From figure 201-3, PMA_PCS_TX_LPI_STATUS_request to be remobed as EEE is not defined yet	see comment	ACT EEE
353	Jonsson, Ragnar	Infineon	201	201.2.2	82	24	T	EEE should be removed	Remove LPI status request signal	ACT EEE
197	van Dyck, Peter	Infineon	201	201.2.2	82		T	Primitive PMA_PCS_TX_LPI STATUS.request is not defined or needed.	Remove PMA_PCS_TX_LPI_STATUS.request from Figure 201-3	ACT EEE
280	Razavi, Alireza	Infineon	201	201.2.2	83	24	E	From figure 201-4, PMA_PCS_RX_LPI_STATUS_request, PMA_ALERTDETECTinduction to be remobed as EEE is not defined yet	see comment	ACT EEE
354	Jonsson, Ragnar	Infineon	201	201.2.2.1.1	83	24	T	EEE should be removed	Remove LPI status and Alert-Detect signals	ACT EEE
198	van Dyck, Peter	Infineon	201	201.2.2	83		T	Primitives PMA_PCS_RX_LPI STATUS.request and PMA_ALERTDETECT are not defined or needed,	Remove PMA_PCS_RX_LPI_STATUS.request and PMA_ALERTDETECT.indication from Figure 201-4	ACT EEE
356	Jonsson, Ragnar	Infineon	201	201.2.2.3	84	26	T	It is optional for PHY-D to be a follower and PHY-S to be a master	See comment	ACT Autonegotiation
118	Wang, Frank	Realtek Semiconductor Corp.	201	201.2.2.2	84	27	T	Since 802.3dm is asymmetric transmission, the use of "and" will restrict optimal PHY design.	change "and" to "or"	ACT Asymmetric
296	Razavi, Alireza	Infineon	201	201.2.2.2	84	29	E	both " LEADER-FOLLOWER" and "LEADER/FOLLOWER" pharases are used.	for consistency, only one of them should be used	EZ
355	Jonsson, Ragnar	Infineon	201	201.2.2.2	84	29	T	Autoneg needs to support selection of PHY-S vs PHY-D	Add Autoneg support for selecting PHY-S vs PHY-D	ACT Autonegotiation
230	Pandey, Sujan	Velinktech	201	201.2.2.2.1	84	43	ER	FOLLOWERThis …	FOLLOWER This	EZ
281	Razavi, Alireza	Infineon	201	201.2.2.1	84	43	E	Missing space in 'FOLLOWERThis value'.	Insert a space: 'FOLLOWER This value'.	EZ
38	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.2.2.2.1	84	43	E	space missing between "FOLLOWER" and "This"	Insert between "FOLLOWER" and "This"	EZ
107	Wienckowski, Natalie	IVN Solutions LLC	201	201.2.2.1	84	43	E		Adjust tab settings so "FOLLOWER" doesn't run in to "This".	EZ
231	Pandey, Sujan	Velinktech	201	201.2.2.3	85	5	ER	for the HS_TX and in201.4.2.2 for ...	for the HS_TX and in 201.4.2.2 for ...	EZ
282	Razavi, Alireza	Infineon	201	201.2.2.3	85	5	E	Missing space in reference 'in201.4.2.2'.	Insert a space: 'in 201.4.2.2'.	EZ
78	Wienckowski, Natalie	IVN Solutions LLC	201	201.2.2.3	85	5	E	missing space	Add space between "in" and "201.4.2.2".	EZ

119	Wang, Frank	Realtek Semiconductor Corp.	201	201.2.2.3	85	5	E	typo	change "in201.4.2.2" to "in 201.4.2.2"	EZ
199	van Dyck, Peter	Infineon	201	201.2.2.3	85	5	E	"in201.4.2.2" space missing	Replace with "in 201.4.2.2"	EZ
120	Wang, Frank	Realtek Semiconductor Corp.	201	201.2.2.3.1	85	16	T	{–1, –1/3, +1/3, +1} is only for the normal operation of 10G mode.	change "{–1, –1/3, +1/3, +1} in normal operation." to the following: {–1, –1/3, +1/3, +1} in normal operation for 10G mode. {-1, +1} in normal operation for 2.5G mode and 5G mode.	EZ
39	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.2.2.3.1	85	17	T	values -1/3 and +1/3 may only be used by 10G+100MBASE-T1/V1 PHY	add after "operation": "for 10G+100MBASE-T1/V1 PHY" Ad a new line with: "{-1, +1} in normal operation for 2.5G+100MBASE-T1/V1 and 5G+100MBASE-T1/V1 PHYs."	EZ
378	Wang, Frank	Realtek Semiconductor Corp.	201	201.2.2.3.1	85	18	E	wording: since there is only one case, I suggest to remove "when zeros are to be transmitted in the following case:"	change: 0 when zeros are to be transmitted in the following case: when PMA_TXMODE.indication is SEND_Z during PMA training. to: 0 when PMA_TXMODE.indication is SEND_Z during PMA training.	EZ
396	Muma, Scott	Microchip	201	201.2.2.3.1	85	23	TR	It's not clear what it means when tx_symb has the value DME. DME should not be in the PCS layer, it should be in the PMA layer as in Clause 147: "the DME encoder/decoder is contained in the PMA (see 147.4)"	tx_symb should be the logic symbol values, and the DME encoder/decoder functions should be removed from the PCS and added to the PMA.	DME
357	Jonsson, Ragnar	Infineon	201	201.2.2.3.1	85	23	E	Not the same clarity for DME signal as PAM2 signal in line 17	Clarify the meaning of DME, by adding a reference to Clause 201.4.2.2.16	EZ
121	Wang, Frank	Realtek Semiconductor Corp.	201	201.2.2.3.1	85	24	E	wording: since there is only one case, I suggest to remove "when zeros are to be transmitted in the following case:"	change: 0 when zeros are to be transmitted in the following case: when PMA_TXMODE.indication is SEND_Z during PMA training. to: 0 when PMA_TXMODE.indication is SEND_Z during PMA training.	EZ
122	Wang, Frank	Realtek Semiconductor Corp.	201	201.2.2.4.1	85	45	E	grammar: comma afrer "During reception"	change "reception" to "reception,"	EZ
40	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.2.2.4.2	85	50	T	It is not only the low speed path PMA that generates PMA_UNITDATA.indication(rx_symb) messages. Also the high speed path.	delete "low speed path"	EZ
250	McCarthy, Frank	Infineon	201	201.2.2.4.2	85	52	E	semicolon should be a comma		EZ
41	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.2.2.4.2	85	52	E	ambiguious use of 2.5G. Other Clauses use the PHY name	replace "2.5G" with "100M+2.5GBASE-T1/V1"	EZ
42	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.2.2.4.2	85	52	E	ambiguious use of 5G. Other Clauses use the PHY name	replace "5G" with "100M+5GBASE-T1/V1"	EZ
43	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.2.2.4.2	85	52	E	ambiguious use of 10G. Other Clauses use the PHY name	replace "10G" with "100M+10GBASE-T1/V1"	EZ
251	McCarthy, Frank	Infineon	201	201.2.2.4.2	85	53	E	semicolon should be a comma		EZ

269	Lo, William	Axonne Inc	201	201.2.2.5.3	86	37	T	The fix here is simple if we add some missing text in another comment. Let's make the simple fix here first	1) Delete Editor's note 2) Change 201.6.2.3 for HS_RX and TBD. To: 201.4.2.3 for LS_RX.	ACT PMA
283	Razavi, Alireza	Infineon	201	201.2.2.5.3	86	37	E	TBD can be removed "The effect of receipt of this primitive is specified in 149.4.2.3 for HS_RX and 201.6.2.3 for HS_RX and TBD."	Replaced by "The effect of receipt of this primitive is specified in 149.4.2.3 for HS_RX and 201.6.2.3 for LS_RX."	ACT PMA
358	Jonsson, Ragnar	Infineon	201	201.2.2.5.3	86	37	T	Reference to wrong clause	Reference Clause 201.5 instead of 149.4.2.3	ACT PMA
359	Jonsson, Ragnar	Infineon	201	201.2.2.5.3	86	37	E	Change second HS_RX tp LS_RX	See comment	ACT PMA
360	Jonsson, Ragnar	Infineon	201	201.2.2.5.3	86	37	E	Remove "and TBD", unless there is specific clause to be referenced	See comment	ACT PMA
200	van Dyck, Peter	Infineon	201	201.2.2.5.3	86	37	E	"201.6.2.3 for HS_RX" wrong RX	Replace with "201.6.2.3 for LS_RX"	ACT PMA
361	Jonsson, Ragnar	Infineon	201	201.2.2.7.3	87	28	E	Remove "TBD", unless there is specific clause to be referenced	See comment	EZ
270	Lo, William	Axonne Inc	201	201.2.2.7.3	87		T	Fix the references.	1) Delete the contents in the entire section including the editor's note 2) Add the following text: The effect of receipt of this primitive is specified in Figure 149–33, 149.4.2.4, 201.3.2.3, 201.4.2.3, and 201.7.2.1.3.	ACT PMA
390	Muma, Scott	Microchip	201	201.3	88	24	T	The PCS is a sublayer within the PHY comprising a transmit and receive, which makes describing it only as HS_PATH functions a challenge in the current text structure.	Describe the functions/structure of a PHY_S PCS in one subclause, including subclauses for the HS_TX and LS_RX. Then in another subclause describe the functions/structure of a PHY_D PCS, including subclauses for the HS_RX and LS_TX. This will be consistent with the layered structure of the document rather than mixing the layer and path within one description.	ACT PCS
44	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.1	88	32	E	lines 32-34 are same as clause 149.3.1	replace lines 32-34 with "PCS service interface is specified as in 149.3.1"	EZ
123	Wang, Frank	Realtek Semiconductor Corp.	201	201.3.1	88	32	E	wording	change "MultiGBASE-T1" to "MultiG+100MBASE-T1/V1"	EZ
252	McCarthy, Frank	Infineon	201	201.3.2	89	20	E	line should not go through pma_data_mode		EZ
362	Jonsson, Ragnar	Infineon	201	201.3.2.2	89	20	E	"pcs_data_mode" is overlapping the line	See comment	EZ
73	Zhu,	Infineon	201	201.3.2	89	20	E	pcs_data_mode text is blocked	adjust text postion	EZ
45	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.2	89	29	E	Figure 201-5 HS_TX PCS TRANSMIT block is missing a dashed output arrow down to PHY_S PMA SERVICE INTERFACE.The dashed arrow is for "tx_lpi_active"	add the arrow	ACT EEE
46	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.2	89	29	E	Figure 201-5 "pcs_data_mode" text is over the arrow	move the text to the right of the arrow	EZ
259	McCarthy, Frank	Infineon	201	201.3.2.2	90	7	E	In fig 201-6, the S_n are from the training frame, and the A_n are from the 2.5G/5G data stream D_n[0]. There should be a note explaining this in the figure.	The S_n are from the training fram, and the A_n are from the 2.5G and 5G HS_PATH when the PAM2 mapper is used.	EZ
284	Razavi, Alireza	Infineon	201	201.3.2.2	91	1	E	Extra punctuation in figure reference 'Figure 149-6. .'.	Remove the extra period.	EZ
47	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.2.2	91	1	E	typo: dot at end of line	remove " ." at end of line	EZ
79	Wienckowski, Natalie	IVN Solutions LLC	201	201.3.2.2	91	1	E	extra period	Remove duplicate period at end of sentence.	EZ
232	Pandey, Sujan	Velinktech	201	201.3.2.2	91	15	ER	Interleaver ad RS-FEC (360,326) encoder	Interleaver and RS-FEC (360,326) encoder	EZ
253	McCarthy, Frank	Infineon	201	201.3.2.2	91	15	E	"ad" should be "and" in block name	Interleave and RS-FEC(360,326) encoder	EZ
363	Jonsson, Ragnar	Infineon	201	201.3.2.2	91	15	E	Typo: "ad" instead of "and"	See comment	EZ

49	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.2.2	91	21	E	Figure 201-7 uses "10G Path" but Figure 201-6 uses "PAM4 data path".	replace "10G Path" with "PAM4 path"	EZ
50	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.2.2	91	23	E	Figure 201-7 uses "2.5G, 5G Path" but Figure 201-6 uses "PAM2 training/data path".	replace "2.5G, 5G Path" with "PAM2 path"	EZ
254	McCarthy, Frank	Infineon	201	201.3.2.2	91	30	E	Add interleaving description	Figure shown for L = 1, which means no interleaving. The L parameter specifies the number of FEC blocks interleaved together.	EZ
51	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.2.2	91	32	E	Figure 201-7 NOTE 3 for consistency with above comments 2.5G, 5G and 10G should be replaced	Replace: "For 2.5G and 5G" with "For PAM2 path". Replace "10G" with "PAM4 path"	EZ
48	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.2.2	91	34	E	The Figure is for HS_TX not HS_PATH. HS_PATH would also include the HS_RX which is not there.	replace "HS_PATH" with "HS_TX"	ACT Nomenclature
285	Razavi, Alireza	Infineon	201	201.3.2.2	92	1	E	reference to 'Figure 149-7" should be remove .	see comment	EZ
52	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.2.2	92	1	E	typo: dot at end of line	remove " ." at end of line	EZ
80	Wienckowski, Natalie	IVN Solutions LLC	201	201.3.2.2	92	1	E	extra period	Remove duplicate period at end of sentence.	EZ
53	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.2.2	92	19	E	Figure 201-8 uses "10G Path" not consistent with "PAM4 data path".	replace "10G Path" with "PAM4 path"	EZ
54	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.2.2	92	21	E	Figure 201-8 uses "2.5G, 5G Path" not consistent with "PAM2 training/data path".	replace "2.5G, 5G Path" with "PAM2 path"	EZ
256	McCarthy, Frank	Infineon	201	201.3.2.2	92	32	E	Note 1 is confusing.	At the top of this figure, the mapping of a 64B/65B block into eight data characters, D0 to D7, for the XGMII is shown.	EZ
255	McCarthy, Frank	Infineon	201	201.3.2.2	92	34	E	Add interleaving description	Figure shown for L = 1, which means no interleaving. The L parameter specifies the number of FEC blocks interleaved together.	EZ
55	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.2.2	92	35	E	Figure 201-8 NOTE 3 for consistency with above comments 2.5G, 5G and 10G should be replaced	Replace: "For 2.5G and 5G" with "For PAM2 path". Replace "10G" with "PAM4 path"	EZ
56	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.2.2	92	36	E	The Figure is for HS_RX not HS_PATH. HS_PATH would also include the HS_TX which is not there.	replace "HS_PATH" with "HS_RX"	EZ
57	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.2.2	92	41	E	"10G HS_PATH". Terminology: "10G" is not defined. The 1800 PMA_UNITDATA transfers are only for the HS_TX. Not for the HS_PATH which consists of both the HS_TX and HS_RX	replace "10G HS_PATH" with "PAM4 path HS_TX (10Gb/s)"	EZ
257	McCarthy, Frank	Infineon	201	201.3.2	92	42	E	The 1:18 refers to the ratio of the transfer rates and only if rate adaptation is not needed.	For the 10G HS_PATH, it takes 1800 PMA_UNITDATA transfers to send an RS-FEC frame of data. For the 10G HS_PATH, if the ratio of the XGMII to PMA transfer rates is exactly 1:18, then the transmit process does not need to perform rate adaptation.	EZ
58	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.2.2	92	44	E	"2.5G and 5G HS_PATH". Terminology: "2.5G" and "5G" are not defined. The 3600 PMA_UNITDATA transfers are only for the HS_TX. Not for the HS_PATH which consists of both the HS_TX and HS_RX	replace "2.5G and 5G HS_PATH" with "PAM2 path HS_TX (2.5Gb/s and 5Gb/s)"	EZ

258	McCarthy, Frank	Infineon	201	201.3.2	92	45	E	The 1:36 refers to the ratio of the transfer rates and only if rate adaptation is not needed.	For 2.5G and 5G HS_PATH, it takes 3600 PMA_UNITDATA transfers to send an RS-FEC frame of data. For 2.5G and 5G HS_PATH, if the PCS is connected to an XGMII and PMA sublayer where the ratio of their transfer rates is exactly 1:36, then the transmit process does not need to perform rate adaptation.	EZ
59	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.2.2	92	47	E	"10G HS_PATH" in consistentcy to previous comments this needs to be updated	replace "10G HS_PATH" with "PAM4 path HS_TX (10Gb/s)"	EZ
260	McCarthy, Frank	Infineon	201	201.3.2.2	92	48	E	There should be commas around respectively.	and 149.3.2.2.21, respectively, with the	EZ
60	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.2.2	92	51	E	"2.5G and 5G HS_PATH" in consistentcy to previous comments this needs to be updated	replace "2.5G and 5G HS_PATH" with "PAM2 path HS_TX (2.5Gb/s and 5Gb/s)"	EZ
261	McCarthy, Frank	Infineon	201	201.3.2.2	92	52	E	comma should be after D_n	presented as D_n, where	EZ
262	McCarthy, Frank	Infineon	201	201.3.2.2	92	53	E	"is scrambled" should be "and are scrambled"	The bits of the interleaved RS-FEC superframe are presented as Dn, where n is an index indicating the symbol number, and are scrambled using an additive scrambler.	EZ
74	Zhu,	Infineon	201	201.3.2.2	92	53	E	... are presented as, Dn where' -- comma may be mis-postioned	change to '... are presented as Dn, where'	EZ
263	McCarthy, Frank	Infineon	201	201.3.2.2	93	1	E	Replace "The DSn is applied as additive scrambler sequence to incoming data bits Dn to generate a single scrambled data An as shown in Equation (201–1)." with the proposed change, which includes defining D_n for the 2.5G and 5G HS_PATH.	All incoming 2.5G and 5G HS_PATH data bits are D_n, and D_n is represented in Figure 201-6 as D_n[0]. The DS_n are applied as an additive scrambler sequence to each incoming data bit, D_n, to generate a single scrambled data bit, A_n, as shown in Equation (201–1).	EZ
61	Lasry, Ariel	Qualcomm Technologies Inc.	201	201.3.2.2	93	8	E	"2.5G and 5G HS_PATH" in consistentcy to previous comments this needs to be updated	replace "2.5G and 5G HS_PATH" with "PAM2 path HS_TX (2.5Gb/s and 5Gb/s)"	EZ
180	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	201	201.3.2.2	93	9	E	Just to say "encode … as specified." doesn't write the requirement. The requirement is actually written below on line 18 - this line isn't needed - 18 just needs to be written as a requirement. Additionally, lines 6 through 17 are unnecessary.	Change P93 L18 to read "For the 2.5G and 5G HS_PATH, each consecutive output symbol, An shall be mapped to a PAM2 encoded symbol M(n) as follows:" Delete lines 6 through 16.	EZ
329	Johnson, Samuel	Infineon	201	201.3.2.2	93	19	T	Mapping of logic0 -> +1 and logic1 -> -1 seems non-intuitive	If this is used by PAM2 in other standards, then leave unchanged. Otherwide, propose Logic0 -> -1 Logic1 -> +1	EZ
264	McCarthy, Frank	Infineon	201	201.3.2.3	93	24	E	"including, compliance" should be "includes compliance"	The PCS receive function for HS_PATH shall conform to the PCS 64B/65B receive state diagram in Figure 149-18, and the PCS Receive bit ordering in Figure 201–8 includes compliance with the associated state variables specified in 201.3.6.	EZ
181	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	201	201.3.2.3	93	26	T	There are no state variables specified in 201.3.6. Only "S" is mentioned there, and S is already taken care of earlier for referneces.	Delete "including, compliance with the associated state variables specified in 201.3.6"	EZ
233	Pandey, Sujan	Velinktech	201	201.3.2.3	93	30	ER	The received symbols are demaped and descrambling performed	The received symbols are demaped and descrambled	EZ
265	McCarthy, Frank	Infineon	201	201.3.2.3	93	30	E	"are demapped and descrambling performed." should be ""are demapped, and descrambling is performed."	The received symbols are demapped, and descrambling is performed.	EZ

81	Wienckowski, Natalie	IVN Solutions LLC	201	201.3.2.3	93	30	E	grammer	Change "descrambling performed" to "descrambling is performed".	EZ
234	Pandey, Sujan	Velinktech	201	201.3.2.3	93	41	ER	… PCS Receive checks the received PAM2 framing and signals the reliable ...	… PCS Receive checks the received PAM2 framing and signals for the reliable ...	EZ
185	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	201	201.3.2.3.1	94	10	T	General comment, Big Ticket Item - MultiSpeed PHYs. We need to decide whether we are specifying one (or 2) PMA/PCS types with multiple speed modes or one (or 2) PMA/PCS types per speed. Most of the language says we have a PMA/PCS per speed, and this is how it is usually done. However, the language here, and elsewhere, describes the speeds as "modes" of a PHY - as though we had a multi-speed PHY. This is the first reference, but it occurs in many places. 2.5G, 5G, or 10G are not "modes" - the text refers to "in 10G" or "in 10G mode" (or 2.5G, or 5G…) in many places. There is a 2.5G+100MBASE-T1/V1 PHY transmiting 2.5 Gb/s, (and a 100M+2.5GBASE-T1/V1 PHY receiveing at 2.5Gb/s, and the other speeds similarly have their own phys). While these edits are clear on clause 201 - they equally apply to 202, where the description of the phy is confused in that it speed-selects during PHY training, without a separate auto-neg sublayer (See 202.4.2.4.5) suggesting a multi-speed PHY.	Assuming at least clause 201 is one PMA/PCS per speed, Change "When operating in the data mode in 10G, the HS_RX PCS forms" to "When operating in the data mode, a100M+10GBASE-T1/V1 PHY's HS_RX PCS shall form", and change, "When operating in the data mode in 2.5G and 5G, the HS_RX PCS" to "When operating in the data mode, a 100M+2.5GBASE-T1/V1 PHY and a 100M+10GBASE-T1/V1 PHY's HS_RX PCS's each"... Similarly, change at P117 L35, "and the PHY is transmitting in 10G mode, it shall transmit" to "a 10G+100MBASE-T1/V1 PHY shall transmit..." 201.8.1 Change at P117 L38, "and the PHY is transmitting in 5G or 2.5G mode, it shall transmit" to "a 2.5G+100MBASE-T1/V1 PHY or a 5G+100MBASE-T1/V1 PHY shall each transmit..." 201.8.2.2 Change at P121 L6, "when transmitting in 10G mode" to "for a 10G+100MBASE-T1/V1 PHY" Change at P121 L6, "For 5G and 2.5G modes" to "For 5G+100MBASE-T1/V1 or 2.5G+100MBASE-T1/V1 PHYs" Editorial license to replace other "mode" usage	Duplexing Method
184	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	201	201.3.2.3.1	94	10	T	Missing shall. There is one for the formation of the PAM2 stream, but not for the PAM4 stream. Additionally, while its nice to reference clause 149, 149.3.2.3.1 is sufficiently short you might as well put it here - AND - it is parallel to the new text needed for 2.5Gb/s and 5Gb/s	change "forms a PAM4 stream" to "shall form a PAM4 stream". Consider simply replacing the first paragraph on 201.3.2.3.1 with the text of 149.3.2.3.1	EZ
391	Muma, Scott	Microchip	201	201.4	95	14	T	The PCS is a sublayer within the PHY comprising a transmit and receive, which makes describing it only as LS_PATH functions a challenge in the current text structure.	Describe the functions/structure of a PHY_S PCS in one subclause, including subclauses for the HS_TX and LS_RX. Then in another subclause describe the functions/structure of a PHY_D PCS, including subclauses for the HS_RX and LS_TX. This will be consistent with the layered structure of the document rather than mixing the layer and path within one description.	ACT PCS
124	Wang, Frank	Realtek Semiconductor Corp.	201	201.4.2.2	96	42	E	wording	change "MultiGBASE-T1" to "100M+MultiGBASE-T1/V1"	EZ
82	Wienckowski, Natalie	IVN Solutions LLC	201	201.4.2.2	96	43	T	copy paste error from Clause 149	Change: MultiGBASE-T1 PCS To: 100M+MultiGBASE-T1/V1	EZ
125	Wang, Frank	Realtek Semiconductor Corp.	201	201.4.2.2	96	51	E	wording	change: "take four 65B blocks and append a 10-bit OAM field followed by 6 reserved bits set to all 1s to each group." to: "take 1 group of 4 65B blocks and append a 10-bit OAM field followed by 6 reserved bits set to all 1s to it."	EZ

201	van Dyck, Peter	Infineon	201	201.2.4	96		E	Leftmost vertical line is out of place.	Align leftmost vertical line arrow top and bottom to touch dotted lines at XGMII and PHY D PMA SERVICE INTERFACE. Align label "PCS" to not overlap line and be centered	EZ
126	Wang, Frank	Realtek Semiconductor Corp.	201	201.4.2.2	97	2	E	wording	change "T" to "T"	EZ
127	Wang, Frank	Realtek Semiconductor Corp.	201	201.4.2.2	97	12	E	wording	change "Tn" to "Tn"	EZ
202	van Dyck, Peter	Infineon	201	201.4.2.2	97	12	E	"(Tn)" the n should be subscript and this should be italic.	See comment	EZ
216	van Dyck, Peter	Infineon	201	201.4.2.2	97	12	E	"defined in 201.3.5.1" This section defines how Tn is derived for Sn in HS_PATH, Sn and Tn are not defined in the draft for LS_PATH, which has a different training frame than the HS_PATH.	Change to "defined in 201.4.5.1" For definition of Sn for LS_PATH and Clause 201.4.5.1 see comment for Clause 201.4.5	EZ
75	Zhu,	Infineon	201	201.4.2.2.2	98	35	T	the bit ordering in the figure looks like Bit299 is sent first	Bit ordering in Figure shall be reversed from Bit0…Bit299 to Bit299…Bit0 to reflect that Bit0 is transmitted first	ACT Bit order
271	Lo, William	Axonne Inc	201	201.4.2.2.15	103	3	T	There is no interleaving or superframes in the LS_PATH	Change: interleaved RS-FEC superframe To: RS-FEC frame	EZ
128	Wang, Frank	Realtek Semiconductor Corp.	201	201.4.2.2.15	103	3	T	wording: since there is no interleaver in LS_TX, "interleaved" should be removed	change "the interleaved RS-FEC" to "the RS-FEC"	EZ
395	Muma, Scott	Microchip	201	201.4.2.2.16	103	12	TR	DME encoding may be better done as a PMA function similar to other existing 802.3 clauses	Move DME encoding from PCS to PMA.	DME
203	van Dyck, Peter	Infineon	201	201.4.2.3.1	104	46	E	"block lock" underscore missing	Replace with "block_lock"	EZ
286	Razavi, Alireza	Infineon	201	201.4.5	105	5	E	enumaration is not correct and all of them are a)	enumaration should be updated	EZ
129	Wang, Frank	Realtek Semiconductor Corp.	201	201.4.3	105	18	E	grammar: comma afrer "mode"	change "mode" to "mode,"	EZ
130	Wang, Frank	Realtek Semiconductor Corp.	201	201.4.3	105	19	T	The initial condition of the scrambler is missed.	change: "by setting the data input to the scrambler to zero" to: "by setting zero input and any non-zero initial condition to the scrambler"	EZ
287	Razavi, Alireza	Infineon	201	201.4.5	105	34	E	64/65 blocks	64/65 blocks" replaced by "64B/65B blocks"	EZ
272	Lo, William	Axonne Inc	201	201.4.5	106	3	T	Add the following sentence for clarity.	After the training frame is assembled, it is scrambled and DME encoded as described in 201.4.2.2.15 and 201.4.2.2.16 respectively.	EZ
273	Lo, William	Axonne Inc	201	201.4.5.1	106	19	T	Need to talk about setting scr_status during descrambling.	1) Add section 201.4.5.1 PMA training mode descrambler polynomials 2) Text should be: The PHY shall acquire descrambler state synchronization to the DME training sequence and report success through scr_status.	ACT PMA

217	van Dyck, Peter	Infineon	201	201.4.5	106	32	E	Definition of Sn for LS_PATH is missing, definition of Tn for LS_PATH (Clause 201.4.5.1) is missing.	For definition of Sn, append below text and equation to Clause 201.4.5, page 106, line 18: "Sn defines the training frame bit at time n, see Equation (201-…)" use equation found in Sn.pdf For definition of Tn, append the below text as Clause 201.4.5.1, page 106, line 18: "201.4.5.1 Generation of symbol Tn The bit Sn is encoded to the DME transmit symbol Tn applying the following rules: — A “clock transition” shall always be generated at the start of each bit. — A “data transition” in the middle of a nominal bit period shall be generated if the bit to be transmitted is a logical '1'. Otherwise, no transition shall be generated until the next bit"	ACT PMA
204	van Dyck, Peter	Infineon	201	201.4.5.2	106		E	The PMA training mode descrambler polynomial, section 201.4.5.2 is missing for LS_PATH	Add the below text at Page 106 Line 18: 201.4.5.2 PMA training mode descrambler polynomial The PHY shall acquire descrambler state synchronization to the DME training sequence and report success through scr_status. For side-stream descrambling, the low speed receiver employs the receiver descrambler generator polynomial per 201.4.4.	ACT PMA
392	Muma, Scott	Microchip	201	201.5	107	12	T	The PMA sublayer description in 149.4 describes a PMA sublayer contained within a single PHY. Attempting to reference it to describe the HS_PATH functions of the PMA could lead to some unintended misunderstandings since the HS_PATH functions are not in a single PHY.	Describe the functions/structure of a PHY_S PMA sublayer in one subclause, including subclauses for the HS_TX and LS_RX. Then in another subclause describe the functions/structure of a PHY_D PMA sublayer, including subclauses for the HS_RX and LS_TX.	ACT PMA
364	Jonsson, Ragnar	Infineon	201	201.5	107	17	T	EEE should be removed	Add to list "3) No EEE support"	ACT EEE
393	Muma, Scott	Microchip	201	201.6	107	19	T	The PMA sublayer description from an LS_PATH only perspective is extremely challenging to understand from the text. The PMA transmit and receive functions defined exist in 2 distinct instances of the PMA sublayer even though the single PMA sublayer is defined as containing a transmit and receive function. Similarly a single PHY control function instance does not interact with both ends of the LS_PATH.	Describe the functions/structure of a PHY_S PMA sublayer in one subclause, including subclauses for the HS_TX and LS_RX. Then in another subclause describe the functions/structure of a PHY_D PMA sublayer, including subclauses for the HS_RX and LS_TX.	ACT LS PMA
365	Jonsson, Ragnar	Infineon	201	201.6.1	107	26	T	Text missing for this section	Add text corresponding to Figure 149-26 and Clause 149.4.2	ACT PMA
366	Jonsson, Ragnar	Infineon	201	201.6.2	107	36	E	Refference figure is missin	Add figure referenced in this line	ACT PMA
367	Jonsson, Ragnar	Infineon	201	201.6.2	107	38	E	Refference figure is missin	Add figure referenced in this line	ACT PMA
368	Jonsson, Ragnar	Infineon	201	201.6.2.1	107	50	T	Change 100ms to 50ms (see also Caluse 202.4.2.1)	See comment	EZ
288	Razavi, Alireza	Infineon	201	201.6.2	107		T	figure for pma refrence diagram is missing.	figure can be copied from 149-26 with removing the dashed line signals related to EEE	ACT PMA
369	Jonsson, Ragnar	Infineon	201	201.6.2.2	108	4	E	Clarify that Coax is also single "pair"	Add the word "signle" in front of "Coax cable"	EZ

370	Jonsson, Ragnar	Infineon	201	201.6.2.1	108	15	T	Support for PHY-D as follower should be optional	See comment	ACT Autonegotiation
379	Wang, Frank	Realtek Semiconductor Corp.	201	201.6.2.3	108	27	E	wording: add "The" before "PMA Receive contains"	change "PMA Receive contains" to "The PMA Receive contains"	EZ
131	Wang, Frank	Realtek Semiconductor Corp.	201	201.6.2.3	108	27	E	wording: remove "low speed"	change "The low speed PMA Receiver" to "The PMA Receiver"	EZ
132	Wang, Frank	Realtek Semiconductor Corp.	201	201.6.2.3	108	28	E	There is no such comma in 149.4.2.3.	change "MDI," to "MDI"	EZ
371	Jonsson, Ragnar	Infineon	201	201.6.2.3	108	31	E	RFER is missing 10^{-10} after 2x	See comment	EZ
133	Wang, Frank	Realtek Semiconductor Corp.	201	201.6.2.3	108	34	E	wording: remove "low speed direction"	change "The low speed direction PMA Receiver" to "The PMA Receiver"	EZ
235	Pandey, Sujan	Velinktech	201	201.6.2.3	108	35	ER	loc_rcvr_status varialbe accordingly	loc_rcvr_status varialbe accordingly.	EZ
83	Wienckowski, Natalie	IVN Solutions LLC	201	201.6.2.3	108	35	E	missing period	Add a period after accordingly.	EZ
134	Wang, Frank	Realtek Semiconductor Corp.	201	201.6.2.3	108	35	E	period is missed	change "accordingly" to "accordingly."	EZ
372	Jonsson, Ragnar	Infineon	201	201.6.2.4	108	48	T	There are sigificant updates from clause 149 that need to be added	See comment	ACT LS PMA
394	Muma, Scott	Microchip	201	201.7	109	3	T	This contradicts the text in 201.5 that says the HS_PATH PMA functions are specified in 149.4 as 149.4 defines all of these functions already.	Describing the PMA in terms of PHY_S/PHY_D instance functions rather than HS_PATH/LS_PATH functions may remove the contradiction if there are some common functions between the PHY_S and PHY_D.	ACT PMA
373	Jonsson, Ragnar	Infineon	201	201.7	109	3	E	Use HS and LS instead of "fast" and "slow"	See comment	EZ
135	Wang, Frank	Realtek Semiconductor Corp.	201	201.7	109	3	E	wording	change "fast and slow directions" to "HS_PATH and LS_PATH"	Nomenclature
374	Jonsson, Ragnar	Infineon	201	201.7.1	109	16	T	PAM2 is only used for training in HS direction	Update text to clarify that PAM2 is osed in HS direction and add "DMA is used in LS direction as specified in Caluse …"	ACT PMA
136	Wang, Frank	Realtek Semiconductor Corp.	201	201.7.1	109	16	T	In the training state, HS_PATH and LS_PATH use different modulation.	change "PAM 2 transmission is used" to " PAM2 transmission is used for HS_PATH and DME transmission is used for LS_PATH,"	EZ
205	van Dyck, Peter	Infineon	201	201.7.1	109	16	E	LS_PATH uses DME during training, not PAM2	Modify text with: "In the TRAINING state, PAM 2 transmission is used for HS_PATH, DME transmission is used for LS_PATH and …."	EZ
375	Jonsson, Ragnar	Infineon	201	201.7.1	109	29	T	100ms is too long, all times in Table 201-6 should be scaled down by 50%	See comment	ACT Startup
376	Jonsson, Ragnar	Infineon	201	201.7.1	109	42	T	100ms is too long, all times in Table 201-7 should be scaled down by 50%	See comment	ACT Startup
405	Muma, Scott	Microchip	201	201.7.2.1	110	18	ER	The state variables subclause of the Link Monitor seems to be incorrect. It has variables for the PHY control state diagram and the PHY control state diagram is a subclause of the variables.	Move the PHY control variables/timers to the state variables section of the PHY Control function. Make the PHY Control state diagram subclause a subclause fo the PHY control function or nmove to the PMA state diagrams in 201.7.8	ACT PHY Control
289	Razavi, Alireza	Infineon	201	201.7.2.1.3	111	4	E	EEE is not defined. this section should be removed " and the EEE Refresh monitor state diagram for the fast data path is shown in Figure 149–34."	see comment	ACT EEE

209	Abedinzadeh, Bizhan	Infineon	201	201.7.2.1.3	111	6	T	Figure 201-17 should remove restart paths from PCS_TEST/TX_SWITCH/COUNT_DOWN to SILENT.	The restart should be only triggered in Link Sync state machine, Figure 201-20 LINK_GOOD_CHECK transition to TRANSMIT_DISABLE.	ACT PHY control
210	Abedinzadeh, Bizhan	Infineon	201	201.7.2.1.3	111	6	E	Figure 201-17 remove MASTER/en_slave_tx	The terms should be changed to LEADER/en_follower_tx	EZ
211	Abedinzadeh, Bizhan	Infineon	201	201.7.2.1.3	111	6	T	Figure 201-17 transition from COUNTDOW to TX SWITCH should be changed.	((phy_role=PHY_S*loc_countd-won_done)*infofield_complete + phy_role=PHY_D	ACT PHY control
212	Abedinzadeh, Bizhan	Infineon	201	201.7.2.1.3	111	6	T	Figure 201-17 , need a state Follower transmits and Leader is silent	Add a state from SILENT to Training where only Follower will enter. In this state Follower should be sending SEND_T. This state shall last for min wait time of 300us. The silent period for FOLLOWER in silent state should be reduced to allow for this extra state.	ACT PHY control
213	Abedinzadeh, Bizhan	Infineon	201	201.7.2.1.3	111	6	T	Figure 201-17. Reduction of min wait timers, allow for quicker linkup	Min wait timer for SILENT and PCS TEST should be reduced to 500us	ACT PHY control
76	Zhu,	Infineon	201	201.7.2.1.3	111	22	E	to unify the names of roles	change to Leader and Follower	EZ
290	Razavi, Alireza	Infineon	201	201.7.2.1.3	111	23	E	en_slave_tx should be replaced by en_follower_tx	see comment	EZ
404	Muma, Scott	Microchip	201	201.7.2.1.3	111	40	TR	The rem_countdown_done is defined as "set to TRUE once the receiver has transitioned from PAM2 to PAM4." So it only works for 10G. How shall it be set to true for 2.5G/5G PHY_D HS_RX? No need to wait in that case, but need a variable phy_type to determine if wait is required, or redefine rem_countdown_done to work for 2.5G/5G.	Change (phy_role = PHY_D * rem_countdown_done) to (phy_role = PHY_D * (rem_countdown_done + phy_type != 100M+10GBASE-T1/V1))	ACT PHY Control
266	McCarthy, Frank	Infineon	201	201.7.3	112	18	T	Should add arrows from the reception of the Leader link sync pulse to the following transmitted pulse from the follower. This would be like a timing diagram showing the leader pulse detection at the follower causing the follower to reply with the follower pulse. The leader pulse must cause the follower to respond so that the timing between the leader and follower is stable.	See comment	ACT Link Sync
267	McCarthy, Frank	Infineon	201	201.7.3	112	42	T	For each SEND_S pulse that the follower detects, the follower is allowed to answer with one SEND_S pulse to the Leader. If follower does not detect a SEND_S pulse from the leader, then the follower skips transmitting its SEND_S pulse. A question is should a missing SEND_S pulse from the leader cause the follower to wait for three consecutive pulses from the leader before sending additional SEND_S pulses to the leader? Should the leader send a "reverse polarity" SEND_S pulse to indicate that the leader detected the SEND_S pulses from the follower? This would provide a "closed-loop" link-synchronization method, i.e. the follower would never leave before the leader had detected its SEND_S pulses.	Add text describing behavior when SEND_S pulse is missing.	ACT Link Sync

291	Razavi, Alireza	Infineon	201	201.7.3	112	44	E	misspelling SENDS_S should eb replaced by SEND_S	see comment	EZ
84	Wienckowski, Natalie	IVN Solutions LLC	201	201.7.3.1	114	4	E	missing space	Add a non-breaking space between 3.1 and us. Also change "u" to the symbol for micro.	EZ
398	Muma, Scott	Microchip	201	201.7.3.2	114	20	TR	98.5.2 defines both break_link_timer_[HSM] and break_link_timer_[LSM], so it's ambiguous which should be used since clause 98 AN is not being used.	After see 98.5.2 Add: Refer to break_link_timer_[HSM].	ACT PHY Control
77	Zhu,	Infineon	201	201.7.3.2	114	20	T	break_link_timer is currently fixed at 300-305us but can be more flexible for different implementations	change to a minimum value corresponding to different link speeds	ACT Link Sync
399	Muma, Scott	Microchip	201	201.7.3.2	114	23	T	The link_fail_inhibit_timer_[HCD] is defined in 98.5.2 as a timer to allow the PHY to determine link integrity. It says "this timer shall expire 97 ms to 98 ms after entering the AN GOOD CHECK state." This state does not exist in the diagram, but assume LINK_GOOD_CHECK is intended instead of AN GOOD CHECK. 97-98ms seems like a very long time to determine link integrity. Suggest 49 to 50 ms or any reasonable value by consensus.	Replace "see 98.5.2" with: Timer for qualifying a link_status=FAIL indication or a link_status=OK indication when a link is first being established. A link will be considered “failed” only if the link_fail_inhibit_timer has expired and the link has still not gone into the link_status=OK state. The expiration time of the link_fail_inhibit_timer shall be 49 ms to 50 ms after entering the LINK_GOOD_CHECK state.	ACT PHY Control
215	Abedinzadeh, Bizhan	Infineon	201	201.7.3.2	114	23	T	Link_fail_inhibit_timer shall be reduced	Propose changing from 100ms to 50ms	ACT Link Sync
397	Muma, Scott	Microchip	201	201.7.3.4	115	1	TR	The figure shows setting sync_tx_symb to 0 or 1, but these are not valid settings according to 201.7.3.3. Valid settings are SEND_S and SEND_Z. Compare to Figure 149-31	Change the diagram to be SEND_Z in place of 0 and SEND_S in place of 1 when assigning sync_tx_symb.	ACT PHY Control
214	Abedinzadeh, Bizhan	Infineon	201	201-20	115	37	T	Allow restart from Link Sync when training fails	add loss of loc_rcvr_status to condition for state machine to transition from LINK_GOOD_CHECK to TRANSMIT_DISABLE	ACT Link Sync
407	Muma, Scott	Microchip	201	201.7.7	116	26	TR	Why is this specific to 100M+MultiGBASE-T1/V1 when it's under the Common PMA Functions section?	Possibly delete this section or correct depending on other changes/intent.	ACT PHY Control
406	Muma, Scott	Microchip	201	201.7.8	116	30	TR	Subclause 149.4.4 doesn't contain any state diagrams, so this reference is incorrect. Assuming 149.4.5 was intended, now the only new information is the PHY Control state diagram which will conflict with the PHY control state diagram in 201.7.2.3	Provide the intended PHY Control state diagram.	ACT PHY Control
137	Wang, Frank	Realtek Semiconductor Corp.	201	201.8	116	35	E	typo	change "forthe high speed path" to "for the HS_PATH"	EZ
206	van Dyck, Peter	Infineon	201	201.8	116	35	E	"forthe" space missing	Replace with "for the"	EZ
334	Jonsson, Ragnar	Infineon	201	201.8	116	36	E	missing space between 'for' and 'the'	for the high speed path	EZ

336	Jonsson, Ragnar	Infineon	201	201.8.1	117	26	T	For 5G and 2.5G NRZ mode, should not use the term JP03A, JP03B pattern anymore, otherwise when digital team implement it, if use the same bit sequence, it will be not what we want for NRZ mode. Or should put note on what is JP03A, JP03B pattern for NRZ mode	Change the text to: "Test mode 2 is for transmitter jitter testing on the MDI when the transmitter is in LEADER timing mode. For 10G HS_PATH, when test mode 2 is enabled, the PHY shall transmit a continuous pattern of JP03A (as specified in 94.2.9.1) or JP03B (as specified in 94.2.9.2) with the transmitted symbols timed from its local clock source. For 2.5G and 5G HS_PATH, the JP03A and JP03B signals shall be replaced with the equivalent PAM2 signals, using repeated sequence of {0,1} instead of repeated sequence of {0,3}."	ACT tests
243	Sakunia, Saket	Infineon Technologies	201	201.8.1	117	26	E	External text reference 94.2.9.1, should be in green		EZ
85	Wienckowski, Natalie	IVN Solutions LLC	201	201.8.1	117	26	E		change character type of 94.2.9.1 to "External"	EZ
337	Jonsson, Ragnar	Infineon	201	201.8.1	117	27	T	For PAM4 signal, to measure EOJ, need JP03B pattern since two bits form one symbol, while for NRZ signal, it's not necessary to define such a pttern anymore, can just use 1010 pattern to get duty cycle distortion (fine to call it EOJ for consistency) as in other NRZ standard (i.e. clause 130 5G KR). Also OK to define another NRZ pattern similar to JP03B pattern for consistency, maybe call it JP01B pattern		ACT tests
244	Sakunia, Saket	Infineon Technologies	201	201.8.1	117	27	E	External text reference 94.2.9.1, should be in green		EZ
86	Wienckowski, Natalie	IVN Solutions LLC	201	201.8.1	117	27	E		change character type of 94.2.9.2 to "External"	EZ
87	Wienckowski, Natalie	IVN Solutions LLC	201	201.8.1	117	38	E		change character type of 94.3.10.8 to "External"	EZ
138	Wang, Frank	Realtek Semiconductor Corp.	201	201.8.1	117	50	E	wording	change "2.5GBASE-T1, 5GBASE-T1, or 10GBASE-T1" to "multiG+100M/100M+MultiGBASE-T1/V1"	EZ
335	Jonsson, Ragnar	Infineon	201	201.8.1	120	11	T	How to understand the transmit reference clock in the test block diagram? DUT provides reference clock to spectrum analyzer? Spectrum analyzer doesn't need refclk.	change the comment to "the transmit reference clock in the test block diagram" is ambigious. DUTdoes provide reference clock to spectrum analyzer. . and ask for its removal	ACT tests
380	Johnson, Samuel	Infineon	201	201.8.2.1	120	48	T	For Output Droop Test, the measurement requires a frequency-locked clock.	Add to section "201.8.2.1 Maximum output droop" after existing text "It is recommended that a FOLLOWER PHY nominally operating in XTAL-less mode should include a method to use a reference clock provided by the measurement device."	ACT tests
88	Wienckowski, Natalie	IVN Solutions LLC	201	201.8.2.2	121	4	E		change character type of 120D.3.1.2 to "External"	EZ
240	Sakunia, Saket	Infineon Technologies	201	201.8.2.2	121	8	T	Transmitter Linearity test.Test Mode 4 measurement is impacted by presence of PoC/PoDL components. The measurement method needs to be updaetd to account for presence of PoC/PoDL components	Update the Value of Np used in calculation to reflect the value of expected PoC/PoDL components.	ACT tests

303	Penumuchu, Venkat	Infineon Technologies	201	201.8.2.3	121	21	TR	The J value is 1 for 10G & 5G and 2 for 2.5G	J=1 for 5G, J=2 for 2.5G	ACT tests
338	Jonsson, Ragnar	Infineon	201	201.8.2.3	121	40	T	The jitter spec is 6ps for Follower, should it be data rate dependent as what for Leader? CH spec for 2.5G is 8ps, higher than DM one.	Change "6 ps" to "6/S ps", "3 ps" to "3/S ps" and "60 ps" to "60/S ps"	ACT tests
381	Johnson, Samuel	Infineon	201	201.8.2.2	122	1	T	For Linearity Test, the measurement requires a frequency-locked clock.	Add to section "201.8.2.2 Transmitter linearity" after existing text "It is recommended that a FOLLOWER PHY nominally operating in XTAL-less mode should include a method to use a reference clock provided by the measurement device."	ACT tests
382	Johnson, Samuel	Infineon	201	201.8.2.4	122	39	T	For PSD Test, the measurement requires a frequency-locked clock.	Add to section "201.8.2.4 "Transmitter power spectral desnsity (PSD) and power level" after the existing text: "It is recommended that a FOLLOWER PHY nominally operating in XTAL-less mode should include a method to use a reference clock provided by the measurement device."	ACT tests
236	Pandey, Sujan	Velinktech	201	201.8.2.4	123	16	ER	all "HZ"	Hz	EZ
241	Sakunia, Saket	Infineon Technologies	201	201.8.2.8	125	9	T	Table 201-11 the Max transmit swing values are significanlty higher than 802.3ch. This causes un-necessary complications in implementing PHY's in Lower geometries.	Please revert the values back to 802.3ch, of 1.3V max	ACT transmitter
339	Jonsson, Ragnar	Infineon	201	Table 201-11	125	15	T			EZ
340	Jonsson, Ragnar	Infineon	201	201.8.2.5	125	15	T	1.7Vdpp will violate power level 2dBm max spec. What's the meaning to increase voltage spec but still keep power level spec to be -1~2dBm?		ACT transmitter
330	Johnson, Samuel	Infineon	201	201.8.2.6	125	28	T	To prevent overclockingg digitial logic, and to allow for natural VCO frequency variation, we prefer to operate open-loop atbetween -20 and 0% of nominal frequency. Current spec is -10 / +10%	For the FOLLOWER PHY running off free-running clock, shall be within the range we prefer 5624 * S MHz +/-20%	ACT transmitter
341	Jonsson, Ragnar	Infineon	201	201.8.2.6	125	29	T	What does short term mean? How short? Need clear definition		ACT transmitter
377	Jonsson, Ragnar	Infineon	201	201.8.2.6	125	29	T	Clock accuracy in crystal-less mode: change +/-10% should be +/-20%	See comment	ACT transmitter

190	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	201	201.8.3.2	125	46	T	While this test is labeled alien crosstalk, it has, for some time, been the only test in the standard for receiver noise tolerance. With the expected use of shielded media, it is time to rename it - because people think there is no alien crosstalk so they don't need to pay attention.	Change "Alien crosstalk noise rejection" to "Broadband stationary noise rejection" at P125 L46 Make same change at P225 L45 to 202.5.3.2. Change "tolerance to alien crosstalk noise." at line 48, to "tolerance to broadband stationary noise from a variety of sources." Change the title of Table 201-12 to "Broadband noise source, high speed" at P126 L44 (after Table 201-12), add Editor's note (to be removed prior to SA ballot) - Contributors to consider whether to specify additional noise sources, such as line spectra from power management ICs, or other common self-noise from associated components.	ACT noise
292	Razavi, Alireza	Infineon	201	201.8.3.2	126	1	E	camma is missing after specification "specification the frame loss ratio is less than"	see comment	EZ
242	Sakunia, Saket	Infineon Technologies	201	201.8.3.2	126	38	T	The alien crosstalk noise source between T1 and V1 shows a 3 dBm/Hz reduction when scaled to signal levels. In differential architectures, common-mode noise is typically rejected. In contrast, single-ended architectures convert this common-mode noise into additive noise. As a result, coaxial systems are generally more vulnerable to such interference. Also Applicable for TDD	The Alien cross talk level for Coax needs to be evaluated differently.	ACT noise
245	Sakunia, Saket	Infineon Technologies	201	201.9.1	127	51	E	External text reference 94.2.9.1, should be in green		EZ
89	Wienckowski, Natalie	IVN Solutions LLC	201	201.9.1	127	51	E		change character type of 94.2.9.1 to "External"	EZ
246	Sakunia, Saket	Infineon Technologies	201	201.9.1	127	52	E	External text reference 94.2.9.1, should be in green		EZ
342	Jonsson, Ragnar	Infineon	201	201.9.1	127	52	T	Similar as above, low speed mode, JP03A and JP03B pattern need to be reclarified, is DME applied or not?	Change paragraph to: "Test mode 2 is for transmitter jitter testing on the MDI when the transmitter is in LEADER timing mode. When test mode 2 is enabled, the PHY shall transmit a continuous pattern based on JP03A (as specified in 94.2.9.1) or JP03B (as specified in 94.2.9.2) with the transmitted symbols timed from its local clock source. The JP03A and JP03B signals shall be replaced with the equivalent DME signals, using repeated sequence of {0,1} instead of repeated sequence of {0,3}."	ACT tests
90	Wienckowski, Natalie	IVN Solutions LLC	201	201.9.1	127	52	E		change character type of 94.2.9.2 to "External"	EZ
91	Wienckowski, Natalie	IVN Solutions LLC	201	201.9.1	128	2	E		change character type of 94.3.10.8 to "External"	EZ
92	Wienckowski, Natalie	IVN Solutions LLC	201	201.9.2.2	128	48	E		change character type of 85.8.3.3.4 to "External"	EZ
237	Pandey, Sujan	Velinktech	201	201.9.2.5	130	1	ER	dBM/Hz	dBm/Hz	EZ

247	Sakunia, Saket	Infineon Technologies	201	201.9.2.5	130	40	T	Low Speed transmitter upped PSD mask needs to be extended beyond 400MHz. It should cover the same frequency region as High Speed Transmit PSD mask. Not doing that leaves the system vulnerable to devices introducing high frequency content beyond 400MHz	Extend the upper limit of PSD mask for the Low speed transmit, specify to 3500MHz	ACT tests
293	Razavi, Alireza	Infineon	201	201.9.2.5	131	1	E	in lines 2 and 3, wrong notation: dBM/Hz should be replaced with 'dBm/Hz'	see comment	EZ
238	Pandey, Sujan	Velinktech	201	201.9.2.5	131	2	ER	dBM/Hz	dBm/Hz	EZ
239	Pandey, Sujan	Velinktech	201	201.9.2.6	132	36	ER	… the transmit signalof ...	… the transmit signal of ...	EZ
294	Razavi, Alireza	Infineon	201	201.9.2.6	132	36	E	complex sentense and spelling error "the transmit signalof a 100M+MultiGBASE-V1 transmitter shall be" can be replaced by "the transmit signal shall be"	see comment	EZ
93	Wienckowski, Natalie	IVN Solutions LLC	201	201.9.2.6	132	36	E	missing space	Add a space between "signal" and "of".	EZ
333	Johnson, Samuel	Infineon	201	201.9.2	132	46	T	For the LEADER to provide a optimal reference clock for the FOLLOWER to use in XTAL-less operation with minimal jitter, define a maximum rise and fall time of the 100MHz transmission. See this presentation for reference: https://www.ieee802.org/3/dm/public/1125/Razavi_3dm_02a_1125.pdf	Create section 201.9.2.8 "Transmitter Rise and Fall Time" and add text: "For the LEADER to provide a optimal reference clock for the FOLLOWER to use in XTAL-less operation with minimal jitter, a maximum rise and fall time is defined for the 100MHz transmission. --The rise and fall transition time between 20% and 80% levels of the steady state voltage amplitude shall be less than TBD ns. --Measurement shall be performed using an all-ones sequence applied to the DME mapper. This sequence generates a deterministic square wave with frequency of 117MHz --Testmode 4 shall be used for this measurement"	ACT clock
248	Sakunia, Saket	Infineon Technologies	201	201.9.3	133	1	T	Alien cross talk noise bandwidth should cover the high speed transmission frequency range.	Extend the noise bandwidth of Alien Cross Talk noise to 3500MHz	ACT tests
384	Cheng, Xiaoyue	Infineon	201	201.11.1.1	133	46	T	Insertion loss spec starts from 3MHz, but return loss spec starts from 1MHz	Modify insertion loss spec to start from1MHz	ACT Link Segment
383	Cheng, Xiaoyue	Infineon	201	201.11.1.1	133	51	E	The unit for Fmax should be GHz or MHz, not Gb/s	Change to GHz	ACT Link Segment
249	Sakunia, Saket	Infineon Technologies	201	201.11.1.3	135	31	E	Return loss instead of "IReturn Loss"		EZ
386	Cheng, Xiaoyue	Infineon	201	201.11.1.6	135	48	E	should be link segment delay	change link delay to link segment delay	ACT Link Segment
387	Cheng, Xiaoyue	Infineon	201	201.11.1.6	135	49	E	should be link segment delay	change link delay to link segment delay	ACT Link Segment
385	Cheng, Xiaoyue	Infineon	201	201.11.1.6	135	50	T	maximum link segment delay. No frequency range	Add "at all frequencies between 2 MHz and Fmax" at the end of the sentence.	ACT Link Segment
388	Cheng, Xiaoyue	Infineon	201	201.12.1.6	136	49	E	should be link segment delay	change link delay to link segment delay	ACT Link Segment
389	Cheng, Xiaoyue	Infineon	201	201.12.1.6	136	50	E	should be link segment delay	change link delay to link segment delay	ACT Link Segment

162	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	201	201.13.2.1	138	17	E	Editor's note is not needed as Fmax is already scaled here.	Delete editor's note.	EZ
188	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	201	201.14.3	139	22	T	The MDI fault tolerance for coax can't possibly be 96.8.3. That specifies short circuits & powering voltages for a differential interface. I assume we can't specify connecting the shield ground to a positive voltage, so this would only apply to the signal conductor.	Replace 201.14.3 text with "The signal conductor of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of any wire to the shield ground or positive voltages of up to 50 V dc with the source current limited to 150 mA, as per Table 201-x, for an indefinite period of time. Normal operation shall resume after the short circuit(s) is (are) removed. The signal conductor of the MDI shall also withstand without damage high-voltage transient noises and ESD per application requirements." Add Table 201-x - Connection fault Signal Conductor No fault Ground +50 V dc -50V dc	ACT MDI
274	Lo, William	Axonne Inc	201	201.16	139		T	Redo delay constraints	2) The following paragraphs are taken from 149.10 but modified: In full duplex mode, predictable operation of the MAC Control PAUSE operation (Clause 31, Annex 31B)also demands that there be an upper bound on the propagation delays through the network. This implies that MAC, MAC Control sublayer, and PHY implementers conform to certain delay maxima, and that network planners and administrators conform to constraints regarding the cable topology and concatenation of devices. The HS_PATH delays for an implementation of the PHY link shall not exceed the limits shown in Table 201–AAA. The data delay is measured from the input of a given unit of data at the PHY_S XGMII to the presentation of the same unit of data by the PHY_D XGMII. The LS_PATH delays for an implementation of the PHY link shall not exceed the limits shown in Table 201–AAA. The data delay is measured from the input of a given unit of data at the PHY_D XGMII to the presentation of the same unit of data by the PHY_S XGMII.	ACT Delay
275	Lo, William	Axonne Inc	201	201.16	139		T	Add table 201-BBB		EZ
95	Wienckowski, Natalie	IVN Solutions LLC	202	202.1.8	140	32	E	duplicated sentence	Delete one instance of "All MultiG+100M/100M+MultiGBASE-T1 PHY implementations are compatible at the MDI.".	EZ

139	Wang, Frank	Realtek Semiconductor Corp.	202	202.1.5	148	49	T	polarity is only for T1	change "in the connection" to "in the connectionfor the single shielded balanced pair of conductors (T1)	EZ
140	Wang, Frank	Realtek Semiconductor Corp.	202	202.1.6	149	17	T	polarity is only for T1	change "in the connection" to "in the connectionfor the single shielded balanced pair of conductors (T1)	EZ
71	Maguire, Valerie	Copperopolis; aff'l w/ CME Consulting, Microchip, and NXP	202	202.1.7	149	26	E	This header and text should have been deleted when the order of the LS_PATH signaling and HS_PATH signaling clauses were swapped.	Delete "202.1.7 L" and re-number subsequent clauses.	EZ Test
94	Wienckowski, Natalie	IVN Solutions LLC	202	202.1.7	149	26	E	delete 202.1.7 as the title is just "L" and there is no content.	Delete: 202.1.7 L	EZ
141	Wang, Frank	Realtek Semiconductor Corp.	202	202.1.8	149	30	E	align with 149.1.5	change "at the XGMII" to "at the MDI and at the XGMII" remove "All MultiG+100M/100M+MultiGBASE-T1 PHY implementations are compatible at the MDI. All MultiG+100M/100M+MultiGBASE-V1 PHY implementations are compatible at the MDI."	EZ
142	Wang, Frank	Realtek Semiconductor Corp.	202	202.2.1.4.2	154	2	E	align with 149.2.2.4.2: insert ";"	change "100M+10GBASE-T1/V1 as" to "100M+10GBASE-T1/V1; as"	EZ
316	Gorshe, Steve	Microchip	202	202.2.1.7.3	155	33	T	The text should be updated to point to the clause 202 equivalent figure and subclauses, which resolves the Editor's Note.	Replace the current text with "The effect of the receipt of this primitive is specified in Figure 202-2, 202.3.2.3, 202.4.2.4 and 202.5." and remove the Editor's Note.	EZ
96	Wienckowski, Natalie	IVN Solutions LLC	202	202.3.2.1	161	13	T	Based on the objective: Define optional startup procedure which enables the time from power_on=FALSE to a state capable of transmitting and receiving valid data to be less than 100 ms, the maximimum time available to resume normal operation after reset is 100 ms.	Change "(TBD) ms" to "100 ms."	EZ
143	Wang, Frank	Realtek Semiconductor Corp.	202	202.3.2.2	163	12	E	wording	change "On" to "On"	EZ
144	Wang, Frank	Realtek Semiconductor Corp.	202	202.3.2.2.5	168	10	E	align with 149.3.2.2.5	change "their mappings to control codes" to "their mappings to MultiG+100M/100M+MultiGBASE-T1/V1 control codes"	EZ
145	Wang, Frank	Realtek Semiconductor Corp.	202	202.3.2.2.5	168	14	E	wording: "for" is missed	change "Control codes MultiG+100M/100M+MultiGBASE-T1/V1" to "Control codes for MultiG+100M/100M+MultiGBASE-T1/V1"	EZ
331	Johnson, Samuel	Infineon	202	202.3.2.2.22	172	29	T	For some Testmodes, a frequency locked to the test equipment is required.	It is recommened that a FOLLOWER PHY nominally operating in XTAL-less mode should include a test method to provide a reference clock such that the transmission rate shall be within the range of 5625 * S MHz +/- 50ppm. It is recommended that the reference clock be 117.186MHz	EZ
332	Johnson, Samuel	Infineon	202	202.3.2.2.22	172	52	T	Mapping of logic0 -> +1 and logic1 -> -1 seems non-intuitive	If this is used by PAM2 in other standards, then leave unchanged. Otherwide, propose Logic0 -> -1 Logic1 -> +1	EZ

97	Wienckowski, Natalie	IVN Solutions LLC	202	202.3.2.2.22	176	1	E	subject verb agrement	Change "transmit process send out" to "transmit process sends out".	EZ
146	Wang, Frank	Realtek Semiconductor Corp.	202	202.3.2.3	176	38	E	wording: "_" is missed (also for lines 39, 49, and 52)	change "block lock" to "block_lock"	EZ
98	Wienckowski, Natalie	IVN Solutions LLC	202	202.3.2.3	176	41	E	missing bracket	Change "RXD 31:0>" to "RXD <31:0>"	EZ
99	Wienckowski, Natalie	IVN Solutions LLC	202	202.3.5.2.1	183	43	T	Incorrect number of bytes and awkward wording.	Change "four bytes header" to "eight header bytes"	Refresh Header
147	Wang, Frank	Realtek Semiconductor Corp.	202	202.4.2.3	200	7	E	wording	change: uses the parameters pcs_status and scr_status, and the state of the equalization, and estimation functions to determine to: uses the parameters pcs_status and scr_status, the state of the equalization, and estimation functions to determine or uses the parameters pcs_status and scr_status, and the state of the equalization and estimation functions to determine	EZ
100	Wienckowski, Natalie	IVN Solutions LLC	202	202.4.2.3	200	16	T	polarity inversion applies to balanced pair only	at the end of the sentence add, "for balanced pair only."	EZ
186	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	202	202.4.2.4.5	202	46	T	Clause 202 related to Big Ticket Item - MultiSpeed PHYs. The PHY_S has 3 speed capabilities here. In other places of the draft, they are referred to as different PHY types. It appears however, that clause 202 describes a single type with speed selection built in, rather than autonegotiated by a separate sublayer which might select other clauses as the PHY type. Assuming that this is the case, then for interoperability, at least ONE of the speed grades should be mandatory, and the others optional. Note - while I've made a suggestion here, I'm not taking a side - but we need to be clear. If we really have an auto-negotiating set of PHY types, we need a separate sublayer, which is much more spec-writing work.	Append the following to line 47 (after "10 Gb/s capable.") "2.5 Gb/s support is a mandatory capability, and Oct10<5> should always be set to 1.	TDD speeds
148	Wang, Frank	Realtek Semiconductor Corp.	202	202.4.2.4.7	204	16	E	202.4.2.4.7 Phase switch PHY burst count	change "data switch" to "phase switch"	EZ
149	Wang, Frank	Realtek Semiconductor Corp.	202	202.4.2.4.11	205	47	E	grammar: comma afrer "PrecoderSel"	change "PrecoderSel and" to "PrecoderSel, and"	EZ
150	Wang, Frank	Realtek Semiconductor Corp.	202	202.4.2.4.11	205	52	T	not only COUNTDOWN stage but also PCS_TEST stage	change "At any COUNTDOWN stage" to "At any COUNTDOWN stage and PCS_TEST stage"	EZ
151	Wang, Frank	Realtek Semiconductor Corp.	202	202.4.2.5	206	16	E	wording: "_" is missed	change "link status" to "link_status"	EZ
400	Muma, Scott	Microchip	202	202.4.2.2	209	41	E	The editor's note can be removed as the descriptions of the timers are up to date with their usage in the diagram	Remove editor's note	EZ

408	Lee, Ching-Yen	Realtek Semiconductor Corp.	202	202.4.5	213	219	T	Figure 202-28 needs to be updated.	A presentation will be provided.	Link Monitor
220	Chini, Ahmad	Broadcom	202	202.5.1	216	18	T	The test mode 5 text does not correlate with the PSD specification of TDD as in Chini_3dm_03a_0125.pdf where the PSD specified for continous signaling with no quiet gap.	Change the following sentence "When test mode 5 is enabled, the PHY shall transmit as in non-test operation and in the LEADER data mode with data set to normal interframe idle signals." to When test mode 5 is enabled, the PHY shall transmit idle signals continuously with no quiet gap and with transmit signal level corresponding to the normal mode of operation. The test applies to both LEADER and FOLLOWER. The clock is sourced from a stable clock with 100PPM accuracy for this test.	TDD tests
307	Gorshe, Steve	Microchip	202	202.5.1	216	21	E	Better to add the explicity local clock rate	Replace the paragraph "When test mode 6 ." with "When the test mode 6 is enabled, the PHY shall transmit a continuous pattern of 30 {+1} symbols followed by 30 {-1} symbols with the transmitted symbols timed from its local 3 GHz clock source."	TDD tests
305	Gorshe, Steve	Microchip	202	202.5.1.1	216	35	T	As explained in the next comment, test fixture 6 should be removed	Remove the reference to Figure 202-35	TDD tests
306	Gorshe, Steve	Microchip	202	202.5.1.1	218	20	T	Test fixture 6 is redundant relative to test fixture 5	Remove Figure 202-35 and replace the Figure 202-34 caption with "Transmitter test fixture 5 for MultiG+100M/100M+MultiGBASE-V1 transmitter droop measurement, transmitter linearity measurement, power spectral density measurement, transmit power level measurement, and MDI jitter"	TDD tests
101	Wienckowski, Natalie	IVN Solutions LLC	202	202.5.2	218	36	T	The 50 ohm load is not a differential load. Change the text to match 201.8.2 and 201.9.2.	Change: Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 O for MultiG+100M/100M+MultiGBASE-T1 or a 50 O for MultiG+100M/100M+MultiGBASE-V1 resistive differential load connected to each transmitter output. To: Where a load is not specified, the transmitter shall meet the requirements of this clause with a 100 O resistive differential load connected to each transmitter output when connected to a -T1 link, and a 50 O resistive load connected to each single-ended transmitter output when connected to a -V1 link.	TDD tests
309	Gorshe, Steve	Microchip	202	202.5.2.3	220	22	T	Need to clarify that this pertains to both transmitter timing jitter and transmitter jitter at the MDI	Add the following sentence at the beginning of the first paragraph of 202.5.2.3: "This clause applies to both Transmitter Timing jitter and Transmitter jitter on the MDI."	TDD tests

308	Gorshe, Steve	Microchip	202	202.5.2.3	220	23	T	This first paragraph and its two numbered bullets need updating for a correction and greater clarity.	In the first paragraph of 202.5.2.3 delete "using test fixture 2 (see Figure 202-31". In the first bullet, replace "test mode 1" with "test mode 2 using test fixture 1 for -T1 and test fixture 5 for -V1" In the second numbered bullet, after "test mode 1" add the phrase "using test fixture 2"	TDD tests
310	Gorshe, Steve	Microchip	202	202.5.2.3.1	220	40	T	Ths sub-clause doesn't directly pertain to TDD, and the relavant information is captured above.	Remove 202.5.2.3.1	EZ
311	Gorshe, Steve	Microchip	202	202.5.2.3.2	220	40	T	Ths sub-clause doesn't directly pertain to TDD, and the relavant information is captured above.	Remove 202.5.2.3.2	EZ
218	Chini, Ahmad	Broadcom	202	202.5.2.4	224	1	T	Power spectral density Uppe/ Lower Masks shown for 10G+100MBASE-T1 is not correct.	Replace with the correct Plot shown in the page 7 of https://www.ieee802.org/3/dm/public/0125/Chini_3dm_03a_0125.pdf	TDD tests
219	Chini, Ahmad	Broadcom	202	202.5.2.5	225	7	T	Transmitter peak-to-peak output in Table 202-17 does not correlate with TDD Upper PSD MASK and for a PoC corner of 7MHz (corresponding to MDI RL limit line). See Chini_3dm_01a_0126.pdf for simulation and calculations.	Replace the values in the table 202.17 with max Peak to Peak of 1.3Vpp for 2.5G+100BASE-T1 and 100M+MultiGBASE-T1 and 1.5Vpp for both 5G+100MBASE-T1. 10G+100MBASE-T1 remains to be 1.7Vpp. Half of the mentioned values apply to V1. In addition change V1 to T1 in the first Column	TDD tests
409	Zerna, Conrad	NXP	202	202.5.3.2	225	46	TR	Missing limit / model	Alien noise model was presented in https://ieee802.org/3/dm/public/1124/Zerna_802.3dm_02_241110_TDD_proposal.pdf, page 4&5, will submit presentation with alien noise model proposal	TDD noise
321	Gorshe, Steve	Microchip	202	202.5.3.2	225	48	T	There have been no presentations on this topic and the 802.3ch limits may not be appropriate.	Add "Presentations on this topic are needed." to the Editor's Note	EZ
304	Gorshe, Steve	Microchip	202	202.6	226	3	T	Open clause with no text	Insert the following text: "2.5G+100MBASE-T1, 5G+100MBASE-T1, 10G+100MBASE-T1, 2.5G+100MBASE-V1, 5G+100MBASE-V1, 10G+100MBASE-V1, 100M+2.5GMBASE-T1, 100M+5GBASE-T1, 100M+10GBASE-T1, 100M+2.5GBASE-V1, and 100M+5GMBASE-V1, 100M+10GBASE-V12.5GBASE-T1, 5GBASE-T1, and 10GBASE-T1 make extensive use of the management functions that may be provided by the optional MDIO (Clause 45), and the communication and self-configuration functions provided by the optional (TBD pending decision on the need for AN) Auto-Negotiation (See Clause 98)."	EZ
410	Zerna, Conrad	NXP	202	202.7.1.1	226	21	TR	Missing IL limit	Take limit line from https://ieee802.org/3/dm/public/0125/Zerna_802.3dm_01_250122_IL_RL.pdf, page 5	TDD T1 LS
411	Zerna, Conrad	NXP	202	202.7.1.3	226	31	TR	Missing RL limit	Take limit line from https://ieee802.org/3/dm/public/0125/Zerna_802.3dm_01_250122_IL_RL.pdf, page 8	TDD T1 LS
412	Zerna, Conrad	NXP	202	202.7.2	227	11	TR	Missing limit	Take limit line from https://ieee802.org/3/dm/public/0524/Coax_Cables_Silvano_de_Sousa_ISAAC_Interim_may_2024(002).pdf, page 6	TDD T1 LS

312	Gorshe, Steve	Microchip	202	202.8.1.4	230	1	T	Coupling attenuation only pertains to differential pair cables and is not defined for coaxial cables	Replace the TBD with "Coupling attenuation is not not defined for coaxial cables.	TDD V1 LS
322	Gorshe, Steve	Microchip	202	202.8.1.5	230	9	T	Adopt the limits from https://ieee802.org/3/dm/public/0524/Coax_Cables_Silvano_de_Sousa_ISAAC_Interim_may_2024(002).pdf	Remove the Editor's note and insert, "The screening attenuation for 100M+MultiGBASE-V1 and MultiG+100MBASE-V1 link segments, measured in accordance with ISO 19642-11, shall meet the values determined using Equation (202-2X). Additional screening attenuation test methodologies are defined in Annex 149A. Screening attenuation(f) = -75 10=f<3000 dB -50 3000=f<5000 where f is the frequency in MHz; Equation (202-2X) is plotted in Figure 202-XX which is provided for information only." Grant Editor's license to apply to equation, numbering, and figure creation style. Grant Editor's license to add ISO 19642-11 details to subclause 1.3 Normative references.	TDD V1 LS
323	Gorshe, Steve	Microchip	202	202.8.2	230	19	T	Since this is a heading for the subsequent subclauses, no text is needed.	Remove the Editor's Note.	EZ
413	Zerna, Conrad	NXP	202	202.8.2.1	230	24	TR	Missing limit	Measurment data has been presented https://ieee802.org/3/dm/public/0524/felso_3dm_01_2405.pdf, will submit a presentation with limit line formula	TDD V1 LS
326	Gorshe, Steve	Microchip	202	202.8.2.1	230	24	T	Clause 149 is specific to differential pairs. There have been no presentations on this topic, especially regarding its relationship to coaxial cables.	Copy and insert the text currently found in 201.12.2.1 for -T1. Add "Presentations on this topic are needed for -V1." to the Editor's Note. Grant Editor's license to apply to equation, numbering, and figure creation style.	TDD V1 LS
414	Zerna, Conrad	NXP	202	202.8.2.2	230	30	TR	Missing limit	Measurment data has been presented https://ieee802.org/3/dm/public/0524/felso_3dm_01_2405.pdf, will submit a presentation with limit line formula	TDD V1 LS
327	Gorshe, Steve	Microchip	202	202.8.2.2	230	30	T	Clause 149 is specific to differential pairs. There have been no presentations on this topic, especially regarding its relationship to coaxial cables.	Copy and insert the text currently found in 201.12.2.2 for -T1. Add "Presentations on this topic are needed for -V1." to the Editor's Note. Grant Editor's license to apply to equation, numbering, and figure creation style.	TDD V1 LS
163	Zimmerman, George	CME Consulting/ADI,APL Gp, Cisco, Infineon, OnSemi, Sony	202	202.9.2.1	231	17	T	If Fmax should scale with baud rate, there should be different Fmax's listed - but there aren't. The link segment parameters are not scaled. If there is a scaling it would only be applicable to 2.5G+100BASE-T1.	Suggest delete editor's note, and add, "For 2.5GBASE-T1	TDD MDI

313	Gorshe, Steve	Microchip	202	202.10.1	232	11	T	Since this is indepent of modulation, it can use the same language as 201.14.1.	Replace the TBD with ; "Where coaxial cabling is used, the mechanical interface to the coaxial cabling is a single pin connector with a shield. Further specification of the mechanical interface is beyond the scope of this standard."	EZ
314	Gorshe, Steve	Microchip	202	202.10.2.1	232	23	T	Both -T1 and -V1 would have the same return loss parameters.	Remove the Editor's Note and insert the sentence "MDI return loss shall comply with 202.9.2.1."	EZ
325	Gorshe, Steve	Microchip	202	202.10.3	232	29	T	Replace the Editor's Note box and TBD with the proposed text and table.	See attached file.	TDD MDI
315	Gorshe, Steve	Microchip	202	202.9.3	232	29	T	.	Remove the Editor's Note and insert the sentence "MDI fault tolerance shall comply with 96.8.3."	EZ
317	Gorshe, Steve	Microchip	0	0			T			EZ
318	Gorshe, Steve	Microchip	0	0			T			EZ
319	Gorshe, Steve	Microchip	0	0			T			EZ
320	Gorshe, Steve	Microchip	0	0			T			EZ
324	Gorshe, Steve	Microchip	0	0			T			EZ