

IEEE P802.3dm D2.0 Asymmetrical Electrical Automotive Ethernet Initial Working Group ballot comments

CI FM	SC FM	P 1	L 34	#	255
Steve, Gorshe		Microchip Technology			
Comment Type	TR	Comment Status	D	7.5G	
Add a 7.5 Gb/s HS PHY option					
SuggestedRemedy					
Add 7.5 Gb/s support according to changes proposed in https://www.ieee802.org/3/dm/public/adhoc/060226/gorshe_3dm_02_D2d0_7d5G-comments.pdf (also attached), with editorial license.					
Proposed Response	Response Status		W		
PROPOSED ACCEPT IN PRINCIPLE.					
Accommodated by comment #357.					

CI FM	SC FM	P 1	L 34	#	265
Chini, Ahmad		Broadcom			
Comment Type	TR	Comment Status	D	7.5G	
Add a 7.5 Gb/s HS PHY option for use with Clause 192					
SuggestedRemedy					
Add 7.5 Gb/s support according to changes proposed in https://www.ieee802.org/3/dm/public/adhoc/060226/gorshe_3dm_02_D2d0_7d5G-comments.pdf , with editorial license.					
Proposed Response	Response Status		W		
PROPOSED ACCEPT IN PRINCIPLE.					
Accommodated by comment #357.					

CI FM	SC FM	P 1	L 34	#	267
Lou, Wei		Broadcom			
Comment Type	TR	Comment Status	D	7.5G	
Add a 7.5 Gb/s HS PHY option in 802.3 Clause 192.					
SuggestedRemedy					
Add 7.5 Gb/s HS PHY support according to changes proposed in https://www.ieee802.org/3/dm/public/adhoc/060226/gorshe_3dm_02_D2d0_7d5G-comments.pdf					
Proposed Response	Response Status		W		
PROPOSED ACCEPT IN PRINCIPLE.					
Accommodated by comment #357.					

CI FM	SC FM	P 1	L 34	#	270
Tu, Mike		Broadcom			
Comment Type	TR	Comment Status	D	7.5G	
The 7.5 Gb/s speed should be added to Clause 192 as a high speed option.					
SuggestedRemedy					
Adopt the proposed changes as shown in "https://www.ieee802.org/3/dm/public/adhoc/060226/gorshe_3dm_02_D2d0_7d5G-comments.pdf" .					
Proposed Response	Response Status		W		
PROPOSED ACCEPT IN PRINCIPLE.					
Accommodated by comment #357.					

CI FM	SC FM	P 1	L 34	#	273
Pan, Chunpo		Broadcom			
Comment Type	TR	Comment Status	D	7.5G	
In Clause 192, add a 7.5 Gb/s HS PHY option					
SuggestedRemedy					
Add 7.5 Gb/s HS PHY support according to changes proposed in https://www.ieee802.org/3/dm/public/adhoc/060226/gorshe_3dm_02_D2d0_7d5G-comments.pdf					
Proposed Response	Response Status		W		
PROPOSED ACCEPT IN PRINCIPLE.					
Accommodated by comment #357.					

CI FM	SC FM	P 3	L 2	#	275
Pan, Chunpo		Broadcom			
Comment Type	TR	Comment Status	D	1G	
In Clause 192, add 5 Gb/s HS and 1000 Mb/s LS PHY options					
SuggestedRemedy					
Add 5 Gb/s HS PHY and 1000 Mb/s LS PHY support according to changes proposed in https://www.ieee802.org/3/dm/public/adhoc/060226/chini_3dm_02a_D2d0_1G_comments-preview.pdf					
Proposed Response	Response Status		W		
PROPOSED ACCEPT IN PRINCIPLE.					
Accommodated by comment #358.					

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CI FM	SC FM	P 3	L 2	# 266
Chini, Ahmad		Broadcom		
Comment Type	TR	Comment Status	D	1G
Add a 7.5 Gb/s HS with 1Gb/s LS option to the Clause 192				
Add a 5.0 Gb/s HS with 1Gb/s LS option to the Clause 192				
SuggestedRemedy				
Add 7.5 Gb/s HS with 1Gb/s LS and 5Gs/s HS with 1Gb/s LS support according to changes proposed in chini_3dm_02a_D2d0_1G_comments-preview.pdf, with editorial license.				
Proposed Response	Response Status		W	
PROPOSED ACCEPT IN PRINCIPLE.				
Accommodated by comment #358.				

CI FM	SC FM	P 3	L 2	# 274
Pan, Chunpo		Broadcom		
Comment Type	TR	Comment Status	D	1G
In Clause 192, add 7.5 Gb/s HS PHY and 1000 Mb/s LS PHY options				
SuggestedRemedy				
Add 7.5 Gb/s HS PHY and 1000 Mb/s LS PHY support according to changes proposed in https://www.ieee802.org/3/dm/public/adhoc/060226/chini_3dm_02a_D2d0_1G_comments-preview.pdf				
Proposed Response	Response Status		W	
PROPOSED ACCEPT IN PRINCIPLE.				
Accommodated by comment #358.				

CI FM	SC FM	P 3	L 4	# 257
Steve, Gorshe		Microchip Technology		
Comment Type	E	Comment Status	D	EZ - pull
Add MultiG PHYs to the list				
SuggestedRemedy				
Add 100M+MultiGBASE-T1, 100M+MultiGBASE-V1, MultiG+100MBASE-T1 and MultiG+100MBASE-V1 to the list				
Proposed Response	Response Status		W	
PROPOSED ACCEPT.				

CI FM	SC FM	P 13	L 25	# 235
Muma, Scott		Microchip Technology Inc.		
Comment Type	TR	Comment Status	D	7.5G
Add a 7.5 Gb/s HS PHY option for use with Clause 192				
SuggestedRemedy				
Add 7.5 Gb/s support according to changes proposed in gorshe_3dm_02_D2d0_7d5G-comments.pdf in the June 2 ad hoc meeting folder https://ieee802.org/3/dm/public/adhoc/060226 , with editorial license.				
Proposed Response	Response Status		W	
PROPOSED ACCEPT IN PRINCIPLE.				
Accommodated by comment #357.				

CI FM	SC FM	P 13	L 25	# 236
Muma, Scott		Microchip Technology Inc.		
Comment Type	TR	Comment Status	D	1G
Add support to Clause 192 for a 1 Gb/s LS PHY option for use with 5 and 7.5 Gb/s HS				
SuggestedRemedy				
Add 1 Gb/s support according to the changes proposed in chini_3dm_02a_D2d0_comments-preview.pdf in the June 2 ad hoc meeting folder https://ieee802.org/3/dm/public/adhoc/060226 , with editorial license.				
Proposed Response	Response Status		W	
PROPOSED ACCEPT IN PRINCIPLE.				
Accommodated by comment #358.				

CI 45	SC 45.5	P 46	L 26	# 448
Zimmerman, George		CME Consulting/ADI,Cisco,Eliyan,Infineon,OnSemi,		
Comment Type	E	Comment Status	D	PICS
PICS are missing for clause 45, 46, 98, 191, 192 (annex 98B doesn't have PICS)				
SuggestedRemedy				
Add draft PICS for all clauses to IEEE 802.3dm from zimmerman_PICS_3dm_061326.pdf with editorial license, including license to add / change per comment resolution.				
Proposed Response	Response Status		W	
PROPOSED ACCEPT.				

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CI 46 SC 46.1 P 47 L 7 # 227

Torres, Luisma KD
Comment Type TR Comment Status D Clause_46

The inclusion of asymmetric PHYs in the Overview is not clear. The first suggested addition at line 10 refers to the concept "Asymmetric PHYs" and the second one at line 11 refers to the inclusion (and not limiting to) asymmetric PHYs with one of these rates in one direction and 100 Mb/s in the reverse direction". A more clear rewording is needed, specially for the undefined "reverse" direction (is the "reverse direction" relative (and inverse) to the "one direction" or an absolute direction equivalent to the "parallel decoding" direction?).I suggest to use the "transmit and receive paths" concepts specified in 46.1.6.

SuggestedRemedy

Reword the third paragraph of 46.1 as follows: "The RS adapts the bit serial protocol of the MAC to the parallel encodings of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s symmetrical PHYs or to the parallel encodings of 2.5 Gb/s, 5 Gb/s, and 10 Gb/s asymmetrical PHYs in the transmit or receive path and 100 Mb/s in the other one.Though the XGMII is an optional interface, it is used extensively in this standard as a basis for specification. The 2.5 Gb/s, 5 Gb/s, and 10 Gb/s Physical Coding Sublayers (PCS), or the 100 Mb/s PCS in case of asymmetric PHYs, are specified to the XGMII, so if not implemented, a conforming implementation shall behave functionally as if the RS and XGMII were implemented."

Proposed Response Response Status W
PROPOSED ACCEPT.

CI 46 SC 46.1 P 47 L 10 # 23

Ran, Adeo Cisco Systems
Comment Type T Comment Status D Clause_46

"The 2.5 Gb/s, 5 Gb/s, and 10 Gb/s (including asymmetric PHYs with one of these rates in one direction and 100 Mb/s in the reverse direction) Physical Coding Sublayers (PCS) are specified to the XGMII"

This amended sentence does not make sense. The original sentence was about the various PCSs and the XGMII being their interface. The added parenthetical text talks about asymmetric PHYs, not PCSs.

The original sentence is still correct for many existing PCSs and should not be made more complicated by the addition of the new PCSs defined in this project.

The suggested remedy points to the specific PCSs using their clause numbers, which would be an improvement.

SuggestedRemedy

Change the quoted sentence to read
"The Physical Coding Sublayers (PCS) in Clause 127 (2.5BASE-X), Clause 179 (5GBASE-R), Clause 49 (10GBASE-R), Clause 191 (MultiG+100M/100M+MultiGBASE-T1/V1), and Clause 192 (MultiGBASE-A) are specified to the XGMII".

Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by #227.

IEEE P802.3dm D2.0 Asymmetrical Electrical Automotive Ethernet Initial Working Group ballot comments

CI 46 SC 46.1 P 47 L 16 # 24

Ran, Adeo

Cisco Systems

Comment Type T Comment Status D Clause_46

"It is capable of supporting at least one of the following rates of operation: 2.5 Gb/s, 5 Gb/s, or 10 Gb/s (including asymmetric PHYs with one of these rates in one direction and 100 Mb/s in the reverse direction)."

This sentence is in the "characteristics" list in the introduction subclause 46.1 and as such is essentially informative. The addition of the parenthesized text is not necessary. The original sentence is correct as it stands - the XGMII is indeed capable of supporting one of these rates - at least in one direction. The change does not create a normative requirement so it can be removed.

Similarly for 46.1.1 item i.

SuggestedRemedy

Delete the parenthesized text in item a and in item i of 46.1.1 (This would result in no change to these lists so the editing instructions can be removed).

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by #227.

CI 46 SC 46.1 P 47 L 19 # 228

Torres, Luisma

KD

Comment Type ER Comment Status D Clause_46

"Reverse direction" is not clear

SuggestedRemedy

Change "(including asymmetric PHYs with one of these rates in one direction and 100 Mb/s in the reverse direction)" to "(including asymmetric PHYs with one of these rates in the transmit or receive path and 100 Mb/s in the other path)."

Proposed Response Response Status W

PROPOSED ACCEPT.

CI 46 SC 46.1.1 P 47 L 26 # 229

Torres, Luisma

KD

Comment Type ER Comment Status D Clause_46

"Reverse direction" is not clear

SuggestedRemedy

Change "(including asymmetric PHYs with one of these rates in one direction and 100 Mb/s in the reverse direction)" to "(including asymmetric PHYs with one of these rates in the transmit or receive path and 100 Mb/s in the other one)."

Proposed Response Response Status W

PROPOSED ACCEPT.

CI 46 SC 46.1.3 P 47 L 42 # 486

Dawe, Piers

Nvidia

Comment Type TR Comment Status D Clause_46

"Symmetric operation at 10 Mb/s and 100 Mb/s is supported by the MII defined in Clause 22 and operation at 1000 Mb/s by the GMII defined in Clause 35": so what, this amendment is not about symmetric operation. Language.

SuggestedRemedy

Maybe something like this is meant: Asymmetric operation at 10 Mb/s and 100 Mb/s is defined for that direction by the MII of Clause 22 and similarly, operation at 1000 Mb/s is defined by the GMII of Clause 35." Add additional detail explaining how this works as necessary.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by #93 which removes this change.

CI 46 SC 46.1.3 P 47 L 43 # 93

Kim, Yong

General Motors

Comment Type TR Comment Status D Clause_46

"A compliant device may implement any subset of these rates in at least one direction" with "in at least one direction" inserted as new text. The new text allows for new capability of having XGMII operating at two separate high-speed, which is not intended nor correct.

SuggestedRemedy

Just delete the new text. I think it works.

Proposed Response Response Status W

PROPOSED ACCEPT.

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CI 46 SC 46.1.3 P 47 L 43 # 230
Torres, Luisma KD
Comment Type ER Comment Status D Clause_46
"Direction" is not specifically defined, but derived from transmit and receive path.
SuggestedRemedy
Change "in at least one direction" to "in the transmit or received path"
Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Accommodated by #93 which removes this change.

CI 46 SC 46.1.3 P 47 L 45 # 94
Kim, Yong General Motors
Comment Type ER Comment Status D Clause_46
"The XGMII supports a MAC data rate of 100 Mb/s in one direction, for asymmetric operation, when at least one of the specified multigigabit rates is used in the other direction." This new text does not flow well with previous sentences.
SuggestedRemedy
How about
"Asymmetric operation at one of the specified multigigabit rates in one direction, XGMII supports a MAC data rate of 100 Mbps in the other direction."
Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Accommodated by #102.

CI 46 SC 46.1.3 P 47 L 45 # 231
Torres, Luisma KD
Comment Type ER Comment Status D Clause_46
"Direction" is not specifically defined, but derived from transmit and receive path.
Asymmetry should appear before in the sentence.
SuggestedRemedy
Change "The XGMII supports a MAC data rate of 100 Mb/s in one direction, for asymmetric operation, when at least one of the specified multigigabit rates is used in the other direction." to "The XGMII supports for asymmetric operation a MAC data rate of 100 Mb/s in the transmit or receive path and 2.5 Gb/s, 5 Gb/s, or 10 Gb/s in the other path."
Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Accommodated by #102.

CI 46 SC 46.1.3 P 47 L 45 # 487
Dawe, Piers Nvidia
Comment Type T Comment Status D Clause_46
The XGMII supports a MAC data rate of 100 Mb/s in one direction, for asymmetric operation, when at least one of the specified multigigabit rates is used in the other direction.
SuggestedRemedy
The XGMII operates at a MAC rate of 100 Mb/s in one direction, for asymmetric operation, when at least one of the specified multigigabit rates is used in the other direction.
Proposed Response Response Status W
PROPOSED REJECT.

The MAC rate is the data rate.

CI 46 SC 46.1.3 P 47 L 45 # 102
Huber, Thomas Nokia
Comment Type E Comment Status D Clause_46
As written, the text talks about symmetric operation at 10/100M, and asymmetric operation at 2.5/5/10G, but never mentions symmetric operation at 2.5/5/10G (this is of course implied). It would be more clear to explicitly state that symmetric operation at 2.5G, 5G, and 10G is supported by the XGMII.
SuggestedRemedy
Replace the last sentence of the paragraph with this:
The XGMII supports symmetric operation with a MAC data rate of 2.5 Gb/s, 5 Gb/s, or 10 Gb/s. The XGMII supports asymmetric operation with a MAC data rate of 100 MB/s in one direction and at least one of the specified multigigabit rates in the other direction.
Proposed Response Response Status W
PROPOSED ACCEPT.

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Cl 46 SC 46.3.1.1 P 48 L 10 # 409

Zimmerman, George CME Consulting/ADI,Cisco,Eliyan,Infineon,OnSemi,

Comment Type T Comment Status D Clause_46

If a 7.5 Gbps high-speed rate is added, the text regarding the RS TX_CLK and RX_CLK need to be specified without specifying a new MAC rate, and the use of a 10 Gbps MAC parameterization should be identified.

SuggestedRemedy

Add the following new sentences (to shown in underline):
46.3.1.1 (at P48 L10, after the "transmit bit rate.") "When interfacing to a PHY with a 7.5 Gbps transmit bit rate, the TX_CLK frequency calculation shall use a 7.5 GHz in place of f_MAC, even though interfacing is to a MAC parameterized for 10 Gb/s as described in Table 4-2."
and, add to 46.3.2.1 (pat P48 L21, after "receive bit rate."
"When interfacing to a PHY with a 7.5 Gbps receive bit rate, the RX_CLK frequency calculation shall use a 7.5 GHz in place of f_MAC, even though interfacing is to a MAC parameterized for 10 Gb/s as described in Table 4-2."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Depends on 7.5G being included

Should either be "a 7.5GHz clock" or "7.5 GHz".

Cl 46 SC 46.3.1.1 P 48 L 10 # 232

Torres, Luisma KD

Comment Type ER Comment Status D Clause_46

Use the "transmit path" definition as specified in 46.1.6

SuggestedRemedy

Change "MAC's nominal transmit bit rate" to "MAC's nominal transmit path bit rate".

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by #25.

Cl 46 SC 46.3.1.1 P 48 L 10 # 25

Ran, Adeo Cisco Systems

Comment Type T Comment Status D Clause_46

"corresponding to the MAC's nominal transmit bit rate"

The MAC does not have a nominal transmit bit rate, nor a nominal receiver bit rate. The MAC is formally defined as an bit-oriented entity that uses service interface primitives, without an associated data rate (there is no frequency parameter for the MAC); it is the choice of RS (and PHY below it) that governs the bit rate. (This is also an issue in the existing text - and it's a good time to fix it)

This project is modifying the specification of the RS such that it will have different bit rates in each direction (essentially creating new types of RS, asymmetric). The MAC is not modified and still does not have bit rates. So it's the RS bit rate in each direction that should be mentioned.

Similarly for RX_CLK in 46.3.2.1.

SuggestedRemedy

Change from
"f_MAC is the frequency (in Hz) corresponding to the MAC's nominal transmit bit rate"
to
"f_MAC is the frequency (in Hz) corresponding to the nominal MAC bit rate that the RS provides in the transmit direction (2.5 Gb/s, 5 Gb/s, 10 Gb/s, or 100 Mb/s)"

Make a similar change in 46.3.2.1 for the receive direction.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Make the requested change, including appropriate strikethrough and underline with appropriate editor's instruction.

Cl 46 SC 46.3.1.1 P 48 L 11 # 115

Kim, Yong General Motors

Comment Type ER Comment Status D Clause_46

The addition of the word "transmit" does not add to clarity. It's already clear. TXCLK is by definitoin transmit direction. There is, however, technical concern on how asymmetric MAC rates are defined. It's missing (see my comment on CL4.4.2 reference).

SuggestedRemedy

Delete the added word "transmit"

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by #25.

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CI 46 SC 46.3.1.1 P 48 L 21 # 233
 Torres, Luisma KD
 Comment Type ER Comment Status D Clause_46
 Use the "transmit path" definition as specified in 46.1.6
 SuggestedRemedy
 Change "MAC's nominal receive bit rate" to "MAC's nominal receive path bit rate".
 Proposed Response Response Status W
 PROPOSED ACCEPT.

CI 46 SC 46.3.2.1 P 48 L 18 # 116
 Kim, Yong General Motors
 Comment Type TR Comment Status D Clause_46
 "it may be that of a nominal clock" of which "it may be that of a" is deleted as a change. I recall the original text to be permissible behavior, whereas with this deletion, it is not -- for other PHYs that use XGMII.
 SuggestedRemedy
 Unless the work was done to ensure all implementations prior to this project is not affected by this change, revert back this change. If the intended change is just for 802.3dm PHYs, text should be revised just for the CL191/2 PHY types.
 Proposed Response Response Status W
 PROPOSED ACCEPT.

CI 46 SC 46.3.2.1 P 48 L 18 # 401
 Nicholl, Shawn AMD
 Comment Type T Comment Status D Clause_46
 The revised text "the nominal clock (e.g., TX_CLK)" is more restrictive than the existing 802.3-2022 text. The revised text suggests (i.e. implies) that there is only one nominal clock. The existing 802.3-2022 text "a nominal clock (e.g., TX_CLK)" permits RX_CLK to use a nominal clock frequency that differs from the nominal frequency of TX_CLK.
 SuggestedRemedy
 Propose returning to the text ("a nominal clock") that exists in 802.3-2022. In other words, restore this text: "... received data or it may be that of a nominal clock (e.g., TX_CLK)."
 Proposed Response Response Status W
 PROPOSED ACCEPT.

CI 46 SC 46.3.2.1 P 48 L 18 # 234
 Torres, Luisma KD
 Comment Type ER Comment Status D Clause_46
 The suggested deletion implies losing the option to do not use the nominal clock
 SuggestedRemedy
 Revert the deletion to preserve flexibility
 Proposed Response Response Status W
 PROPOSED ACCEPT.

CI 46 SC 46.6.3.1 P 49 L 7 # 26
 Ran, Adeo Cisco Systems
 Comment Type T Comment Status D Clause_46
 The optional items in the PICS are intended to identify the feature set of a product. In the original PICS it was clear what G1, G2, and G3 mean. The proposed changes make it ambiguous: PHYs that use 100M in the Tx direction and PHYs that use 100M in the Rx direction will have the same set of PICs responses.
 There is a better way to define the features.
 SuggestedRemedy
 Replace the new item G3a with three separate items:
 G3a - PHY uses 100 Mb/s in the transmit direction
 G3b - PHY uses 100 Mb/s in the receive direction
 G3c - PHY does not use 100 Mb/s in either direction
 Ther 3 should have status "PHY:O/1" so that one and only one of them has to be supported.

Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 Make the requested change with editorial license to update if the referenced text changes.

CI 98 SC 98 P 50 L 4 # 488
 Dawe, Piers Nvidia
 Comment Type ER Comment Status D AN
 There is 73, Auto-Negotiation for backplane and copper cable assembly, which includes single-lane media. 73 precedes 98, so 98 cannot broaden its scope to "Auto-Negotiation for single-lane media"
 SuggestedRemedy
 If the distinction is that 98 is bidirectional and 73 is not, use that to choose a suitable title.
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 Accommodated by #1.

IEEE P802.3dm D2.0 Asymmetrical Electrical Automotive Ethernet Initial Working Group ballot comments

CI 98 SC 98.1.1 P 50 L 15 # 1

Ran, Adeo

Cisco Systems

Comment Type T Comment Status D AN

The original text included the words "single twisted pair", but it is amended to "single-lane media". This is an inappropriate name since there is another auto-negotiation function in clause 73 that also works on single-lane media, and there are other single-lane media (such as optical fibers) that do not use any form of auto-negotiation.

Clause 98 was indeed written specifically for single twisted pair applications. The new name is too broad and will cause confusion for readers who are not familiar with all of the 802.3 PHYs.

This change is pervasive in clause 98.

SuggestedRemedy

If the scope of this clause is to be extended to other media such as shielded balanced cables or unbalanced coaxial cables, the name can be changed to include these specific media. Alternatively, change the text such that it refers to the specific PHY types that use this clause, regardless of the media type.

In the remainder of the clause, change "Single twisted pair Auto-negotiation" to "Auto-negotiation defined in this clause" or just delete it if appropriate. Do not use "single-lane".

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change the title of Clause 98 to: Auto-Negotiation for single differential-pair or single-ended unbalanced media

P50L15

Change the first sentence of Clause 98:

Change: Clause 98 describes the single twisted-pair Auto-Negotiation function that allows a device to advertise....

To: Clause 98 describes the --single twisted-pair-- Auto-Negotiation function --that allows-- _used on single differential-pair media or single-ended unbalanced media to allow_ a device to advertise...

Throughout Clause 98 change: "Single-lane Auto-Negotiation" or "Auto-Negotiation for single-lane media"

To: Clause 98

Note 3 on Figure 98-2

Change: Medium is either a single-lane of differential balanced pair or unbalanced single-ended

To: Medium is either a single differential-pair or single-ended unbalanced

Change the title of Table 98-7 to: State diagram variable to _Clause 98_ --Single twisted-

pair-- Auto-Negotiation MDIO register mapping

Change 98.6 PICs to new Clause 98 title

98.5.1 PICS introduction needs to be updated to new clause title

98.6.2.2 PICS Protocol summary needs to be adjusted (P54 L20) to the new clause title.

98.6.4 PICS item G1 Feature changes to simply "Auto-Negotiation function"

--xxx-- means "xxx" is shown in strikethrough

xxx means "xxx" is shown in underline.

CI 98 SC 98.2.4.2 P 53 L 0 # 209

Slavick, Jeff

Broadcom

Comment Type TR Comment Status D AN

The base standard definition for Priority Resolution in Clause 98 appears to need some updating as well. I believe the resolution for Asymmertric is for not a single matching bit, but a pair of corresponding abilities where for example one side is 10G/100M (A16) and the other is 100M/10G (A15). If you hooked two devices that only advertised 10G/100M to each other they should fail to select a 10G/100M operation (which is a matching set of ability bits with both set A16).

SuggestedRemedy

In 98.2.4.2 change:

"The single PHY enabled to connect to the MDI by Auto-Negotiation shall be the technology corresponding to the bit in the Technology Ability Field common to the local device and link partner that has the highest priority as defined in 98B.4 (listed from highest priority to lowest priority)."

To:

"The PHY enabled to connect to the MDI by Auto-Negotiation shall be the technology corresponding to the bit in the Technology Ability Field that has the highest priority as defined in 98B.4."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Consider with #41

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general

COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed U/unsatisfied Z/withdrawn

SORT ORDER: Clause, Subclause, page, line

CI 98

SC 98.2.4.2

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CI 98 SC 98.5.1 P 53 L 46 # 41

Muma, Scott

Microchip

Comment Type T Comment Status D AN

This section contains a Note that redefines how priority resolution HCD is to work. This should be updated in 98.2.4.2 instead since that is where priority resolution is defined.

SuggestedRemedy

Replace the text in 98.2.4.2 with changes shown in muma_d2d0_asymmetric_98_4_2_4.pdf

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Consider with #209

CI 98 SC 98.6.2.2 P 54 L 21 # 103

Huber, Thomas

Nokia

Comment Type E Comment Status D AN

In the right-hand column of the table, Single Differential-Pair should be removed

SuggestedRemedy

Change Single Differential Pair to strike-through font

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Comment #1 or #488 may change what the name is. Make the appropriate change indications, strikethrough and underline, based on the final name.

CI 98B SC 98B.4 P 251 L 38 # 210

Slavick, Jeff

Broadcom

Comment Type TR Comment Status D AN

Table 93B-2 doesn't appear to be sustainable. I think you can retain it as a dashed list.

SuggestedRemedy

Replace 98B.4 with the following:

Since a local device and a link partner may have multiple abilities in common, a prioritization scheme exists to ensure that the highest common denominator ability is chosen. For PHYs with asymmetric transmit and receive rates the proper combination of abilities is required to negotiate to that operating mode. The following list shall represent the relative priorities of the technologies supported by the IEEE 802.3 Selector Field value, where priorities are listed from highest to lowest and "(L)" stands for "Leader" and "(F)" for "Follower":

- 25GBASE-T1
- 10GBASE-T1
- 100M+10GBASE-T1/V1 (L) with 10G+100MBASE-T1/V1 (F)
- 10G+100MBASE-T1/V1 (L) with 100M+10GBASE-T1/V1 (F)
- 5GBASE-T1
- 100M+5GBASE-T1/V1 (L) with 5G+100MBASE-T1/V1 (F)
- 5G+100MBASE-T1/V1 (L) with 100M+5GBASE-T1/V1 (F)
- 2.5GBASE-T1
- 100M+2.5GBASE-T1/V1 (L) with 2.5G+100MBASE-T1/V1 (F)
- 2.5G+100MBASE-T1/V1 (L) with 100M+2.5GBASE-T1/V1 (F)
- 1000BASE-T1
- 100BASE-T1L increased tx/rx
- 100BASE-T1L standard tx/rx
- 100BASE-T1
- 10BASE-T1S full duplex
- 10BASE-T1S half duplex
- 10BASE-T1L

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by 211.

IEEE P802.3dm D2.0 Asymmetrical Electrical Automotive Ethernet Initial Working Group ballot comments

CI 191 SC 191 P 56 L # 118

Kim, Yong

General Motors

Comment Type TR Comment Status D MAC

Asymmetric PHYs operate with XGMII down to 100 Mbps MAC rate (for the low-speed path). There is no reference to 100 Mbps MAC rates (explicit or implicit reference to CL 4.4.2 MAC parameters).

Suggested Remedy

If TF addressed this concern but not obvious to the reviewer, please help identify where it is addressed. And if it is addressed, whether CL4 or Annex 4A MAC is referenced.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Add the following as a new paragraph in 191.1 after the paragraph added by #143.

This clause defines multiple PHY types named according to <maximum transmit data rate>+<maximum receive data rate>BASE-T1/V1, where -T1 is for single differential balanced-pair media, and -V1 is for single-ended unbalanced media. Clause 191 PHYs are defined to use the Clause 46 Add: XGMII in a configuration where the RS supports an asymmetric data rate with the multigigabit transmit (or receive) rate on the TX (or RX) path, and the 100 Mb/s receive (or transmit) rate on the RX or TX path of the XGMII. The Clause 4 MAC parameters for the appropriate rate (multigigabit or 100 Mb/s) are used in conjunction with the PHYs described in this clause in conjunction with either the multigigabit (HS) path or the 100 Mb/s (LS) path.

CI 191 SC 191 P 56 L 4 # 2

Ran, Adeo

Cisco Systems

Comment Type T Comment Status D nomenclature

The title of clause 191 includes the list of PHYs covered, which is long. The same list repeats in the text of the clause as well as in other places in this draft. This is very disruptive to readers and does not add much value.

Since these PHYs have some common features and are distinct from others, it is adequate to give them a common nomenclature as a family of PHYs, following the example of MultiGBASE-A in this project, and other precedence, such as "BASE-R" and "BASE-T1" in the existing definitions.

I suspect that the new definition of 100M+MultiGBASE (1.4.46g) is suitable for some of these PHYs and MultiG+100MBASE (1.4.249a) covers the rest. The term "MultiG+100M/100M+MultiGBASE-T1/V1" is mentioned in 191.1.1 as covering both, but has no definition in 1.4.

Suggested Remedy

Use the family names 100M+MultiGBASE and MultiG+100MBASE to refer to all the PHYs in the respective family instead of listing all PHYs.

Add a definition of MultiG+100M/100M+MultiGBASE-T1/V1 in 1.4. and use this family name in the title of clause 191 and to replace the long lists in clause 191 and elsewhere in the document (e.g. in 46.1.2).

Use the family names in 191.1 and refer to the definitions in 191.1.1.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

See #281 for updated name and text in 191.1.

Add definition for MultiG+100M/100M+MultiGBASE between definitions as 1.4.249b, and increment new definitions added after this.

1.4.249b MultiG+100MBASE/100M+MultiGBASE: PHYs that belong to the set of specific asymmetric PHYs that transmit or receive at speeds in excess of 1000 Mb/s and receive or transmit at 100 Mb/s, with concurrent transmission in both directions, including 2.5G+100MBASE-T1, 2.5G+100MBASE-V1, 5G+100MBASE-T1, 5G+100MBASE-V1, 10G+100MBASE-T1, 10G+100MBASE-V1, 100M+2.5GBASE-T1, 100M+2.5GBASE-V1, 100M+5GBASE-T1, 100M+5GBASE-V1, 100M+10GBASE-T1, and 100M+10GBASE-V1. (See IEEE Std 802.3, Clause 191.)

IEEE P802.3dm D2.0 Asymmetrical Electrical Automotive Ethernet Initial Working Group ballot comments

CI 191 SC 191 P 56 L 4 # 452

RAJAGOPAL, KARTHIK

TEXAS INSTRUMENTS INC

Comment Type TR Comment Status D consensus

The draft as looked at an IEEE standard to facilitate interoperability fails to offer a clear implementation guide with more than 1 type of implementation/standard to choose from. Sections 191 and 192 with their widely different PCS & PMA layers fails to fulfil the primary goal which is to be a standard. This would not qualify as standard if users are free to choose from multiple implementations which tries to achieve the same function.

SuggestedRemedy

Rather than letting users guess or arbitrarily choose 1 of the 2 types of PCS & PMA implementation, a technically superior implementation needs to be selected and made as a standard with clear guideline on the PCS and PMA layers. This way facilitates maximum interoperability, which is the only path for this draft to be considered as an IEEE standard

Proposed Response Response Status W

PROPOSED REJECT.

The PHYs in Clause 191 and Clause 192 meet different approved objectives found in https://ieee802.org/3/dm/public/0326/Objectives_ISAAC_01_0326.pdf. The comment does not contain sufficient detail so that the CRG can understand the specific change being suggested by the commenter.

CI 191 SC 191 P 56 L 5 # 281

Jones, Peter

Cisco Systems

Comment Type E Comment Status D nomenclature

The repeated usage of "100M+2.5GBASE-T1, 2.5G+100MBASE-T1, 100M+5GBASE-T1, 5G+100MBASE-T1, 100M+10GBASE-T1, 10G+100MBASE-T1, 100M+2.5GBASE-V1, 2.5G+100MBASE-V1, 100M+5GBASE-V1, 5G+100MBASE-V1, 100M+10GBASE-V1, 10G+100MBASE-V" makes this hard to read.

Moving the definitions of MultiG+100M/100M+MultiGBASE-T1, MultiG+100M/100M+MultiGBASE-V1 and MultiG+100M/100M+MultiGBASE-T1/V1 to the front of the introduction and using them in the clause heading and in the rest of "191.1 Overview", as well as in PICs sub-clauses will significantly improve readability

SuggestedRemedy

Please see changes in P8023dm_D2p0_pjones_introduction.docx attached to ballot submission.

Make the equivalent changes in:

- 191.15 title
- 191.15.1 first paragraph
- 191.15.2.2 - Identification of protocol standard text
- 191.15.4 title

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Make changes as defined in P8023dm_D2p0_pjones_introduction.pdf with editorial license to make other updates, as appropriate.

CI 191 SC 191.1 P 56 L 15 # 117

Kim, Yong

General Motors

Comment Type E Comment Status D nomenclature

The list of PHY types is really long, and reader must follow carefully to understand slight differences. Normally we do not use PHY types in a table in the overview section. But this overview could use a table to help readers to make sense quickly.

SuggestedRemedy

Was going to suggest adding a table, by speed (HS and LS) and media type, but then found the Table 191-2. Consider moving and referencing Table 191-2 to the overview section and remove a long list of PHY types in the text. It may be clearer to split the Table 191-2 into two tables, one for balanced and one for single ended (easier to referecne from the overview clause).

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by #281 which updates the text in 191.1.

IEEE P802.3dm D2.0 Asymmetrical Electrical Automotive Ethernet Initial Working Group ballot comments

CI 191 SC 191.1 P 56 L 48 # 4

Ran, Adeo

Cisco Systems

Comment Type T Comment Status D 191_overview

I assume that the PHY types defined in this clause interoperate only asymmetrically, e.g. 100M+2.5GBASE-T1 and 2.5G+100MBASE-T1 can be used to form a link, but not two PHYs of the same type.

This is a non-trivial property of these PHYs and should be mentioned in the overview. In fact I do not see it mentioned anywhere, except implicitly in 98B.4, which is unclear and not referenced from clause 191; and auto-negotiation is defined as optional.

Also possibly in clause 192.

SuggestedRemedy

Add text in 191.1 and possibly elsewhere to describe the possible configurations of links using these PHYs.

Implement in clause 192 if appropriate.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

See #143

CI 191 SC 191.1 P 56 L 49 # 143

Wienckowski, Natalie

IVN Solutions LLC; Ethernova & Bosch

Comment Type E Comment Status D 191_overview

add new paragraph to define the type of transmission.

SuggestedRemedy

These PHYs continuously transmit in both directions concurrently, but at different baud rates. Unlike frequency division techniques, the PHYs have full spectral overlap in the two transmit directions, but utilize the relatively narrow bandwidth of the Low Data Rate (LDR) signal to enable separation without echo cancellation.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

These PHYs continuously transmit in both directions concurrently, but at different baud rates. Unlike frequency division techniques, the PHYs have full spectral overlap in the two transmit directions, but utilize the relatively narrow bandwidth of the Low Data Rate (LDR) signal to enable separation of the remote signal from the echo signal.

CI 191 SC 191.1.1 P 57 L 42 # 5

Ran, Adeo

Cisco Systems

Comment Type E Comment Status D nomenclature

The nomenclature subclause is supposed to explain to the reader what the terms mean. The text here looks like instructions to the editors or contributors.

Also possibly in clause 192.

SuggestedRemedy

Change from

"For all PHYs communicating on a shielded, balanced, pair of conductors, regardless of transmit bit rate, use: MultiG+100M/100M+MultiGBASE-T1"

to

"The term MultiG+100M/100M+MultiGBASE-T1 is used to refer to the PHYs in this clause that communicate on a shielded, balanced, pair of conductors, regardless of transmit bit rate".

Make similar changes to the text describing the other terms.

Implement in clause 192 if appropriate.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

This text is deleted based on comment #281.

See comment #109 for updates to Clause 192.

CI 191 SC 191.1.2 P 59 L 14 # 77

Ran, Adeo

Cisco Systems

Comment Type T Comment Status D PMD

Both stacks in figure 191-2 include a "PMD" box. But these PHYs do not have a PMD sublayer (based on the clause title and lack of a PMD subclause). The -T1 and -V1 are PHYs for different media, and the differences are in the MDI (191.5.2.10 and 191.5.2.11).

There are other mentions of "PMD" in 191.1.3.3 and 191.11.2.1, and in the PICS.

SuggestedRemedy

Delete the PMD boxes and legend item from the figure.

Delete other mentions of PMD from the clause.

Proposed Response Response Status W

PROPOSED ACCEPT.

IEEE P802.3dm D2.0 Asymmetrical Electrical Automotive Ethernet Initial Working Group ballot comments

CI 191 SC 191.1.3 P 61 L 24 # 454

Law, David

HPE

Comment Type E Comment Status D 191_state_diag

Subclause 191.5.2.8.1 'State diagram variables' says sync_link_control is a variable that indicates the data source for the PMA Transmit function. Further, subclause 191.5.2.2 'PMA Transmit function' says, 'During Link Synchronization, when sync_link_control = DISABLE and Auto-Negotiation is either not enabled or is not implemented, the sync_tx_symb output by the PHY Link Synchronization function shall be used in place of tx_symb as the data source for PMA Transmit.'.

Based on this, the output of the PMA TRANSMIT block is controlled by sync_link_control, yet Figures 191-3 'PHY_S functional block diagram', 191-4 'PHY_D functional block diagram', and 191-25 'PMA reference diagram' do not show sync_link_control connected to the PMA TRANSMIT block.

SuggestedRemedy

Add sync_link_control as a connection to the PMA TRANSMIT block in Figures 191-3, 191-4 and 191-25.

Proposed Response Response Status W

PROPOSED ACCEPT.

CI 191 SC 191.1.3.2 P 63 L 25 # 521

Jonsson, Ragnar

Infineon

Comment Type T Comment Status D late-2

The RS-FEC used for both ACT LS and TDD have low correction capability, increasing the probability of uncorrectable error occurrence. For ACT LS we can more reliably detect uncorrectable errors by replacing the "six vendor-specific bits" with a CRC-6 checksum to help detect uncorrectable FEC frames.

SuggestedRemedy

Update the text to replace the "six vendor-specific bits" with a CRC-6 checksum to help detect uncorrectable FEC frames. These changes will propagate through several places in the document and this change will be described in more detail in an accompanying presentation.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Implement the changes shown on slides 3 through 7 of
https://www.ieee802.org/3/dm/public/0726/jonsson_3dm_01_0726.pdf.

CI 191 SC 191.3.2.2 P 76 L 20 # 402

Zimmerman, George

CME Consulting/ADI,Cisco,Eliyan,Infineon,OnSemi,

Comment Type T Comment Status D 191_PCS

The 65B/65B state diagram is not Figure 191-9 or 191-10 - those are the block diagrams and are not required. Figure 191-18 is the 64B/65B state diagram and should be required at this point in the text.

SuggestedRemedy

Change the first paragraph of 191.3.2.2 to read:

The PCS Transmit function shall conform to the PCS 64B/65B Transmit state diagram in Figure 191-18.

The PCS Transmit bit ordering shall conform to Figure 191-11 for a 10G+100MBASE-T1/V1 PHY. For a 5G+100MBASE-T1/V1 or a 2.5GBASE-T1/V1 PHY, the PCS Transmit bit ordering shall conform to Figure 191-12.

Adjust PICS appropriately if added by another comment.

Proposed Response Response Status W

PROPOSED ACCEPT.

CI 191 SC 191.3.2.2 P 79 L 31 # 285

van Dyck, Peter

Infineon

Comment Type E Comment Status D EZ - pull

Figure 191-11: For 10G, a RS-FEC superframe always has L x 1800 PAM4 symbols. A Training frame always has 7200 PAM2 symbols. The training frame symbols match the data path symbols for a case with L=4

SuggestedRemedy

Replace:

RS-FEC superframe (L x 1800 x u symbols)

With:

RS-FEC superframe (L x 1800 symbols) / Training Frame (u x 1800 symbols)

Replace:

For PAM2 path, V=2 and u=2

With:

For PAM2 path, V=2 and u=4

Proposed Response Response Status W

PROPOSED ACCEPT.

IEEE P802.3dm D2.0 Asymmetrical Electrical Automotive Ethernet Initial Working Group ballot comments

CI 191	SC 191.3.2.2	P 80	L 29	# 286
van Dyck, Peter		Infineon		
Comment Type	E	Comment Status	D	EZ - pull
Figure 191-12: For 2.5G and 5G, a RS-FEC superframe always has L x 3600 PAM2 symbols. A Training frame always has 7200 PAM2 symbols. The training frame symbols match the data path symbols for a case with L=2				
SuggestedRemedy				
Replace:				
RS-FEC superframe (L x 1800 x u symbols)				
With:				
RS-FEC superframe (L x 3600 symbols) / Training Frame (7200 symbols)				
Replace:				
For PAM2 path, V=2 and u=2				
With:				
For RS-FEC Frame u=1. For Training Frame u=2.				
Replace:				
PAMVu x 1800-1				
With:				
PAM2u x 3600-1				
Proposed Response	Response Status		W	
PROPOSED ACCEPT.				

CI 191	SC 191.3.2.2	P 81	L 43	# 287
van Dyck, Peter		Infineon		
Comment Type	E	Comment Status	D	EZ - pull
Figure 191-13: Same as comment for Figure 191-11				
SuggestedRemedy				
Replace:				
For PAM2 path, V=2 and u=2				
With:				
For PAM2 path, V=2 and u=4				
Proposed Response	Response Status		W	
PROPOSED ACCEPT.				

CI 191	SC 191.3.2.2	P 82	L 43	# 288
van Dyck, Peter		Infineon		
Comment Type	E	Comment Status	D	EZ - pull
Figure 191-14: Same as comment for Figure 191-12				
SuggestedRemedy				
Replace:				
For PAM2 path, V=2 and u=2. For PAM4 path, V=4 and u=1.				
With:				
For RS-FEC Frame u=1. For Training Frame u=2.				
Replace:				
rx_PAMVn+(u x 1800-1)				
With:				
rx_PAM2n+(u x 3600-1)				
Proposed Response	Response Status		W	
PROPOSED ACCEPT.				

CI 191	SC 191.3.2.2.5	P 79	L 1	# 123
de Koos, Andras		Microchip Technology		
Comment Type	E	Comment Status	D	191_PCS
In figure 191–11, only L=1 is shown (just like in clause 149) . Rather than having to refer to the full explanation of the superframe and interleave depth in clause 149 (where it is still somewhat cryptic), an illustration of how the RS-FEC frames are interleaved into a superframe would be helpful, and would fit well into this diagram.				
Same comment for figures 191–13, 192–6, and 192–13				
SuggestedRemedy				
In figure 191–11 (and similar HS PCS bit ordering diagrams), consider showing the figure with interleave depth L=2 or L=4.				
Proposed Response	Response Status		W	
PROPOSED REJECT.				
The comment does not contain sufficient detail so that the CRG can understand the specific change being suggested by the commenter.				

IEEE P802.3dm D2.0 Asymmetrical Electrical Automotive Ethernet Initial Working Group ballot comments

CI 191 SC 191.3.2.2.5 P 79 L 38 # 361

Lasry, Ariel Qualcomm Technologies, Inc.

Comment Type ER Comment Status D 191_PCS

Figure 191-11 is at the wrong Sub-Clause

SuggestedRemedy

Move to 191.3.2.2.2 line 40

Proposed Response Response Status W

PROPOSED REJECT.

The Figure has the anchor in the correct place; however, FM moves the figures around to reduce white space. This will change as the spec is updated and text is added/deleted. The final location of the Figure will be optimized by the IEEE editorial staff during publication preparation.

CI 191 SC 191.3.2.2.8 P 80 L 37 # 362

Lasry, Ariel Qualcomm Technologies, Inc.

Comment Type ER Comment Status D 191_PCS

Figure 191-12 is at the wrong Sub-clause

SuggestedRemedy

Move to 191.3.2.2.2 after Figure 191-11 from previous comment

Proposed Response Response Status W

PROPOSED REJECT.

The Figure has the anchor in the correct place; however, FM moves the figures around to reduce white space. This will change as the spec is updated and text is added/deleted. The final location of the Figure will be optimized by the IEEE editorial staff during publication preparation.

CI 191 SC 191.3.2.2.12 P 82 L 1 # 122

de Koos, Andras Microchip Technology

Comment Type ER Comment Status D 191_PCS

Placement of figure 191-13 and 191-14 - the receive bit ordering diagrams - is within the transmit function section. Very confusing.

SuggestedRemedy

please move figures 191-13 and 191-14 to the receive function section.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD. The Figures are included where they are mentioned first.

CI 191 SC 191.3.2.2.14 P 83 L 24 # 147

Wienckowski, Natalie IVN Solutions LLC; Ethernovia & Bosch

Comment Type T Comment Status D 191_PCS

Reference to 149.3.2.2.15 needs to be replaced with text to refer to specific Clause 191 requirements.

SuggestedRemedy

Copy in text from 149.3.2.2.15 replacing 149.4.2.4.5 with 191.5.2.4.5.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by #413.

CI 191 SC 191.3.2.2.14 P 83 L 24 # 367

Lasry, Ariel Qualcomm Technologies, Inc.

Comment Type ER Comment Status D 191_PCS

The referenced Sub-clause 149.3.2.2.15 is referencing the InterleaverDepth from 149.4.2.4.5 where only 1 PHY Capability bits is specified. For Clause 191 there are 2 PHY capabilities one for the HS_PATH one for the LS_PATH. The Sub-clause also mentions specific PHYs for 802.3ch which are not relevant to Clause 191

SuggestedRemedy

Replace line 24 with text from 149.3.2.2.15 and replace the reference 149.4.2.4.5 with 191.5.2.4.5. And replace the 3 listed .3ch PHYs with the corresponding Clause 191 PHYs.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by #413.

IEEE P802.3dm D2.0 Asymmetrical Electrical Automotive Ethernet Initial Working Group ballot comments

Cl	191	SC	191.3.2.2.19	P	84	L	9	#	80
Ran, Adeo				Cisco Systems					
Comment Type	T	Comment Status				D	191_PCS		
"An implementation of side-stream scramblers by linear-feedback shift registers is shown in Figure 149–11" Figure 149-11 shows two scramblers and uses the labels MASTER and SLAVE to distinguish them. But these terms are not used in 802.3dm. If a reference to content in clause 149 is used, it should state which one is used. Based on equation 191-2, which has the same polynomial as equation 149-6, it is the "MASTER" one Also in 191.4.2.2.16, but there it is the MASTER polynomial. The suggested remedy is to point back to the respective polynomial equations in clause 149. Alternatively the equations can be retained, but the reference to figure 149-11 should be specific. <i>SuggestedRemedy</i> Replace the first paragraph of 191.3.2.2.19, equation 191-2, and the quoted sentence by the following: "The PHY_S PCS Transmit function shall employ side-stream scrambling using the generator polynomial specified in Equation (149-6) for both LEADER and FOLLOWER PHY configurations. An implementation of the side-stream scrambler by a linear-feedback shift register is shown in the bottom part of Figure 149–11 (labeled SLAVE PHY)." Implement corresponding changes in 191.4.2.2.16 (using equation 149-5 and MASTER PHY).									
Proposed Response		Response Status		W					
PROPOSED ACCEPT IN PRINCIPLE.									
See #378									

Cl 191	SC 191.3.2.3	P 85	L 15	# 125
de Koos, Andras		Microchip Technology		
Comment Type	TR	Comment Status	D	training
How to synchronize the Rx descrambler state to that of the Tx (during training frames) is not spelled out.				
"During PMA training mode, PCS Receive checks the received PAM2 framing and indicates the reliable acquisition of the PCS descrambler state by setting the scr_status parameter of the PMA_SCRSTATUS.request primitive to OK."				
What does "reliable" mean?? how reliable is reliable enough? Needs a definition!				
This is likely the same language and verbosity as similar clauses, but it would be beneficial for the standard to have a well-defined scrambler-state synchronization method.				
Same comment for 192.3.2.3				
SuggestedRemedy				
consider adding an explicit method (state machine) for the scrambler state sync.				
Proposed Response		Response Status W		
PROPOSED REJECT.				
The comment does not contain sufficient detail so that the CRG can understand the specific change being suggested by the commenter.				

Cl 191	SC 191.3.2.3.3	P 86	L 16	# 276
Jonsson, Ragnar		Infineon		
Comment Type	E	Comment Status	D	EZ - pull
There should be a SHALL statement in "The R_BLOCK_TYPE of an invalid block is set to E."				
SuggestedRemedy				
Change to "The R_BLOCK_TYPE of an invalid block shall be set to E."				
Proposed Response		Response Status W		
PROPOSED ACCEPT IN PRINCIPLE.				
Also update proposed PICS as appropriate.				

IEEE P802.3dm D2.0 Asymmetrical Electrical Automotive Ethernet Initial Working Group ballot comments

CI 191 SC 191.3.3 P 86 L 21 # 417

Zimmerman, George CME Consulting/ADI,Cisco,Eliyan,Infineon,OnSemi,

Comment Type T Comment Status D 191_tests

149.3.3 Test pattern generators has requirements in it. Further, those requirements relate to the bit ordering figures in clause 149, which are only valid for 10 Gb/s and not for 2.5 Gb/s and 5 Gb/s. This section needs reworking to be simpler - better to bring it in.

SuggestedRemedy

Replace "As specified in 149.3.3." with
 "The test-pattern generator mode is provided for enabling joint testing of the local transmitter, the channel, and remote receiver. When the transmit PCS is operating in test-pattern mode it shall transmit continuously according to the appropriate rate's transmit bit ordering diagram (Figure 191-11 or Figure 191-12), with the input to the RS-FEC encoder set to zero and the initial condition of the scrambler set to any non-zero value. This has the same effect as setting the input to the scrambler to zero.
 When the receiver PCS is operating in test-pattern mode it shall receive continuously according to the appropriate rate's receive bit ordering diagram (Figure 191-13 or Figure 191-14). The output of the received descrambled values should be zero. Any nonzero values correspond to receiver bit errors. The output of the RS-FEC decoder should also be zero; however, there is the possibility that the RS-FEC decoder corrected some errors. This mode is further described as test mode 7 in 191.1.6."
 Insert PICS duplicating PICS TPG1, with status PHY_S: M, and TPG2, with status PHY_D: M.

Proposed Response Response Status W

PROPOSED ACCEPT.

CI 191 SC 191.3.5.1.3 P 88 L 25 # 214

Slavick, Jeff Broadcom

Comment Type TR Comment Status D variables

rfer_timer_done is not used anywhere and automatically exists per 14.2.3.2

SuggestedRemedy

Remove "When the timer reaches its terminal count, rfer_timer_done = TRUE."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

This is on P89L25.

This text is deleted by #52.

CI 191 SC 191.3.5.1.3 P 88 L 25 # 216

Slavick, Jeff Broadcom

Comment Type TR Comment Status D variables

rfer_timer is not used within Clause 191, why is it here?

SuggestedRemedy

Move rfer_timer to Clause 192.3.5.x

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by #52.

CI 191 SC 191.3.5.1.3 P 89 L 22 # 52

Muma, Scott Microchip

Comment Type E Comment Status D variables

rfer_timer is the only timer defined and is never used, so the Timers section and subsections can be deleted.

SuggestedRemedy

Delete section 191.3.5.1.3 and rfer_timer definition.

Proposed Response Response Status W

PROPOSED ACCEPT.

CI 191 SC 191.3.5.1.4 P 90 L 39 # 520

Muma, Scott Microchip Technology Inc.

Comment Type E Comment Status D late-2

T_TYPE_NEXT is defined but never used

SuggestedRemedy

Delete text lines 39-41: T_TYPE_NEXT
 Prescient end of packet check function. It returns the T_BLOCK_TYPE of the tx_raw vector immediately following the current tx_raw vector.

Proposed Response Response Status W

PROPOSED ACCEPT.

IEEE P802.3dm D2.0 Asymmetrical Electrical Automotive Ethernet Initial Working Group ballot comments

CI 191 SC 191.3.7 P 95 L 38 # 421
 Zimmerman, George CME Consulting/ADI,Cisco,Eliyan,Infineon,OnSemi,
 Comment Type T Comment Status D EZ - pull
 The OAM behavior in 149.3.9 (including state diagrams Figure 149-24 and Figure 149-25) are not pulled in as requirements. They should be.
 SuggestedRemedy
 Change P95 L38 from "behavior is defined in 149.3.9" to "behavior shall be as defined in 149.3.9" add PICS as appropriate (see PICS comment)
 Proposed Response Response Status W
 PROPOSED ACCEPT.

CI 191 SC 191.3.7.2 P 96 L 1 # 420
 Zimmerman, George CME Consulting/ADI,Cisco,Eliyan,Infineon,OnSemi,
 Comment Type T Comment Status D EZ - pull
 The OAM functions in 149.3.9.2 are not pulled in with requirement language. Further, the exceptions, are not only in 191.3.7.2.1, but are also in .2 (PHY Health) and .3 (PHY health indicator).
 After requiring 191.3.7.2.1, there will be duplicate shalls...
 SuggestedRemedy
 Change 191.3.7.2 to from : "MultiG+100MBASE-T1/V1 OAM functions are the same as those defined for a MultiGBASE-T1 PHY in 149.3.9.2 with the exception that the MultiG+100MBASE-T1/V1 OAM frame structure, PHY health, and PHY health indicator are defined in 191.3.7.2.1."
 to: "MultiG+100MBASE-T1/V1 OAM functions shall be as defined for a MultiGBASE-T1 PHY in 149.3.9.2 with the exception that the MultiG+100MBASE-T1/V1 OAM frame structure, PHY health, and PHY health indicator are defined in 191.3.7.2.1, 191.3.7.2.2, and 191.3.7.2.3, respectively."
 Add pics reflecting sections of 149 and 191.3.7.2.2
 Change "the first symbol (OAM<0>) shall be" to "the first symbol (OAM<0>) is" at P96 L21 (4th para 191.3.7.2.1)
 Change "10-bit OAM field shall be set to all 0's" to "10-bit OAM field is set to all 0's." at P96 L31 (last para 191.3.7.2.1)
 Proposed Response Response Status W
 PROPOSED ACCEPT.

CI 191 SC 191.4.2.2.1 P 99 L 1 # 55
 Ran, Adeo Cisco Systems
 Comment Type T Comment Status D common
 The 64B65B coding for LS_PATH seems identical to that of the HS_PATH in 192.3.2.2.1 and subsequent subclauses. If it's different, it would help the reader if the differences were stated instead of repeating everything.
 SuggestedRemedy
 Replace whatever is redundant with references to the parallel content in 191.3.2.2, listing exceptions if they exist.
 Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.

TFTD if references between 191 and 192 are desired, if these should stand alone, or both should refer to 149.

CI 191 SC 191.4.4 P 106 L 1 # 57
 Ran, Adeo Cisco Systems
 Comment Type T Comment Status D 191_PCS_LS
 Equation 191-9 has no indexing of Infocfield, OAM, "6bit v-s", Parity - are these constants or scalars that do not need indexing?
 SuggestedRemedy
 Change to Infocfield(n-195), OAM(n-260), v-s(n-270), Parity(n-276)
 Proposed Response Response Status W
 PROPOSED ACCEPT.

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CI 191 SC 191.5.2.2 P 109 L 10 # 9

Ran, Adeel

Cisco Systems

Comment Type T Comment Status D 191_PMA

"The PMA Transmit function comprises a transmitter to generate a four-level modulated signal for PAM4, a two-level modulated signal for PAM2, both for HS_TX, and a DME modulated signal for LS_TX "

This reads as if all components are required for a PMA transmit function. But implementations can have either an HS_TX or a LS_TX, not necessarily both, and in the case of HS_TX, it does not necessarily need PAM4.

Also possibly in clause 192.

SuggestedRemedy

Rewrite this sentence to make the PMA transmit function dependent on the specific PHY type.

Implement in clause 192 if appropriate.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change: The PMA Transmit function comprises a transmitter to generate a four-level modulated signal for PAM4, a two-level modulated signal for PAM2, both for HS_TX, and a DME modulated signal for LS_TX

To: The HS_TX PMA Transmit function comprises a transmitter to generate a two-level PAM2 signal for 2.5 Gb/s and 5 Gb/s and a four-level PAM4 signal for 10Gb/s. The LS_TX PMA Transmit function generates a DME modulated signal."

This does not apply to 192.

CI 191 SC 191.5.2.2 P 110 L 18 # 516

Razavi, Alireza

Eliyan

Comment Type T Comment Status D late - 191_PHY_Cntrl

When Auto-Negotiation is bypassed or undefined, neither PHY can identify the remote PHY vendor, so the VendorSpecificData bits (Oct8/9, 191.5.2.4.5) of the HS_PATH Infofield may be interpreted differently by different vendors, creating an interoperability risk.

SuggestedRemedy

Move OAMen to octet 7, and use octet 8,9, and 10 for 24 bits OUI
P112, L1 : change Message Field to Message Field and PHY capability bits
P112, L21: bring the definition of OAMen to this line
P112, L22, L33 : convert the first reserved bit to OAMen
P112, L42 : rename section 191.5.2.5.6 to Organizationally Unique Identifier
[Oct8 = OUI[7:0], Oct9 = OUI[15:8], Oct10 = OUI[23:16]] contains Organizationally Unique Identifier (OUI).

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

CI 191 SC 191.5.2.4 P 111 L 2 # 153

Wienckowski, Natalie

IVN Solutions LLC; Ethernovia & Bosch

Comment Type E Comment Status D 191_PMA

There is not always a PAM2 to PAM4 transition when completing training,

SuggestedRemedy

Change: PAM2 to PAM4 transition.
To: PCS_TEST to PCS_DATA transition.

Proposed Response Response Status W

PROPOSED ACCEPT.

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CI 191 SC 191.5.2.4.4 P 112 L 4 # 500

Razavi, Alireza

Eliyan

Comment Type E Comment Status D late - 191_PHY_Cntrl

The Message Field uses the bit timing_lock_OK for the FOLLOWER (Oct7<4>), but timing_lock_OK is not defined as a state diagram variable in 191.5.2.6.1 and does not appear in the PHY Control state diagram (Figure 191-31) .

SuggestedRemedy

timing_lock_OK bit does not carry any information. replace timing_lock_OK bit with a reserved bit

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

It may be useful to convey this bit especially if the follower is crystal-less and for some reason loses timing lock during training.

Proposed text to address this:

Insert text in 191.5.2.6 (page 116) after line 28.

Whenever a Follower loses the Leader's timing reference it sets timing_lock_OK=0, which is communicated to the link partner via the InfoField. Otherwise, timing_lock_OK is set to 1.

-OR-

Upon entering TRAINING state the Follower initially sets timing_lock_OK = 0 until it has acquired timing lock at which point the Follower sets timing_lock_OK = 1.

CI 191 SC 191.5.2.4.5 P 113 L 1 # 368

Lasry, Ariel

Qualcomm Technologies, Inc.

Comment Type TR Comment Status D 191_Infofields

Table 191-7 should show the fields described on lines 48, 49 of page 112.

It seems that the content of this table should be swapped with the content of Table 191-10.

SuggestedRemedy

Replace Table-191-7 with the content of Table 191-10 and add ",HS_PATH" to the table title

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change the title of Table 191-7 to:

PHY control bits, HS_PATH

Change title of 191.4.2.4.5 to:

PHY control bits, HS_PATH

Add as a new first sentence in 191.5.2.4.5

The HS_PATH PHY control bits are sent by PHY_D to PHY_S on the LS_PATH to control the transmitter settings on the HS_PATH.

CI 191 SC 191.5.2.4.7 P 113 L 28 # 292

van Dyck, Peter

Infineon

Comment Type E Comment Status D EZ - pull

"149.4.2.4.7 Reserved fields" section is missing in Clause 191.

SuggestedRemedy

Move 191.5.2.4.8 to 191.5.2.4.9, move 191.5.2.4.7 to 191.5.2.4.8, add new section 191.5.2.4.7 with the text from 149.4.2.4.7

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

This is already defined in 191.5.2.5.1.

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CI 191 SC 191.5.2.5 P 114 L 39 # 515

Razavi, Alireza

Eliyan

Comment Type T Comment Status D late - 191_PHY_Cntrl

When Auto-Negotiation is bypassed or undefined, neither PHY can identify the remote PHY vendor, so the VendorSpecificData bits (Oct6/7, 191.5.2.5.4) of the LS_PATH Infofield may be interpreted differently by different vendors, creating an interoperability risk.

SuggestedRemedy

Redefine Oct2/3/4 of the LS_PATH Infofield as a 24-bit Organizationally Unique Identifier (OUI):
P114, L 30 : replace "reserved " with Organizationally Unique Identifier
P116, L 3 : rename section 191.5.2.5.6 with Organizationally Unique Identifier
[Oct2 = OUI[7:0], Oct3 = OUI[15:8], Oct4 = OUI[23:16]] contains Organizationally Unique Identifier (OUI). The OUI is a 24-bit organization identifier assigned by the IEEE Registration Authority.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

CI 191 SC 191.5.2.5.1 P 114 L # 429

Zimmerman, George

CME Consulting/ADI,Cisco,Eliyan,Infineon,OnSemi,

Comment Type E Comment Status D 191_Infofields

Since infofield notation is the same for both, don't repeat it. It could get changed and be confusing....

SuggestedRemedy

Replace content of 191.5.2.5.1 with "See 191.5.2.4.1."

Proposed Response Response Status W

PROPOSED REJECT.

This is not much text so why make the reader jump around.

CI 191 SC 191.5.2.5.4 P 115 L 30 # 369

Lasry, Ariel

Qualcomm Technologies, Inc.

Comment Type TR Comment Status D 191_Infofields

Table 191-10 has fields for InterleaverDepth and PrecodeSel. However, there is no FEC interleaving and no PreCoder on the LS_PATH.

SuggestedRemedy

Table 191-10: bits 1,2,3 and 4 should be changed to Reserved.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change the title of Table 191-10 to:

PHY control bits, LS_PATH

Change title of 191.4.2.5.4 to:

PHY control bits, LS_PATH

Add as a new first sentence in 191.5.2.4.5

The LS_PATH PHY control bits are sent by PHY_S to PHY_D on the HS_PATH to control the transmitter settings on the LS_PATH.

CI 191 SC 191.5.2.5.4 P 115 L 44 # 370

Lasry, Ariel

Qualcomm Technologies, Inc.

Comment Type TR Comment Status D 191_Infofields

Delete "Oct8<2:1> = InterleaverDepth[1:0], Oct8<4:3> = PrecodeSel[1:0]," as there is no FEC interleaving and no precoder on the LS_PATH

SuggestedRemedy

See comment

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

See #369 which clarifies this.

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Cl 191 SC 191.5.2.5.4 P 115 L 50 # 373

Lasry, Ariel Qualcomm Technologies, Inc.

Comment Type TR Comment Status D 191_Infocfields

Remove the sentence "InterleaverDepth indicates the requested data mode interleaving depth. PrecoderSel indicates the requested precoder, available for 10G only." As there is no 10G on the LS_PATH

SuggestedRemedy
see comment

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

See #369 which clarifies this.

Cl 191 SC 191.5.2.6 P 116 L 29 # 432

Zimmerman, George CME Consulting/ADI,Cisco,Eliyan,Infineon,OnSemi,

Comment Type T Comment Status D 191_PHY_Cntrl

It appears that Table 191-11 is simply informational, and is a consequence of the PHY control state diagram. If so, it should not have a shall.

SuggestedRemedy
Consider wheter Tables 191-11 and 191-12 have requirements or are simply informational. If they have requirments,incorporate them into the PHY control state diagram. If not, change"shall comply with" to "is shown in" at P116 L29

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

Cl 191 SC 191.5.2.6.3 P 120 L 47 # 462

Law, David HPE

Comment Type TR Comment Status D 191_PHY_Cntrl

Figure 191–31 'PHY Control state diagram' in the PMA uses the hi_rfer and block_lock variables, yet these variables are not defined in subclause 191.5.2.6.1 'State diagram variables'. The hi_rfer and block_lock variables are generated in the PCS, with the hi_rfer variable generated in Figure 191–17 'RFER monitor state diagram', and the block_lock generated in subclause 191.4.2.3 PCS 'Receive function'. As a result, these variables pass across the PMA Service interface, yet they are not parameters of any of the primitives defined in subclause 191.2.2 'PMA service interface'. Further, they are not illustrated in Figure 191–3 'PHY_S functional block diagram', Figure 191–4 'PHY_D functional block diagram', Figure 191–7 'PHY_S 'PCS reference diagram', Figure 191–8 'PHY_D PCS reference diagram', and Figure 191–25 'PMA reference diagram'.

SuggestedRemedy

[1] Add the following to the list of primitives in subclause 191.2.2 'PMA service interface':

PMA_PCSSYNC.request(block_lock, rfer_cnt)

[2] Add an arrow labelled 'PMA_PCSSYNC.request' from the PHY_S PCS to PHY_S PMA block in Figure 191–5 'PHY_S service interfaces' in Figure 191–5 'PHY_S service interfaces' and Figure 191–6 'PHY_D service interfaces'.

[3] Add the following new subclauses to subclause 191.2.2:

191.2.2.X PMA_PCSSYNC.request

191.2.2.X.1 Semantics of the primitive

PMA_PCSSYNC.request(block_lock, rfer_cnt)

The PMA_PCSSYNC.request primitive passes the block_lock and rfer_cnt parameters from the PCS to the PMA.

The parameter block_lock can take on one of the following two values of the form:

TRUE The PCS Synchronization process has acquired block delineation.
FALSE The PCS Synchronization process has not acquired block delineation.

The parameter rfer_cnt can take on one of the following two values of the form:

TRUE The PCS Synchronization has detected 16 errors in one RFRX_CNT_LIMIT interval.
FALSE The PCS Synchronization has not detected 16 errors in one RFRX_CNT_LIMIT interval.

191.2.2.X.2 When generated

The PCS generates PMA_PCSSYNC.request messages to indicate a change in block_lock

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or rfer_cnt.

191.2.2.X.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 191–31.

[4] Add block_lock and rfer_cnt to figures 191–3, 191–4, 191–7, 191–8 and 191–25.

[5] Add the following variables to subclause 191.5.2.6.1 'State diagram variables':

block_lock

Boolean variable that is set TRUE by the PCS Synchronization process when it acquires block delineation. It is passed to the PMA via the block_lock parameter of the PMA_PCSSYNC.request primitive.

hi_rfer

Boolean variable that is set TRUE by the PCS Synchronization process when the rfer_cnt reaches 16 errors in one RFRX_CNT_LIMIT interval. It is passed to the PMA via the rfer_cnt parameter of the PMA_PCSSYNC.request primitive.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT.

Maintenance requests may be needed for 149 and 165 as they have the same issue.

<i>Cl</i> 191	<i>SC</i> 191.5.2.8.1	<i>P</i> 124	<i>L</i> 4	<i>#</i> 280
Jonsson, Ragnar		Infineon		
<i>Comment Type</i>	TR	<i>Comment Status</i>	D	<i>191_link_sync</i>

Incorrect condition for FALSE state

SuggestedRemedy

Change "At least one SEND_S pulse" to "At least three SEND_S pulses".

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

TFTD. There was discussion on this in March and May.

<i>Cl</i> 191	<i>SC</i> 191.5.2.8.4	<i>P</i> 126	<i>L</i> 42	<i>#</i> 465
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Law, David

HPE

Comment Type **T** *Comment Status* **D** *191_link_sync*

Figure 191–35 'PHY Link Synchronization state diagram' uses the training_failure variable in the transition from the LINK_GOOD_CHECK state to the TRANSMIT_DISABLE state. However, the training_failure variable is not defined in subclause 191.5.2.8.1 'State diagram variables'.

SuggestedRemedy

Add the following to subclause 191.5.2.8.1:

training_failure

A Boolean variable indicating whether PHY Control has resulted in a successful training.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

This is defined in 191.5.2.6.1.

On P124L26

Add: training_failure:
see 191.5.2.6.1.

<i>Cl</i> 191	<i>SC</i> 191.5.6.1	<i>P</i> 128	<i>L</i> 47	<i>#</i> 436
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Zimmerman, George

CME Consulting/ADI,Cisco,Eliyan,Infineon,OnSemi,

Comment Type **E** *Comment Status* **D** *191_tests*

The text says Test mode 2 transmits JP03A or JP03B, we need to know which one is transmitted. That doesn't appear until several pages later, and leads to confusion. (Table 191-15).

SuggestedRemedy

Consider whether a separate test mode is needed for each pattern or else add text indicating how the pattern is selected. If it is implementer's choice, add, "See Table 191-15 for control of jitter test modes." after "from its local clock source." (before discussion of PAM2 at P128 L48)

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

add, "See Table 191-15 for control of jitter test modes." after "from its local clock source." (before discussion of PAM2 at P128 L48)

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CI 191 SC 191.6.2.4 P 133 L 32 # 441
 Zimmerman, George CME Consulting/ADI,Cisco,Eliyan,Infineon,OnSemi,
 Comment Type T Comment Status D 191_tests
 A rate of 5625xS MHz would only apply to PHY_S transmitting, and 5625/48 MHz for a PHY_D transmitting, yet this spec is divided on leader and follower...
SuggestedRemedy
 Change the frequency for the follower PHY from 5625/48 MHz +/-20%" to "5625 x S MHz +/- 100 ppm. See Table 191-1 for definition of S."
Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 TFTD
 Should we add 100 Mb/s to Table 191-1, change it to 117.1875 or keep it as is?

CI 191 SC 191.6.2.5 P 133 L 42 # 295
 Sakunia, Saket Infineon
 Comment Type T Comment Status D 191_tests
 802.3dm PSD mask allows for a a low-frequency high-pass filtering that produces baseline wander outside the usual impulse-response window. Without compensation, this baseline energy is counted as distortion/noise, depressing SNDR and degrading inter-lab correlation. The proposed subclause adds a narrowly scoped, LTI compensation step in Clause 201—without modifying 120D.3.1.2—restoring accuracy and repeatability while preserving test modes, fixtures, and limits.
SuggestedRemedy
 With the transmitter in test mode 4, transmitting in MultiG mode, and using the transmitter test fixture 1 shown in Figure 191–36 for -T1 and Figure 191–37 for -V1, the test defined in 120D.3.1.2 shall be performed. "Annex191B describes additional High Pass Filter to be applied to the measured data when the DUT includes any low frequency high pass filtering (e.g. PoC/PoDL)"
Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 Add additional text shown in "" in suggested remedy.
 Add Normative Annex 191 B shown in
https://www.ieee802.org/3/dm/public/0726/Proposed_Annex_191B.pdf.

CI 191 SC 191.7.2.2 P 139 L 24 # 445
 Zimmerman, George CME Consulting/ADI,Cisco,Eliyan,Infineon,OnSemi,
 Comment Type T Comment Status D 191_tests
 191.7.2.1 and 191.7.2.2 define jitter for the phy transmitting 100 Mb/s. However, the jitter spec on lines 23 and 24 reference the value of J in Table 191-14. (similarly on lines 44 and 45) There is no value of J in 191-14 for a 100M+xBASE-T PHY. As a starting point consider whether a PHY_D as leader (which is what this spec is on) it should have the same jitter spec as the equivalent PHY_S.
SuggestedRemedy
 Add to the end of the 1st paragraph of 191.7.2.1 (after "for the definition of J."), "For an LS transmitter as Leader, use J for the equivalent HS transmitter on its partner PHY_S in Table 191-14."
 Add the same sentence after "for the definition of J." in 191.7.2.2 (middle of the paragraph, P139 L44)

Proposed Response Response Status W
 PROPOSED ACCEPT.

CI 191 SC 191.7.2.4 P 140 L 5 # 446
 Zimmerman, George CME Consulting/ADI,Cisco,Eliyan,Infineon,OnSemi,
 Comment Type T Comment Status D 191_tests
 There is only a spec for the low speed transmitter as leader, there needs to be one as follower - there appears to be a specification for that in the high speed section.
SuggestedRemedy
 Add the following, base on the second paragraph of 191.6.2.4 to 191.7.2.4. Add PICS (TES_LS1 shown in the PICS comment) for this.
 New paragraph added to 191.7.2.4 is: "In test mode 2 and using test fixture 3 as shown in Figure 191–39 for -T1 and Figure 191–40 for -V1, the symbol transmission rate of the FOLLOWER PHY, when running off of a free-running clock, shall be within the range 5625/48 MHz +/-20%.
 The short-term rate of frequency variation for both leader and follower shall be less than 1% / second."

Proposed Response Response Status W
 PROPOSED ACCEPT.

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CI 191 SC 191.14 P 153 L 45 # 13

Ran, Adeo

Cisco Systems

Comment Type T Comment Status D 191_delay

The delay constraints are given in terms of HS_PATH delay and LS_PATH delay, but the way these are defined is a sum of delay in the transmitter and the receiver of the same rate - and these are in two different devices, which are different PHY types and possibly from different vendors. The "shall" statement addressing the delays cannot be fulfilled or verified by a single vendor. No vendor can claim compliance to such a "shared" requirement.

Other Base-T PHYs have either defined the requirement using the sum of the transmit and receive delays of a specific implementation (e.g. 55.11, 97.10, and 149.10) or specified separate delays for the transmit and receive path (e.g. 40.11 and 96.10).

In this case it seems that the latter option is preferable because loopback is not possible so the delays must be measured separately anyway. But specifying the sum on the delays of a specific implementation would still be acceptable.

Annex 191A provides recommendations but it is informative, and does not solve the problem that the specification is split between two vendors.

Also possibly in clause 192.

SuggestedRemedy

Change the delay constraints to either of the following:

- Separate transmit delay and receive delay maximum values for a specific implementations, splitting the budget e.g. according to the recommendations in Annex 191A (preferred)
- Sum of transmit delay and receive delay for a specific implementation.

Implement in clause 192 if appropriate.

Proposed Response Response Status W

PROPOSED REJECT.

TFTD

CI 191 SC 191.15 P 156 L 45 # 86

Lusted, Kent

Synopsys

Comment Type TR Comment Status D PICS

PICS entries for 192.15.3, 192.15.4.1, and 192.15.4.2 are incomplete

SuggestedRemedy

Complete PIC entries

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by #448.

CI 191 SC 191.15.3 P 156 L 45 # 283

Jones, Peter

Cisco Systems

Comment Type TR Comment Status D PICS

PICS are missing.

SuggestedRemedy

Complete PICS

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by #448.

CI 191 SC 191.15.3 P 156 L 46 # 15

Ran, Adeo

Cisco Systems

Comment Type E Comment Status D PICS

PICS tables are empty

Also possibly in clause 192.

SuggestedRemedy

Populate them.

Implement in clause 192 if appropriate.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by #448.

CI 191 SC 191.15.3 P 156 L 46 # 119

Kim, Yong

General Motors

Comment Type TR Comment Status D PICS

This sub-clause on, PICS Profoma is incomplete. Please complete.

SuggestedRemedy

Please complete.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by #448.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general

COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed U/unsatisfied Z/withdrawn

SORT ORDER: Clause, Subclause, page, line

CI 191
SC 191.15.3

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CI 191A SC 191A P 253 L 25 # 135

Turner, Max Ethernovia

Comment Type TR Comment Status D 191A

get rid of the "frame or superframe" wording in the Figure, in lines 12, 15 and 17, as well as in the last paragraph

As per page 162 of the draft

"The RS-FEC output superframe consists of $L \times 3600$ bits"

I.e. for $L=1$ the superframe consists of a single frame – superframe is always correct, "frame or superframe" is ambiguous, as this will not work for the 3rd frame in an $L=4$ superframe.

So we can always just use "superframe"

SuggestedRemedy

Replace last paragraph: Due to potential interleaving only the XGMII transfer $X(n)$ encoded into the first 64B/65B block of an RS-FEC superframe (identical to the RS-FEC frame for $L=1$, per 202.3.2.2.14) can practically be used to define the delay between XGMII and MDI (or vice versa). As this is not accessible easily, it is recommended for the PHY implementers to specify TX delay and RX delay in the product's documentation and keep their variation low.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

CI 192 SC 192 P 158 L 1 # 453

RAJAGOPAL, KARTHIK TEXAS INSTRUMENTS INC

Comment Type TR Comment Status D consensus

The draft as looked at an IEEE standard to facilitate interoperability fails to offer a clear implementation guide with more than 1 type of implementation/standard to choose from. Sections 191 and 192 with their widely different PCS & PMA layers fails to fulfil the primary goal which is to be a standard. This would not qualify as standard if users are free to choose from multiple implementations which tries to achieve the same function.

SuggestedRemedy

Rather than letting users guess or arbitrarily choose 1 of the 2 types of PCS & PMA implementation, a technically superior implementation needs to be selected and made as a standard with clear guideline on the PCS and PMA layers. This way facilitates maximum interoperability, which is the only path for this draft to be considered as an IEEE standard

Proposed Response Response Status W

PROPOSED REJECT.

The PHYs in Clause 191 and Clause 192 meet different approved objectives found in https://ieee802.org/3/dm/public/0326/Objectives_ISAAC_01_0326.pdf. The comment does not contain sufficient detail so that the CRG can understand the specific change being suggested by the commenter.

CI 192 SC 192 P 158 L 1 # 331

Pal, Debajyoti Onsemi

Comment Type TR Comment Status D 1G

Support for a 1 Gbps Mode in Low Speed Direction to be used with 5 Gbps and 7.5 Gbps Modes in the HS direction for the TDD PHY must be included.

SuggestedRemedy

The 1 Gbps mode support should be added according to the proposal made in https://www.ieee802.org/3/dm/public/adhoc/060226/chini_3dm_02a_D2d0_1G_comments-preview.pdf

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #358.

CI 192 SC 192 P 158 L 1 # 240

Ahuja, Ramanjit Onsemi

Comment Type TR Comment Status D 1G

Support for a 1 Gbps Mode in Low Speed Direction to be used with 5 Gbps and 7.5 Gbps Modes in the HS direction for the TDD PHY must be included.

SuggestedRemedy

The 1 Gbps mode support should be added according to the proposal made in https://www.ieee802.org/3/dm/public/adhoc/060226/chini_3dm_02a_D2d0_1G_comments-preview.pdf

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #358.

CI 192 SC 192 P 158 L 1 # 239

Ahuja, Ramanjit Onsemi

Comment Type TR Comment Status D 7.5G

Support for a 7.5 Gbps Mode for the High Speed Direction in TDD PHY must be included.

SuggestedRemedy

The 7.5Gbps mode support should be added according to the proposal made in https://www.ieee802.org/3/dm/public/adhoc/060226/gorshe_3dm_02a_D2d0_7d5G-comments.pdf

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #357.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general

COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed U/unsatisfied Z/withdrawn

SORT ORDER: Clause, Subclause, page, line

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CI 192 SC 192 P 158 L 1 # 330

Pal, Debajyoti Onsemi

Comment Type TR Comment Status D 7.5G

Support for a 7.5 Gbps Mode for the High Speed Direction in TDD PHY must be included.

SuggestedRemedy

The 7.5Gbps mode support should be added according to the proposal made in https://www.ieee802.org/3/dm/public/adhoc/060226/gorshe_3dm_02a_D2d0_7d5G-comments.pdf

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #357.

CI 192 SC 192 P 158 L 1 # 491

Zerna, Conrad NXP

Comment Type TR Comment Status D 7.5G

Proposed speed of 7.5Gbps is not included in the draft

SuggestedRemedy

Add proposed highlights from https://www.ieee802.org/3/dm/public/adhoc/060226/gorshe_3dm_02a_D2d0_7d5G-comments.pdf into the draft

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #357.

CI 192 SC 192 P 158 L 1 # 492

Zerna, Conrad NXP

Comment Type TR Comment Status D 1G

Proposed speed of 1Gbps is not included in the draft

SuggestedRemedy

Add proposed green highlights from https://www.ieee802.org/3/dm/public/adhoc/060226/chini_3dm_02a_D2d0_1G_comments-preview.pdf into the draft

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #358.

CI 192 SC 192.1 P 158 L 22 # 165

Wienckowski, Natalie IVN Solutions LLC; Ethernovia & Bosch

Comment Type E Comment Status D EZ - pull

typo

SuggestedRemedy

Change: 64/65B To: 64B/65B

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Also correct on P188L43.

Editorial license to adjust for any other similar errors.

CI 192 SC 192.1 P 158 L 28 # 450

Ganesan, Aravind Texas Instruments

Comment Type TR Comment Status D 192_overview

The paragraph talks about the timing operations at the follower. it is expected that the follower locks on to the leader clock. The accuracy requirement of the lock and holdover quality of the leader clock is not mentioned.

SuggestedRemedy

The accuracy requirement of the clock lock and holdover performance of the follower needs to be mentioned.

Proposed Response Response Status W

PROPOSED REJECT.

This topic is covered by the information in:
192.5.2.6 Transmitter clock frequency
192.5.2.3 Transmitter timing jitter and jitter at the MDI
192.4.2.4.11 Startup sequence

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CI 192 SC 192.1 P 158 L 28 # 451

Ganesan, Aravind

Texas Instruments

Comment Type T Comment Status D 192_overview

In multi lane operation does the PHY_D synchronize all the TDD slots?

SuggestedRemedy

The recommendation for TDD slots synchronisation multi lane operation can be given.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

Proposed remedy for discussion:

Insert the following new paragraph on P158,L33:

"A device that supports multiple simultaneous MultiGBASE-A PHYs may choose to align the start time of its transmit TDD cycle across links operating as the LEADER to reduce crosstalk. Such an alignment is optional and implementation specific."

CI 192 SC 192.1 P 158 L 30 # 238

Chandrasekhar Sriram

Comment Type T Comment Status D 192_overview

The draft suggests that the FOLLOWER phy recovers the clock from the received signal, but this clock is not available during time when LEADER's transmit is switched off (as part of time duplexing). Moreover since the time duration of the LEADER's transmit/FOLLOWER's receive is much less than FOLLOWER's transmit, I believe this implementation will lead to a very complicated CDR to deal with clock drifts.

SuggestedRemedy

Suggest scraping this LEADER/FOLLOWER concept for TDD or give an option to the implementer to use an independent clock source for the FOLLOWER.

Proposed Response Response Status W

PROPOSED REJECT.

Eliminating the LEADER/FOLLOWER concept runs counter to the crystal-less objective.

CI 192 SC 192.1.1 P 159 L 1 # 109

Huber, Thomas

Nokia

Comment Type E Comment Status D Editorial

The wording for the aggregate terminology below the figure is a bit awkward: "When talking about the asymmetric PHY communicating on a shielded, balanced, pair of conductors, regardless of transmit bit rate, use: ", etc.

SuggestedRemedy

Delete the definitions below the figure. Add these to the list of nomenclature that is above the table:

MultiGBASE-AT1 Refers to the asymmetric PHY communicating on a shielded, balanced, pair of conductors

MultiGBASE-AV1 Refers to the asymmetric communicating on a coaxial cable

MultiGBASE-A Refers to all PHYs regardless of cable type or bit rate

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

(Editor's note: "shielded, balanced, pair" should simply be "shielded balanced pair". "PHY" is missing from the MultiGBASE-AV1 nomenclature. No change is required to clause 191 if Comment #281 is accepted.)

Delete lines 1 - 11 on page 159.

Add these to the list of nomenclature that is above the table:

MultiGBASE-AT1 Refers to the asymmetric PHY communicating on a shielded balanced pair of conductors

MultiGBASE-AV1 Refers to the asymmetric PHY communicating on a coaxial cable

MultiGBASE-A Refers to all PHYs regardless of cable type or bit rate

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CI 192 SC 192.1.1 P 159 L 17 # 225

Schedl, Anton

BMW Group

Comment Type TR Comment Status D 7.5G

Add a 7.5 Gb/s HS PHY option for use with Clause 192

SuggestedRemedy

Add 7.5 Gb/s HS PHY support according to changes proposed in https://www.ieee802.org/3/dm/public/adhoc/060226/gorshe_3dm_02_D2d0_7d5G-comments.pdf.

Note: for efficiency reasons (i.e., avoid a lot of duplicates in the comments) the referenced page, sub-clause and line # in this comment is reduced to a single sub-clause (192.1.1). All relevant pages, sub-clauses and lines that require update can be seen in the referenced markup file (gorshe_3dm_02_D2d0_7d5G-comments.pdf).

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #357.

CI 192 SC 192.1.1 P 159 L 17 # 226

Schedl, Anton

BMW Group

Comment Type TR Comment Status D 1G

Add a 1 Gb/s LS PHY option for use with Clause 192

SuggestedRemedy

Add 1 Gb/s LS PHY support according to changes proposed in https://www.ieee802.org/3/dm/public/adhoc/060226/chini_3dm_02a_D2d0_1G-comment-preview.pdf

Note: for efficiency reasons (i.e., avoid a lot of duplicates in the comments) the referenced page, sub-clause and line # in this comment is reduced to a single sub-clause (192.1.1). All relevant pages, sub-clauses and lines that require updates can be seen in the referenced markup file (chini_3dm_02a_D2d0_1G-comment-preview.pdf).

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #358.

CI 192 SC 192.1.1 P 159 L 17 # 222

Veloso, Gumersindo

BMW Group

Comment Type TR Comment Status D 1G

Add a 1 Gb/s LS PHY option for use with Clause 192

SuggestedRemedy

Add 1 Gb/s LS PHY support according to changes proposed in https://www.ieee802.org/3/dm/public/adhoc/060226/chini_3dm_02a_D2d0_1G-comment-preview.pdf and adapt any affected chapter/subchapter as can be seen under chini_3dm_02a_D2d0_1G-comment-preview.pdf.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #358.

CI 192 SC 192.1.1 P 159 L 17 # 223

Lee, Ching-Yen

Realtek Semiconductor Corp.

Comment Type TR Comment Status D 7.5G

For the high-speed/low-speed options, add 7.5 Gbps/100 Mbps to Clause 192.

SuggestedRemedy

With editorial license, implement the changes proposed in https://www.ieee802.org/3/dm/public/adhoc/060226/gorshe_3dm_02a_D2d0_7d5G-comments.pdf

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #357.

CI 192 SC 192.1.1 P 159 L 17 # 221

Veloso, Gumersindo

BMW Group

Comment Type TR Comment Status D 7.5G

Add a 7.5 Gb/s HS PHY option for use with Clause 192

SuggestedRemedy

Add 7.5 Gb/s HS PHY support according to changes proposed in https://www.ieee802.org/3/dm/public/adhoc/060226/gorshe_3dm_02_D2d0_7d5G-comments.pdf and adapt any affected chapter/subchapter as can be seen under gorshe_3dm_02_D2d0_7d5G-comments.pdf.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #357.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general

COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed U/unsatisfied Z/withdrawn

SORT ORDER: Clause, Subclause, page, line

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CI 192 SC 192.1.1 P 159 L 17 # 220
 Matheus, Kirsten BMW Group
 Comment Type TR Comment Status D 1G
 Add a 1 Gb/s LS PHY option for use with Clause 192
SuggestedRemedy
 Add 1 Gb/s LS PHY support in accordance with changes proposed in
https://www.ieee802.org/3/dm/public/adhoc/060226/chini_3dm_02a_D2d0_1G-comment-preview.pdf
 Note: for efficiency reasons (the referenced page, sub-clause and line # in this comment is reduced to a single sub-clause (192.1.1). All relevant pages, sub-clauses and lines that require updates can be seen in the referenced markup file (chini_3dm_02a_D2d0_1G-comment-preview.pdf).
Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 Accommodated by Comment #358.

CI 192 SC 192.1.1 P 159 L 17 # 219
 Matheus, Kirsten BMW Group
 Comment Type TR Comment Status D 7.5G
 Add a 7.5 Gb/s HS PHY option for use with Clause 192
SuggestedRemedy
 Add 7.5 Gb/s HS PHY support in accordance with changes proposed in
https://www.ieee802.org/3/dm/public/adhoc/060226/gorshe_3dm_02_D2d0_7d5G-comments.pdf
 Note: for efficiency reasons the referenced page, sub-clause and line # in this comment is reduced to a single sub-clause (192.1.1). All relevant pages, sub-clauses and lines that require update can be seen in the referenced markup file (gorshe_3dm_02_D2d0_7d5G-comments.pdf).
Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 Accommodated by Comment #357.

CI 192 SC 192.1.1 P 159 L 17 # 358
 Wang, Frank Realtek Semiconductor Corp.
 Comment Type T Comment Status D 1G
 In clause 192, add 1 Gb/s data rate for low-speed path when the data rates in high-speed path are 7.5 Gb/s or 5 Gb/s.
SuggestedRemedy
 With editorial license, implement the changes proposed in
https://www.ieee802.org/3/dm/public/adhoc/060226/chini_3dm_02a_D2d0_1G_comments-preview.pdf
Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 TFTD
 (Editor's Note: Resolution of this comment resolves Comments #220, #222, #224, #226, #236, #240, #256, #263, #264, #266, #268, #268, #271, #272, #274, #275, #331, #492, and #496. Filter by Topic In("1G") to locate comments.)

Incorporate changes indicated with green highlights from
https://www.ieee802.org/3/dm/public/adhoc/060226/chini_3dm_02a_D2d0_1G_comments-preview.pdf into the draft

Editorial license granted to conform with Style, etc.

CI 192 SC 192.1.1 P 159 L 17 # 495
 Lin, YK Realtek Semiconductor Corp.
 Comment Type T Comment Status D late - 7.5g
 Add an option of 7.5 Gb/s in the HS_PATH with 100 Mb/s in the LS_PATH
SuggestedRemedy
 With editorial license, add 7.5 Gb/s in the HS_PATH according to the changes proposed in
https://www.ieee802.org/3/dm/public/adhoc/060226/gorshe_3dm_02a_D2d0_7d5G-comments.pdf
Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.
 Accommodated by Comment #357.

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CI 192 SC 192.1.1 P 159 L 17 # 357

Wang, Frank Realtek Semiconductor Corp.

Comment Type TR Comment Status D 7.5G

In clause 192, add a 7.5 Gb/s PHY option for high-speed path.

SuggestedRemedy

With editorial license, implement the changes proposed in https://www.ieee802.org/3/dm/public/adhoc/060226/gorshe_3dm_02a_D2d0_7d5G-comments.pdf

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

(Editor's Note: Resolution of this comment resolves Comments #219, #221, #223, #225, #235, #239, #255, #262, #265, #267, #270, #273, #330, #491, and #495. Filter by Topic In("7.5G") to locate comments.)

Incorporate changes indicated with revision marks from https://www.ieee802.org/3/dm/public/adhoc/060226/gorshe_3dm_02a_D2d0_7d5G-comments.pdf into the draft

Editorial license granted to conform with Style, etc. (blue highlights in the contribution above provide assisting implementation notes for the Editor).

CI 192 SC 192.1.1 P 159 L 17 # 262

Tazebay, Mehmet Broadcom

Comment Type TR Comment Status D 7.5G

Add a 7.5 Gb/s High Speed direction PHY support in Clause 192

SuggestedRemedy

Add a 7.5 Gb/s High Speed direction PHY support https://www.ieee802.org/3/dm/public/adhoc/060226/gorshe_3dm_02_D2d0_7d5G-comments.pdf, with editorial license.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #357.

CI 192 SC 192.1.2 P 160 L 21 # 37

Muma, Scott Microchip

Comment Type E Comment Status D PMD

Text says PHY sublayers are shown shaded, but PMD is not shaded.

SuggestedRemedy

Shade PMD blocks in Figure 192-1.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #64.

CI 192 SC 192.1.2 P 160 L 35 # 64

Ran, Adeo Cisco Systems

Comment Type T Comment Status D PMD

The stack in figure 192-2 includes "PMD" boxes. But these PHYs do not have a PMD sublayer (based on the clause title and lack of a PMD subclause). The AT1 and AV1 are PHYs for different media, and the differences are in the MDI (per 192.1.6).

There are other mentions of "PMD" in 192.9.2.1 and 192.10.2.1, and in the PICS.

SuggestedRemedy

Delete the PMD boxes and legend item from the figure.

Delete other mentions of PMD from the clause.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

(Editor's note: In some cases, PMD should be changed to PMA, in other cases PMD appears in register names and no change is needed.)

Grant the clause 192 Editor license to work with the TDD champion to review use of "PMD" and make updates where appropriate.

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CI 192 SC 192.2.1.9 P 171 L 8 # 168

Wienckowski, Natalie

IVN Solutions LLC; Ethernovia & Bosch

Comment Type T Comment Status D Editorial

There is a "from" but no "to".

SuggestedRemedy

Change: from their initialization states.

To: from their initialization states to their data states.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

(Editor's note: Referring to the non-initialization states as "data states" may not be accurate.)

Replace, "This primitive indicates whether or not the PCS state diagrams are able to transition from their initialization states."

with, "This primitive indicates when the PCS 64B/65B state diagrams are able to process data."

Consider replacing this text is clause 191 as well.

CI 192 SC 192.3.2.2.4 P 177 L 23 # 66

Ran, Adele

Cisco Systems

Comment Type T Comment Status D 192_PCS

The 64B65B coding in this clause seems identical to the one used in previous PHYs (such as clause 149, which is referenced by Clause 191.

If it is the same, it should be referred back too, for consistency and ease of reading and reviewing.

If there are differences, it would help the reader if they are indicated.

SuggestedRemedy

Replace the content of 192.3.2.2.4 through 192.3.2.2.11 with references to clause 149, as done in 191.3.2.2.2 through 191.3.2.2.11 and in 191.4.2.2.4 through 191.4.2.2.11.

Proposed Response Response Status W

PROPOSED REJECT.

Feedback is that people prefer not having to flip between pages in different amendments. 192.3.2.2.4 calls out to the block format in Figure 192-7. 193.3.2.2.5 calls out to the control codes in Table 192-3. Clauses 192.3.2.2.6 through 192.3.2.2.11 support the notations in Table 192-3. Furthermore, accepting Comment #67 will change Table 192-3.

CI 192 SC 192.3.2.2.4 P 177 L 28 # 248

Steve, Gorshe

Microchip Technology

Comment Type E Comment Status D 192_PCS

Suggestion to improve the flow and reduce redundancy of this and the following first paragraph of 193.2.2.5 (line 3 of pp. 179).

SuggestedRemedy

Suggested replacement for the paragraphs beginning in Line 28 and 33: "As illustrated in Figure 192-7, data blocks contain eight data characters and control blocks begin with an eight-bit block type field that indicates the format of the remainder of the block."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Delete lines 28 through 40.

Replace with, "Data blocks contain eight data characters. Control blocks begin with an eight-bit block type field that indicates the format of the remainder of the block."

64B/65B block formats are shown in Figure 192-7. The column labeled Input Data shows, in abbreviated form, the eight characters used to create the 65-bit block. These characters are either data characters or control characters and, when transferred across the XGMII interface, the corresponding TXC or RXC bit is set accordingly. Within the input data column, D0 through D7 are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control octets and are transferred with the corresponding TXC or RXC bit set to one. Each control block contains eight characters. For control blocks containing a Start or Terminate character, as indicated by an S or T octet in the Figure 192-7 Input Data field, that character is implied by the block type field. Other control characters are encoded in a seven-bit control code or a four-bit O Code. The single bit fields in control blocks (thin rectangles with no label in the figure) are sent as zero and ignored upon receipt."

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CI 192 SC 192.3.2.2.4 P 177 L 33 # 249
 Steve, Gorshe Microchip Technology
 Comment Type E Comment Status D 192_PCS

SuggestedRemedy

"The specific format of the blocks is shown in Figure 192-7. The column labeled Input Data shows, in abbreviated form, the eight characters used to create the 65-bit block. These characters are either data characters or control characters and, when transferred across the XGMII interface, the corresponding TXC or RXC bit is set accordingly. Within the input data column, D0 through D7 are data octets and are transferred with the corresponding TXC or RXC bit set to zero. All other characters are control octets and are transferred with the corresponding TXC or RXC bit set to one. Each control block contains eight characters. For control blocks containing a Start or Terminate character, as indicated by an S or T octet in the Figure 192-7 Input Data field, that character is implied by the block type field. Other control characters are encoded in a seven-bit control code or a four-bit O Code. The single bit fields in control blocks (thin rectangles with no label in the figure) are sent as zero and ignored upon receipt."

Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #248.

CI 192 SC 192.3.2.2.5 P 179 L 29 # 67
 Ran, Adeo Cisco Systems
 Comment Type T Comment Status D 192_PCS

Table 192-3 contains two control codes defined as ordered sets, which are encoded by block type and O code; the O codes are provided. In addition, it contains six "reserved" control codes for which the O code is listed as "reserved" too. But these are not O codes (4 bit values).

The reason for having these reserved values is unclear. Valid and reserved XGMII control characters are listed in Table 46-3 and Table 46-4 (802.3-2022), and there are many reserved ones. What is special in the six values listed here?

SuggestedRemedy

Delete "reserved0" through "reserved5" from the "O code" column.

Consider deleting these rows entirely.

Proposed Response Response Status W
 PROPOSED ACCEPT.

CI 192 SC 192.3.2.2.5 P 179 L 41 # 68
 Ran, Adeo Cisco Systems
 Comment Type T Comment Status D 192_PCS

The designation of a special ordered set and control codes for "reserved for Fibre Channel" was made for the BASE-X PCS and then carried over to BASE-R PCS. It is unlikely that Fibre Channel will ever use the new PCS defined here or coexist on same networks, and T11 has not requested the 802.3dm task force to make these reservations. Therefore these reserved codes and ordered sets are just confusing the reader. Carrying this designation forward is not justified.

SuggestedRemedy

Delete the "Signal ordered set" row and update the text in 192.3.2.2.6 accordingly. Also update R_BLOCK_TYPE 192.3.5.1.3 to remove the block type field 0x55.

Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.

(Editor's note: More information is needed regarding the rationale to update R_BLOCK_TYPE 192.3.5.1.3 to remove the block type field 0x55.)

Delete the "Signal ordered set" row in and its corresponding note in Table 192-3.

Delete, "An additional ordered set, the signal ordered set, has been reserved and it begins with another control code." on P179, L52

CI 192 SC 192.3.2.2.5 P 179 L 43 # 250
 Steve, Gorshe Microchip Technology
 Comment Type E Comment Status D 192_PCS

There are other Signal ordered set values in addition to the one for Fibre Channel (i.e., FlexE and MTN). If we include Fibre Channel, they should also be included in the text.

SuggestedRemedy

Since there is no chance that any of those applications would appear in a P802.3dm network application, I recommend deleting this note rather than elaborating the list.

Proposed Response Response Status W
 PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #68.

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CI 192 SC 192.3.2.2.14 P 182 L 1 # 69

Ran, Adeo

Cisco Systems

Comment Type E Comment Status D 192_PCS

The curved arrows in Figure 192-8 are confusing - they don't appear to include RS encoder #1. Supposedly they should denote "round-robin" but that is not the usual representation (more commonly a circular arc is used with terminals placed accordingly. The definition of the sequence under the "output encoded symbols" arrow is sufficient.

SuggestedRemedy

Either draw the curved arrows such that they span all the inputs and outputs (circular arcs), or just remove them.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Consider with Comment #126.

(Editor's note: The intent is to show round-robin distribution of input data to encoder 1..L, and round-robin output from encoder 1..L.)

Center the input arrow and split into "L" pieces. Converge "L" pieces into a single output arrow at the output. Label the input split point "round-robin symbol distribution" and label the output convergence point "round-robin symbol interleave".

Grant Editorial license to work with the TDD champion to make any other supporting changes.

CI 192 SC 192.3.2.2.15 P 182 L 3 # 126

de Koos, Andras

Microchip Technology

Comment Type ER Comment Status D 192_PCS

Though largely reused from Clause 149, the interleave diagram (Figure 192-8) is strange. Specifically, the input distribution and output recombine arrows don't look like they include the first FEC Encoder!

SuggestedRemedy

Consider modifying Figure 192-8 to more effectively show the round robin.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #69.

CI 192 SC 192.3.2.2.16 P 184 L 1 # 70

Ran, Adeo

Cisco Systems

Comment Type T Comment Status D 192_PCS

In Figure 192-9 the output of block p₁ feeds the input of block p_{n-k-1}. This seems incorrect.

SuggestedRemedy

Add something in between (e.g. arrows and ellipsis).

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Grant Editorial license to align with Figure 149-10. Change P2 box to ellipsis and line above P2 to ellipsis.

CI 192 SC 192.3.2.2.17 P 185 L 28 # 180

Wienckowski, Natalie

IVN Solutions LLC; Ethernova & Bosch

Comment Type E Comment Status D 192_PCS

This sentences is very confusing. Do you meand the second MSB, meaning bit 7 if there were 8 bits, or do you mean the 2nd bit is the MSB. I think it is the latter and my suggestion is based on this.

SuggestedRemedy

Change: The first least significant bit (LSB) is DS_n[0] equal to Sc_{rn}[0]. The second most significant (MSB) bit is DS_n[1] .

To: The first bit, which is the least significant bit (LSB) is DS_n[0] equal to Sc_{rn}[0]. The second bit, which is the most significant (MSB) bit is DS_n[1] ...

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Change: The first least significant bit (LSB) is DS_n[0] equal to Sc_{rn}[0]. The second most significant (MSB) bit is DS_n[1].

To: The first bit, which is the least significant bit (LSB), is DS_n[0] equal to Sc_{rn}[0]. The second bit, which is the most significant (MSB) bit, is DS_n[1] .

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CI 192 SC 192.3.2.2.17 P 185 L 35 # 72

Ran, Adeo

Cisco Systems

Comment Type T Comment Status D 192_PCS

Equations 192-6 and 192-7 defining A_n and B_n, which seem to apply only with tx_mode=SEND_N. Assuming that is the case, then there is no need to list tx_mode=SEND_N in their definitions (it raises the question what happens when the mode is different?)

SuggestedRemedy

Delete "tx_mode=SEND_N" and the opening brace in both equations

Proposed Response Response Status W

PROPOSED REJECT.

"tx_mode=SEND_N" should not be deleted as the assignment is only defined during the range of "n" shown and when tx_mode=SEND_N. The curly bracket indicates a conditional assignment and should not be deleted.

CI 192 SC 192.3.2.2.18 P 185 L 46 # 73

Ran, Adeo

Cisco Systems

Comment Type T Comment Status D scrambler

The initial value of the PRBS11 generator is not specified. I assume it can be any value except all zeros, as in the PRBS33 scramblers.

SuggestedRemedy

Indicate the reset conditions and requirements for the PRBS11 generator, as done in 192.3.2.2.19.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Insert, "The pattern generator is reset upon execution of the PCS Reset function. If PCS Reset is executed, all bits of the eleven-bit vector representing the scrambler state are arbitrarily set. The initialization of the scrambler state is left to the implementer. In no case, shall the scrambler state be initialized to all zeros." on P185, L45 before the sentence that starts, "This implements the generator polynomial."

Editorial license to add PICS.

CI 192 SC 192.3.2.2.18 P 185 L 53 # 251

Steve, Gorshe

Microchip Technology

Comment Type E Comment Status D scrambler

Add clarification regarding when the PRBS11 runs.

SuggestedRemedy

While this is specified in 192.3.6.3, for consistency with 192.3.2.2.19, it would be good to add new text below Equation 192-8: "This scrambler, once started during PMA training, shall continue to run uninterrupted during the refresh headers of each frame and shall stop during the burst payload field and QUIET." Note that 192.3.6 also contains a statement similar to the one in 192.3.2.2.19.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Insert the following text after the new text inserted by Comment #73:

"This scrambler, once started during PMA training, shall continue to run uninterrupted during the refresh headers of each frame and shall stop during the burst payload field and QUIET."

Editorial license to add PICS.

CI 192 SC 192.3.2.2.19 P 186 L 20 # 128

de Koos, Andras

Microchip Technology

Comment Type ER Comment Status D scrambler

Though we've abandoned master/slave terminology in favour of Leader/Follower, Equations (192-9) and (192-10) still use "M/S".
Comment also applies to equation (191-8) in Section 191.4.2.2.16

SuggestedRemedy

Replace gM(x) and gS(s) with gL(X) and gF(x), respectively.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

(Editor's note: For information only - it is proposed to replace gM(x) and gS(s) with gD(X) for PHY_D and gS(x) for PHY_S in clause 191.)

In clause 192:

Replace gM(x) with gL(X) and replace gS(s) with gF(x) in Equations (192-9), (192-10), and (191-8).

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CI 192 SC 192.3.2.2.19 P 186 L 34 # 181
Wienckowski, Natalie IVN Solutions LLC; Ethernovia & Bosch
Comment Type E Comment Status D Editorial
unnecessary comma
SuggestedRemedy
Delete the comma after "In no case".
Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
(Editor's note: Explicitly state as a requirement.)
Replace, "In no case, shall the scrambler state be initialized to all zeros."
with, "The scrambler state shall not be initialized to all zeros."
Editorial license granted to adjust PICS.

CI 192 SC 192.3.2.2.19 P 187 L 1 # 74
Ran, Adeo Cisco Systems
Comment Type E Comment Status D scrambler
Figure 192-11 shows two LFSR realizations which are conceptually similar to the PRBS11 generator in Figure 192-10, but the symbols used for the addition and the delay elements are different, the figure titles are different, and the scrambler in figure 192-11 has no explicit output (although in Figure 192-6 it is shown that it has three outputs, Scr_n indexes 0, 3, and 8).
SuggestedRemedy
Change one of the figures (preferably figure 192-10) to be consistent with the other, especially the addition and delay elements.
Preferably, show the outputs of the LFSRs in Figure 192-11.
Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
(Editor's note: Figure 192-10 comes from Figure 72-3, while Figure 192-11 comes from Figure 149-11. Modifying Figure 192-11 to show LFSR outputs would be a divergence from clauses 149, 165, and 191.)
License granted for Editor to work with TDD champion to modifying Figure 192-10 for consistency with Figure 192-11 and to show LFSR outputs.

CI 192 SC 192.3.2.2.22 P 188 L 23 # 490
Zerna, Conrad NXP
Comment Type TR Comment Status D 192_PCS
PAM2 encoding is inconsistent with PAM4 encoding, which is problematic for refresh header versus payload.
SuggestedRemedy
Change line to:
Input bit Sn is mapped to the transmit symbol Tn as follows: if Sn = 0, then Tn = -1, if Sn = 1, then Tn = +1.
Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
Change line to:
Input bit Sn is mapped to the transmit symbol Tn as follows:
if Sn = 0, then Tn = -1, and
if Sn = 1, then Tn = +1.

CI 192 SC 192.3.4 P 193 L 23 # 75
Ran, Adeo Cisco Systems
Comment Type E Comment Status D 192_PCS
The symbol S_t is mixed typographic subscript and markup subscript. It is very unusual, and it makes it awkward to read and to refer to verbally (is it S-sub-t-sub-n?) I guess the "t" signifies that these are training symbols. But lowercase t usually stands for time.
Surely a simpler notation is possible.
SuggestedRemedy
In Figure 192-5 this symbol appears as the output of the "training payload generator" so I'd suggest labeling it TP_n.
Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
(Editor's note: Suggest TF to be Training Frame to avoid confusion with Training Payload.)
Globally replace, "S_{tn}" with "TF_n"
where n is in subscript.

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CI 192 SC 192.3.4 P 196 L 3 # 252

Steve, Gorshe Microchip Technology

Comment Type T Comment Status D 192_PCS

Add reference to new figure and table described in comment below.

SuggestedRemedy

Add new sentence to the end of the paragraph: "See Figure 192-hh and Table 192-hh for an illustration of the data burst payload structure."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #254.

CI 192 SC 192.3.4 P 196 L 33 # 254

Steve, Gorshe Microchip Technology

Comment Type T Comment Status D 192_PCS

Add new figure and table to illustrate the data burst payload structure.

SuggestedRemedy

Add new paragraph below Figure 192-18: "The burst payload structures are illustrated in Figure 192-hh, with the data burst payload information summarized in Table 192-h." Below this paragraph, insert the new figure and table from the attached file data_burst_format_fig_table.pdf

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Add new paragraph below Figure 192-18, "The burst payload structures are illustrated in Figure 192-hh. Data burst payload information is summarized in Table 192-h."

Insert the new figure and table from https://www.ieee802.org/3/dm/public/0726/data_burst_format_fig_table.pdf after the paragraph.

Editorial license granted to align figure and table with IEEE Style.

CI 192 SC 192.3.4.1 P 196 L 36 # 127

de Koos, Andras Microchip Technology

Comment Type E Comment Status D 192_PCS

It could be informative to note in this paragraph that the values in tables 192-7, 192-8, and 192-9 (symbols) are equivalent to the time values in Table 192-6

SuggestedRemedy

Add the an explicative note to the paragraph:

The durations (expressed in symbols) in the tables below match the durations (expressed in time) in Table 192-6.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Insert NOTE on P196L40:

NOTE - The durations for $N_{_r}$, $N_{_p}$, and $N_{_z}$ (expressed in symbols) in the Table 192-7 and Table 192-8 correspond to the durations (expressed in ns) in Table 192-6.

where $$ indicates a subscript.

CI 192 SC 192.3.4.3 P 198 L 42 # 76

Ran, Adeo Cisco Systems

Comment Type T Comment Status D 192_PCS

The terms $A_{_n}$ and $G_{_n}$ are used in equation 192-13 without a definition in the equation. $A_{_n}$ is defined in equations 192-5 and 192-6, but I found only one other instance of $G_{_n}$ (in Figure 191-9, another clause). I suspect that $G_{_n}$ corresponds to $G(n)$ defined in 192.3.2.2.20.

SuggestedRemedy

Add references to the definitions of these terms.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Insert the following variables before PAM2_Mapper:

$A_{_n}$ is specified in 192.3.2.2.20

$G_{_n}$ is the Gray-coded symbol specified in 192.3.2.2.20

Globally replace $G(n)$ with $G_{_n}$

where n is in subscript.

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CI 192 SC 192.3.5.1.2 P 199 L 52 # 183

Wienckowski, Natalie IVN Solutions LLC; Ethernovia & Bosch

Comment Type T Comment Status D 192_PCS

missing definition of when to set FALSE

SuggestedRemedy

Add to the end of the definition: It is set FALSE otherwise.
Also on P200L3, P200L11, and P200L15.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

(Editor's note: This change is OK for block_lock and pcs_reset, but perhaps not for hi_rfer and rf_valid. Hi_rfer has a state machine which defines when it's TRUE/FALSE, while rf_valid is false when an RS-FEC frame is received and is uncorrectable.)

Add to the end of the definition: It is set FALSE otherwise.

Also on P200L11.

CI 192 SC 192.4.1 P 207 L 21 # 470

Law, David

HPE

Comment Type TR Comment Status D 192_PHY_Cntrl

Figure 192-22 'PMA reference diagram' shows the config variable sourced from the PHY CONTROL block and passed from the PMA to the PCS across the PMA service interface. Subclause 192.4.2.4 'PHY Control function' says that 'PHY Control shall comply with the state diagram in Figure 192-26'.

Figure 192-26 'PHY Control state diagram', however, uses the config variable as an input, as part of the transition condition from the SILENT to TRAINING0 state. The config variable, therefore, is not sourced from the PHY CONTROL block as shown in Figure 192-22. Instead, both subclause 192.4.2.4.11 'Startup sequence' and subclause 192.2.1.2 'PMA_CONFIG.indication' say that the config variable is determined via management control or default hardware setup.

In addition, the PMA_CONFIG.indication primitive passes the config parameter from the PMA sublayer to the PCS; therefore, it seems odd to reference the PMA_CONFIG.indication config parameter in the PMA, since it is sourced there.

SuggestedRemedy

[1] Update figure 192-22 'PMA reference diagram' to [a] show a Configuration block that sources config and [b] show the config variable as an input to the PHY control block.

[2] Add a new PMA subclause as follows:

192.4.2.X PMA Configuration function

The PMA Configuration function sets the config variable to LEADER or FOLLOWER based on management control during initialisation or hardware setup.

[3] In subclause 192.4.4.1 'State diagram variables', change the definition of the config variable to read:

config
See 192.4.2.X.

[4] In subclause 192.4.2.4.11 'Startup sequence', delete the text 'PMA_CONFIG is predetermined to be the LEADER or FOLLOWER ...' since this is now addressed in the new 192.4.2.X 'PMA Configuration function' subclause.

[5] In subclause 192.4.2.2 'PMA Transmit function' change the text 'When the PMA_CONFIG.indication parameter config is LEADER, the ...' to read 'When the config variable (see 192.4.2.X) is set to LEADER, the ...' and change the text 'If the PMA_CONFIG.indication parameter config is FOLLOWER, the PMA Transmit function ...' to read 'When the config variable is set to FOLLOWER, the PMA Transmit function ...'.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general

COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed U/unsatisfied Z/withdrawn

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(Editor's note: This is a carry-over issue from clauses 149 and 165.)

License granted for the Editor to work with the TD champion to define config as a variable for the PMA and PCS that is set according to the value of register bit 1.2100.14, and pull config out of the PMA interface since it's really a static management/config setting not a PMA->PCS signal.

Editorial license granted to update diagrams, etc. affected by this change.

Cl 192 SC 192.4.2.4.5 P 212 L 16 # 40

Muma, Scott Microchip

Comment Type T Comment Status D 192_PHY_Cntrl

The HS Rate fields could better align with the registers 1.2318 and 1.2320 in Clause 45 and the negotiated rate field by leaving a gap between 10G and 5G.

SuggestedRemedy

In Table 192-11 swap 10 Gb/s and Reserved between bit 5 and bit 4 in both Octet 9 and Octet 10.

In Table 192-12 swap 10Gb/s and Reserved between row 000100 and 001000.

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 192 SC 192.4.2.4.5 P 212 L 44 # 54

Muma, Scott Microchip

Comment Type E Comment Status D 192_PHY_Cntrl

Their can be multiple rates supported, so instead of 0's for the rows that have a 1 bit there should be x's.

SuggestedRemedy

In Table 192-12 in LS rate change 01 to x1, change 10 to 1x, delete the row with 11.

In HS rate change:

000001 to xxxxx1

000010 to xxxx1x

000100 to xxx1xx

001000 to xx1xxx

010000 to x1xxxx

100000 to 1xxxxx

Proposed Response Response Status W

PROPOSED ACCEPT.

Cl 192 SC 192.4.2.4.6 P 214 L 19 # 449

Ganesan, Aravind

Texas Instruments

Comment Type TR Comment Status D 192_PHY_Cntrl

It is not clear how the link segment delay maps to the delay count in the TDD delay counter. the link segment delay could also have some slow variation over time due to temperature drift.

SuggestedRemedy

A clarification in this section will help avoid ambiguity in implementation.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Insert, "The TDD delay counter may be calculated as the estimated link segment delay in symbol times (at the 3 Gbd rate) divided by 16, then rounded to the nearest integer." after ".. delay_count_valid bit to 1." on P214, L21

Cl 192 SC 192.4.2.4.6 P 214 L 20 # 196

Wienckowski, Natalie

IVN Solutions LLC; Ethernovia & Bosch

Comment Type T Comment Status D 192_PHY_Cntrl

The "should" should be "shall. Is it okay if the LEADER doesn't estimate the link segment delay? Can it just guess or pick a random value?

SuggestedRemedy

Change: it should estimate the link segment delay

To: it shall estimate the link segment delay

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

(Editor's note: The observable behavior is setting the delay_count and setting the delay_count_valid.)

Replace, "After the LEADER detects the FOLLOWER TDD burst position, it should estimate the link segment delay, then set its delay_count in the TDD delay counter to a value between 0 to 63, as well as set delay_count_valid bit to 1."

With, "After the LEADER detects the FOLLOWER TDD burst position and estimates the link segment delay, it shall set its delay_count in the TDD delay counter to a value between 0 to 63, as well as set delay_count_valid bit to one."

Grant Editorial license to add supporting PICS.

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CI 192 SC 192.4.5 P 220 L 20 # 347

Wang, Frank Realtek Semiconductor Corp.

Comment Type TR Comment Status D 192_link_mon

link_fail_inhibit_timer_done should only be valid when training_active = TRUE. Therefore, the condition for SILENT to DT needs update to avoid possible deadlock.

SuggestedRemedy

change one of the output conditions of SILENT state, "link_fail_inhibit_timer_done", to "link_fail_inhibit_timer_done * training_active".

Proposed Response Response Status W

PROPOSED ACCEPT.

CI 192 SC 192.4.5 P 220 L 24 # 348

Wang, Frank Realtek Semiconductor Corp.

Comment Type TR Comment Status D 192_link_mon

rem_countdown_done has a similar definition as loc_countdown_done. As the description in 192.4.4.1, both are set to FALSE when entering to a TRAINING state. If "loc_countdown_done <= FALSE" is included in TRAINING0 and TRAINING1 of PHY Control state diagram, "rem_countdown_done <= FALSE" should also be included.

SuggestedRemedy

Add "rem_countdown_done <= FALSE" to TRAINING0 and TRAINING1 states.

Proposed Response Response Status W

PROPOSED ACCEPT.

CI 192 SC 192.4.5 P 221 L 36 # 472

Law, David HPE

Comment Type TR Comment Status D 192_link_mon

Figure 192-27 'PHY Control state diagram' in the PMA uses the hi_rfer and block_lock variables, yet these variables are not defined in subclause 192.4.4.1 'State diagram variables'. The hi_rfer and block_lock variables are generated in the PCS, with the hi_rfer variable generated in Figure 192-19 'RFER monitor state diagram', and the block_lock generated in subclause 192.3.2.3 PCS 'Receive function'. As a result, these variables pass across the PMA Service interface, yet they are not parameters of any of the primitives defined in subclause 192.2.1 'PMA service interface'. Further, they are not illustrated in Figure 192-3 'MultiGBASE-A service interface', Figure 192-4 'PCS reference diagram', or Figure 192-22 'PMA reference diagram'.

SuggestedRemedy

[1] Add the following to the list of primitives in subclause 192.2.1 'PMA service interface':

PMA_PCSSYNC.request(block_lock, rfer_cnt)

[2] Add an arrow labelled 'PMA_PCSSYNC.request' from the PHY_S PCS to PHY_S PMA block in Figure 191-5 'PHY_S service interfaces' in Figure 191-5 'PHY_S service interfaces' and Figure 191-6 'PHY_D service interfaces'.

[3] Add the following new subclauses to subclause 192.2.1:

192.2.1.X PMA_PCSSYNC.request

192.2.1.X.1 Semantics of the primitive

PMA_PCSSYNC.request(block_lock, rfer_cnt)

The PMA_PCSSYNC.request primitive passes the block_lock and rfer_cnt parameters from the PCS to the PMA.

The parameter block_lock can take on one of the following two values of the form:

TRUE The PCS Synchronization process has acquired block delineation.

FALSE The PCS Synchronization process has not acquired block delineation.

The parameter rfer_cnt can take on one of the following two values of the form:

TRUE The PCS Synchronization has detected 16 errors in one RFRX_CNT_LIMIT interval.

FALSE The PCS Synchronization has not detected 16 errors in one RFRX_CNT_LIMIT interval.

192.2.1.X.2 When generated

The PCS generates PMA_PCSSYNC.request messages to indicate a change in block_lock or rfer_cnt.

TYPE: TR/technical required ER/editorial required GR/general required T/technical E/editorial G/general

COMMENT STATUS: D/dispatched A/accepted R/rejected RESPONSE STATUS: O/open W/written C/closed U/unsatisfied Z/withdrawn

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192.2.1.X.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 191-31.

[4] Add block_lock and rfer_cnt to figures 192-3, 192-4, and 192-22.

[5] Add the following variables to subclause 192.4.4.1 'State diagram variables':

block_lock

Boolean variable that is set TRUE by the PCS Synchronization process when it acquires block delineation. It is passed to the PMA via the block_lock parameter of the PMA_PCSSYNC.request primitive.

hi_rfer

Boolean variable that is set TRUE by the PCS Synchronization process when the rfer_cnt reaches 16 errors in one RFRX_CNT_LIMIT interval. It is passed to the PMA via the rfer_cnt parameter of the PMA_PCSSYNC.request primitive.

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.

(Editor's note: This is a carry-over issue from clauses 149 and 165. Some figure references in the comment referred to clause 191 and needed to be corrected.)

Grant editorial license to implement the following changes with any necessary style or other adjustments needed in case of reference or other inconsistencies:

[1] Add the following to the list of primitives in subclause 192.2.1 'PMA service interface':

PMA_PCSSYNC.request(block_lock, rfer_cnt)

[2] Add an arrow labelled 'PMA_PCSSYNC.request' from the PHY_S PCS to PHY_S PMA block in Figure 192-3 'PHY_S service interfaces' in Figure 192-3 'PHY_S service interfaces' and Figure 192-3 'PHY_D service interfaces'.

[3] Add the following new subclauses to subclause 192.2.1:

192.2.1.X PMA_PCSSYNC.request

192.2.1.X.1 Semantics of the primitive

PMA_PCSSYNC.request(block_lock, rfer_cnt)

The PMA_PCSSYNC.request primitive passes the block_lock and rfer_cnt parameters from the PCS to the PMA.

The parameter block_lock can take on one of the following two values of the form:

TRUE The PCS Synchronization process has acquired block delineation.

FALSE The PCS Synchronization process has not acquired block delineation.

The parameter rfer_cnt can take on one of the following two values of the form:

TRUE The PCS Synchronization has detected 16 errors in one RFRX_CNT_LIMIT interval.

FALSE The PCS Synchronization has not detected 16 errors in one RFRX_CNT_LIMIT interval.

192.2.1.X.2 When generated

The PCS generates PMA_PCSSYNC.request messages to indicate a change in block_lock or rfer_cnt.

192.2.1.X.3 Effect of receipt

The effect of receipt of this primitive is specified in Figures 192-27 and 192-28.

[4] Add block_lock and rfer_cnt to figures 192-3, 192-4, and 192-22.

[5] Add the following variables to subclause 192.4.4.1 'State diagram variables':

block_lock

Boolean variable that is set TRUE by the PCS Synchronization process when it acquires block delineation. It is passed to the PMA via the block_lock parameter of the PMA_PCSSYNC.request primitive.

hi_rfer

Boolean variable that is set TRUE by the PCS Synchronization process when the rfer_cnt reaches 16 errors in one RFRX_CNT_LIMIT interval. It is passed to the PMA via the rfer_cnt parameter of the PMA_PCSSYNC.request primitive.

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CI 192 SC 192.5.1 P 223 L 23 # 349

Wang, Frank Realtek Semiconductor Corp.

Comment Type TR Comment Status D 192_tests

10 Gb/s PHY transmits PAM4 for test mode 4, not PAM2.

SuggestedRemedy

change:

"PHYs that support 5 Gb/s and 10 Gb/s transmit rates shall support transmission of this signal at 6 GBd."

to:

"PHYs that support 5 Gb/s transmit rate shall support transmission of this signal at 6 GBd."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

(Editor's note: 10G PHYS also use PAM2 transmission at 6GBd, so for a 10G PHY is it useful to test in both PAM2 and PAM4 at 6Gb/s? An "a" or a "the" now seems appropriate before 5 Gb/s transmit rate.)

Change:

"PHYs that support 5 Gb/s and 10 Gb/s transmit rates shall support transmission of this signal at 6 GBd."

to:

"PHYs that support a 5 Gb/s transmit rate shall support transmission of this signal at 6 GBd."

Grant Editorial license to adjust PICS, if necessary.

CI 192 SC 192.5.2.4 P 227 L 26 # 359

Seth, Sumantra Texas Instruments

Comment Type TR Comment Status D consensus

Table 192-19 power levels are higher than Table 191-16 power level.

SuggestedRemedy

Should have Same power level between Table 192-19 and Table 191-16

Proposed Response Response Status W

PROPOSED REJECT.

The comment does not contain sufficient rationale to justify the change.

CI 192 SC 192.7.1.5 P 233 L 53 # 29

Bergner, Bert TE Connectivity

Comment Type T Comment Status D 192_Lnk_Seg

Screening attenuation refers to SC 149.7.1.5. This subclause defines screening attenuation with 45dB from 30MHz up to Fmax. Fmax depends on speed grade in Clause 149. Thus, we inherit the speed grade dependency from Clause 149 which will differentiate between 2.5G, 5G and 10G. This conflicts with the idea of screening and coupling attenuation in 192 to be independent of speed grade.

SuggestedRemedy

Change the sentence to "The screening attenuation of each -T1 link shall be as specified in 149.7.5.1 with Fmax = 5000 MHz."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

(Editor's note: "segment" was dropped from the comment. A "," seems missing.)

Replace, "The screening attenuation of a -T1 link segment shall be as specified in 149.7.1.5."

with, "The screening attenuation of a -T1 link segment shall be as specified in 149.7.1.5, with Fmax = 5000 MHz."

Grant Editorial license to adjust PICS as necessary.

CI 192 SC 192.7.1.6 P 234 L 3 # 205

Wienckowski, Natalie IVN Solutions LLC; Ethernova & Bosch

Comment Type T Comment Status D 192_Lnk_Seg

Why is the frequency range for the maximum link delay different from the frequency range for IL and RL?

SuggestedRemedy

Change: between 3 MHz and 4 GHz.

To: between 10 MHz and 5 GHz.

Proposed Response Response Status W

PROPOSED ACCEPT.

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CI 192 SC 192.8.1.5 P 239 L 3 # 136

Long, Richard TE Connectivity

Comment Type TR Comment Status D 192_Lnk_Seg

Screening attenuation limits need to be changed

SuggestedRemedy

The screening attenuation of a -V1 link segment shall meet the values determined using Equation (191-19). Screening attenuation is tested as specified in IEC 62153-4-7 using triaxial tube-in-tube method. Additional screening attenuation test methodologies are defined in Annex 149A. These methodologies shall be applied with adaptation to unbalanced coaxial cabling. (See Bergner contribution from June 16 Ad Hoc)

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comments #34 and #30.

CI 192 SC 192.8.1.5 P 239 L 4 # 34

Bergner, Bert TE Connectivity

Comment Type T Comment Status D 192_Lnk_Seg

Screening attenuation for -V1 coaxial unbalanced link segment: The sentence "Additional screening attenuation test methodologies are defined in Annex 149A." takes reference to clause 149A which defines screening attenuation measurement specifically for balanced link segments only. This may cause confusion.

SuggestedRemedy

Change the sentence to "The additional screening attenuation test methodologies defined in Annex 149A shall be applied with adaptation to unbalanced coaxial cabling."

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

(Editor's note: A contribution addressing -V1 screening attenuation final test methods is expected.)

Delete, "Additional screening attenuation test methodologies are defined in Annex 149A." and replace with new text pending contribution

Editorial license granted to align PICS.

CI 192 SC 192.8.1.5 P 239 L 7 # 30

Bergner, Bert TE Connectivity

Comment Type T Comment Status D 192_Lnk_Seg

Screening attenuation for clause 192 -V1 link segments is defined by (192-27) with 64dB up to 3GHz and 54dB up to 5GHz. The link segment contains cable and connectors. The USCAR-49 defines screening attenuation for a single connector only with 62dB up to 2GHz which is less than the 192 -V1 link segment. USCAR-49 is considered as state of the art definition of automotive grade coaxial connectors. Thus, the 802.3dm objective "Define ... link segments suitable for use with ... automotive unbalanced coaxial cabling supporting use of up to 4 inline connectors ..." cannot be fulfilled.

SuggestedRemedy

Change screening attenuation requirements for 192.8.1.5 in equation (192-27) to same value as in 191.10.1.5 (equation (191-19)).

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

CI 192 SC 192.8.1.6 P 239 L 42 # 206

Wienckowski, Natalie IVN Solutions LLC; Ethernovia & Bosch

Comment Type T Comment Status D 192_Lnk_Seg

Why is the frequency range for the maximum link delay different from the frequency range for IL and RL?

SuggestedRemedy

Change: between 3 MHz and 4 GHz.
To: between 10 MHz and 5 GHz.

Proposed Response Response Status W

PROPOSED ACCEPT.

IEEE P802.3dm D2.0 Asymmetrical Electrical Automotive Ethernet Initial Working Group ballot comments

CI 192 SC 192.8.2 P 239 L 50 # 35
Bergner, Bert TE Connectivity
Comment Type T Comment Status D 192_Lnk_Seg
Coupling parameters for -V1 coaxial link segments: The sentence "Test methodologies are specified in Annex 97B." refers to Annex 97B which specifically describes cross talk measurements for balanced cabling. Especially the description in 97A "Link segment ends not under test are terminated in 100 Ohm differential mode and 200 Ohm common mode." and Figure 97B-1 may cause confusion.
SuggestedRemedy
Change the sentence to "Test methodologies are specified in Annex 97B and shall be applied with adaptation to unbalanced coaxial cabling."
Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
TFTD. Resolve after Comment #34.
(Editor's note: A contribution addressing -V1 screening attenuation final test methods is expected.)
Delete, "The test methodologies are specified in Annex 97B." and replace with new text pending contribution
Editorial license granted to align PICS.

CI 192 SC 192.9.2.1 P 243 L 21 # 207
Wienckowski, Natalie IVN Solutions LLC; Ethernovia & Bosch
Comment Type T Comment Status D 192_Lnk_Seg
Why is the maximum MDI RL frequency less than the link segment RL frequency? I think is left from before the link segment requirements were finalized.
SuggestedRemedy
Change: 4000
To: 5000 for 5 Gb/s and 10 Gb/s
Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
TFTD

CI 192 SC 192.10.2.1 P 244 L 36 # 208
Wienckowski, Natalie IVN Solutions LLC; Ethernovia & Bosch
Comment Type T Comment Status D 192_Lnk_Seg
Why is the maximum MDI RL frequency less than the link segment RL frequency? I think is left from before the link segment requirements were finalized.
SuggestedRemedy
Change: 4000
To: 5000 for 5 Gb/s and 10 Gb/s
Proposed Response Response Status W
PROPOSED ACCEPT IN PRINCIPLE.
TFTD

IEEE P802.3dm D2.0 Asymmetrical Electrical Automotive Ethernet Initial Working Group ballot comments

CI 192 SC 192.12 P 246 L 40 # 121

Kim, Yong

General Motors

Comment Type TR Comment Status D 192_delay

Pause (CL31 and Annex 31B) operation seem irrelevant to camear and display application that these asymmetric PHYs are defined to be used. This said, 31.B.4.3, Pg 6383 on 802.3-2022 edition, refers to 31.B.3.7 that says "Stations that do not implement an exposed MII, shall measure this time at the MDI, with the timing specification increased to one pause_quantum + 64 BT." This project has 100 Mbps that does not have exposed MII, the timing is increased by 64 BT. this conflicts with "The sum of the transmit and receive data delays for an implementation of the PHY shall not exceed the limits shown in Table 192-24." in CL192.12, pg 247 line 1.

SuggestedRemedy

Select which one is correct, i.e. pause quanta with our without +64 BT, and revise the text to match.

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

TFTD

(Editor's note: 192.12 addresses the transmit+receive delay in one direction between 2 different devices (i.e., Tx XGMII->MDI, Tx->MDI, Rx->Rx XGMII) so only one speed is involved. The limit in Annex 31B is from an Rx MDI->Rx XGMII->MAC Control->TX MAC->Tx XGMII->Tx MDI, which is all within a single device. In this case, there are 2 different speeds involved and application of the limits in Annex 31B is unclear. It may reduce confusion if the system uses the delay limits in 192.12, as well as updated limits for asymmetric links added to 31B.4.6. Note the time for 2.5G is only 6 pause_quanta, which is not met by many clauses.)

Grant Editor license to work with TDD champion to bring appropriate sections of Annex 31B (e.g., text and PICS) into the draft and add limits for the Clause 192 PHY.

Consider whether any updates are needed based on Clause 191 as well.

CI 192 SC 192.12 P 247 L 10 # 383

Maguire, Valerie

Copperopolis; affl w/ CME Consulting, Microchip, and

Comment Type T Comment Status D delay

Make adjustments to Table 192-24 and Table 191-24 to align with Table 81-1 and make minor editorial adjustments.

SuggestedRemedy

In Table 192-24 and Table 191-24,

Change table title from "Delay Limits" to "Delay constraints"

Change "Bit times" column header to "Maximum bit time (BT)"

Change "Pause quanta" column header to "Maximum pause_quantum"

Change "Delay (ns)" to "Maximum delay (ns)"

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

In Table 192-24 and Table 191-24,

Change table title from "Delay Limits" to "Delay constraints"

Change "Bit times" column header to "Maximum delay (BT)"

Change "Pause quanta" column header to "Maximum delay (pause_quantum)"

Change "Delay (ns)" to "Maximum delay (ns)"

CI 192 SC 192.13 P 249 L 4 # 85

Lusted, Kent

Synopsys

Comment Type TR Comment Status D PICS

PICS entries for 192.13.3, 192.13.4.1, and 192.13.4.2 are incomplete

SuggestedRemedy

Complete PIC entries

Proposed Response Response Status W

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #448.

IEEE P802.3dm D2.0 Asymmetrical Electrical Automotive Ethernet Initial Working Group ballot comments

CI 192 **SC 192.13.3** **P 248** **L 5** # 284

Jones, Peter Cisco Systems

Comment Type **TR** **Comment Status** **D** **PICS**

PICS are missing.

SuggestedRemedy
Complete PICS

Proposed Response **Response Status** **W**

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #448.

CI 192 **SC 192.13.3** **P 249** **L 6** # 120

Kim, Yong General Motors

Comment Type **TR** **Comment Status** **D** **PICS**

This sub-clause on, PICS Profoma is incomplete. Please complete.

SuggestedRemedy
Please complete.

Proposed Response **Response Status** **W**

PROPOSED ACCEPT IN PRINCIPLE.

Accommodated by Comment #448.