Cl **45** *SC* **45.2.1** *P* **37** *L* **18** # 294

Wienckowski, Natalie IVN Solutions LLC; Ethernovia, Bosch

Comment Type **T** *Comment Status* **D** *late - EZ*

We changed the name of register 1.18, but don't show the updated name in Table 45-3

SuggestedRemedy

Bring in the row for register 1.18 and show the name change as shown in 45.2.1.16.

Proposed Response *Response Status* **O**

Cl **45** *SC* **45.2.1** *P* **37** *L* **24** # 295

Wienckowski, Natalie IVN Solutions LLC; Ethernovia, Bosch

Comment Type **T** *Comment Status* **D** *late - EZ*

We changed the name of register 1.2100, but don't show the updated name in Table 45-3

SuggestedRemedy

Bring in the row for register 1.2100 and show the name change as shown in 45.2.1.214.

Proposed Response *Response Status* **O**

Cl **46** *SC* **46.6.2.3** *P* **55** *L* **43** # 296

Muma, Scott Microchip

Comment Type **T** *Comment Status* **D** *late - PICS*

Given that XGMII currently supports one or more symmetric data rates it follows that the XGMII can support both one or more asymmetric and symmetric data rates. So asymmetric data rates should be in the same group of options as symmetric data rates (PHY:O.1).

SuggestedRemedy

Change ASM to *ASM and change the Status of *ASM to PHY:O.1

Proposed Response *Response Status* **W**

Cl **46** *SC* **46.6.3.1** *P* **56** *L* **5** # 297

Muma, Scott Microchip

Comment Type **T** *Comment Status* **D** *late - PICS*

This comment supercedes comment #147 and assumes status of *ASM is PHY:O.1

An Asymmetric PHY must support at least one or more high speed rate in at least one direction AND simultaneously support a lower speed in the other direction. Listing out all the speeds as independent options makes this difficult to capture. Instead define a PHY_D Feature and a PHY_S Feature both with Status ASM:O.2 with reference to Clause 191 and Clause 192. Then define the 10 transmit speed/direction combinations:
TX100M Status: PHY_D:M
RX100M Status: PHY_S:M
TX2.5G Status: PHY_S:O.3
TX5G Status: PHY_S:O.3
TX7.5G Status: PHY_S:O.3
TX10G Status: PHY_S:O.3
RX2.5G Status: PHY_D:O.4
RX5G Status: PHY_D:O.4
RX7.5G Status: PHY_D:O.4
RX10G Status: PHY_D:O.4

SuggestedRemedy

Add *PHY_S and *PHY_D items to the major capabilities/options table in 46.6.2.3 following the *ASM item with the Status ASM:O.2 for both new items.

Add the following 10 speed/direction combination items to the table in 46.6.3.1:
TX100M Status: PHY_D:M
RX100M Status: PHY_S:M
TX2.5G Status: PHY_S:O.3
TX5G Status: PHY_S:O.3
TX7.5G Status: PHY_S:O.3
TX10G Status: PHY_S:O.3
RX2.5G Status: PHY_D:O.4
RX5G Status: PHY_D:O.4
RX7.5G Status: PHY_D:O.4
RX10G Status: PHY_D:O.4
with editorial license on Feature Subclause Value/Comment, deleting/replacing the current items G3a, G3b.

Proposed Response *Response Status* **W**

Cl **191** *SC* **191.3.5.2** *P* **104** *L* **16** # 291

Lo, Willliam Axonne Inc.

Comment Type **E** *Comment Status* **D** *late - EZ*

ENCODE(tx_raw), EBLOCK_T are underlined and not in same font as other text in Figure 191-19. The C and D labels also need changing.

SuggestedRemedy

Fix the fonts

Proposed Response *Response Status* **W**

Cl **191** *SC* **191.3.5.2** *P* **105** *L* **6** # 293

Lo, Willliam Axonne Inc.

Comment Type **E** *Comment Status* **D** *late - EZ*

The arrow into RX_INIT is misaligned and pokes into the box. Also all the arrow heads do not all look like the same size.

SuggestedRemedy

Realign the arrow. Fix arrow head size

Proposed Response *Response Status* **W**

Cl **191** *SC* **191.3.5.2** *P* **105** *L* **18** # 292

Lo, Willliam Axonne Inc.

Comment Type **E** *Comment Status* **D** *late - EZ*

DECODE(rx_coded), EBLOCK_R are underlined and not in same font as other text in Figure 191-20. The C, D and E labels also need changing.

SuggestedRemedy

Fix the fonts

Proposed Response *Response Status* **W**

Cl **191** *SC* **191.4.2.2.15** *P* **114** *L* **13** # 285

Lo, Willliam Axonne Inc.

Comment Type **T** *Comment Status* **D** *late - CRC*

The CRCout and the diagonal arrow supposed to mean something like a switch. This is a bit confusing and if this is not interpreted as a switch the picutre and the text do not produce the same results.

SuggestedRemedy

See Figure 191-32 for an example on how to fix this.
In line 8 add the sentence:
CRCgen is selected when computing the CRC and CRCout is selected when outputting the 6-bit CRC.

Proposed Response *Response Status* **W**

Cl **191** *SC* **191.5.2** *P* **119** *L* **40** # 303

Razavi, Alireza Eliyan

Comment Type **T** *Comment Status* **X** *late*

191.5.2 states: "The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Tx Clock Generation." This enumeration omits the PHY Link Synchronization function, which is defined as a PMA operating function in 191.5.2.8 with its own state diagram (Figure 191-38) and is shown as the LINK SYNCHRONIZATION functional block in the PMA reference diagram (Figure 191-28) on the same page. The count "five" and the list are inconsistent with both 191.5.2.8 and Figure 191-28, which together establish six PMA operating functions.

SuggestedRemedy

Change "five" to "six" and add PHY Link Synchronization to the list: "The PMA sublayer comprises one PMA Reset function and six simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, PHY Link Synchronization, and Tx Clock Generation." Also confirm whether the following sentence ("All operating functions are started immediately after the successful completion of the PMA Reset function") holds for PHY Link Synchronization, whose start is governed by the AN-enable condition per Figure 191-38; qualify it if not.

Proposed Response *Response Status* **O**

Cl **191** *SC* **191.5.2.4.4** *P* **123** *L* **14** # 305

Razavi, Alireza Eliyan

Comment Type **T** *Comment Status* **X** *late*

In Table 191-6 (Follower Message Field settings) and the associated ordering rules in 191.5.2.4.4 (HS_PATH) and 191.5.2.5.3 (LS_PATH), the Follower must progress such that timing_lock_OK is asserted in an earlier Infofield than loc_rcvr_status: row 2 (timing_lock_OK=1, loc_rcvr_status=0) is a mandatory intermediate step between row 1 and row 3. A Follower that achieves a stable transmit clock and OK local receiver status concurrently is still required to first transmit a Message Field with timing_lock_OK=1 and loc_rcvr_status=0, adding an unnecessary Infofield to startup. Separately, the current ordering rule ("the next Message Field setting shall be ... a row below the current setting") is ambiguous as to whether rows may be skipped and does not explicitly prohibit skipping to the COUNTDOWN row (PMA_state=01) before loc_rcvr_status and timing_lock_OK are set.

SuggestedRemedy

Permit, as an option, the Follower to assert loc_rcvr_status and timing_lock_OK in the same Message Field, while retaining the stepwise progression and prohibiting all other skips and any return to a prior row. (1) In 191.5.2.4.4 and 191.5.2.5.3, replace "the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting" with: "the next Message Field setting shall be either the same Message Field setting or the Message Field setting in the row immediately below the current setting, except that the Follower may advance from the first row of Table 191-6 directly to the third row, asserting loc_rcvr_status and timing_lock_OK in the same Message Field. The Message Field setting shall not change to a row above the current setting." (2) In 191.5.2.6, after "The setting of timing_lock_OK value is implementation specific.", add: "A Follower is permitted to assert timing_lock_OK in the same Message Field in which it first asserts loc_rcvr_status; it is not required to transmit a Message Field with timing_lock_OK = 1 and loc_rcvr_status = 0 beforehand. See 191.5.2.4.4 and 191.5.2.5.3." Table 191-6 is unchanged (all four rows remain valid); the receiver requires no change, as row 3 is already a valid received setting.

Proposed Response *Response Status* **O**

Cl **191** *SC* **191.5.2.4.5** *P* **125** *L* **14** # 286

Lo, Willliam Axonne Inc.

Comment Type **T** *Comment Status* **D** *late - infofield*

The OAMen and VendorSpecificData is not implemented correctly per my previous comment. I think this is a confusion conflating HS_PATH with PHY_S. They are not the same. In this section we are talking about HS_PATH. Explanation:
Let AS be the OAMen advertised bit in PHY_S. Let RD be the bit in PHY_D that reflect the AS bit. In the other direction let AD be the OAMen advertised bit in PHY_D. Let RS be the bit in PHY_S that reflect the AD bit.
Since this is the HS_PATH we need to talk about AS and RD, but instead we are talking about AS and RS here. What may be causing confusion in the text is that we assign 1.2311.1 to both AS and AD and 1.2312.1 to both RD and RS. Note that there is no need to assign the same address to to AS and AD. But since AS and AD are in different devices we chose the same address out of symmetry. Similar for RD and RS.
A similar issue is occurring for VendorSpecificData.

SuggestedRemedy

Change Line 14 from:
The link partner's OAMen is advertised
to:
The value of PHY_S OAMen is reported at the link partner (PHY_D)

Delete Line 19-20 and add:
The VendorSpecificData PHY_S sends to its link partner are bits 1.2316.15:0 (see 45.2.1.249). The value of PHY_S VendorSpecificData is reported at the link partner (PHY_D) in bits 1.2317.15:0 (see 45.2.1.250).

Proposed Response *Response Status* **W**

Cl **191** *SC* **191.5.2.5.4** *P* **127** *L* **36** # 287

Lo, Willliam — Axonne Inc.

Comment Type **T** *Comment Status* **D** *late - infofield*

Same problem as above but this time we don't even reference the address. As noted in the previous comment AS and AD do not necessarily need to be in the same register address and we cannot infer that, hence we need to state the details even though it may look like we are saying the same thing twice because we chose the same register address to represent AS and AD.

SuggestedRemedy

Line 37:
Remove the entire line and replace with:
OAMen indicates PHY_D OAM capability is enabled. The OAMen is advertised in bit 1.2311.1. (See 45.2.1.244.5 for the definition of bit 1.2311.1.) The value of PHY_D OAMen is reported at the link partner (PHY_S) in bit 1.2312.1. (See 45.2.1.245.4 for the definition of bit 1.2312.1.)

Insert the following at line 42.
The VendorSpecificData PHY_D sends to its link partner are bits 1.2316.15:0 (see 45.2.1.249). The value of PHY_D VendorSpecificData is reported at the link partner (PHY_S) in bits 1.2317.15:0 (see 45.2.1.250).

Delete line 28-29 and add:
The InterleaverDepth request PHY_D sends to its link partner is bits 1.2311.12:11 (see 45.2.1.244.1). The value of PHY_D InterleaverDepth reported at the link partner (PHY_S) in bits 1.2312.12:11 (see 45.2.1.245.1).

Delete line 35 and add:
The value of PHY_D PrecodeSel is reported at the link partner (PHY_S) in bit 1.2312.3:2 (see 45.2.1.245.3).

Proposed Response *Response Status* **W**

Cl **191** *SC* **191.5.2.8** *P* **133** *L* **33** # 301

Razavi, Alireza — Eliyan

Comment Type **T** *Comment Status* **X** *late*

191.5.2.8 scopes Figure 191-38 to the case where Auto-Negotiation is disabled or not implemented, yet (a) the state diagram's global entry into SYNC_DISABLE and its power-up behavior depend on power_on, mr_main_reset, and mr_autoneg_enable, all defined by cross-reference to 98.5.1 (Clause 98 Auto-Negotiation). When AN is not implemented, Clause 98 is absent and these variables have no defined source, leaving the power-up entry undefined for a PHY that does not implement AN. (b) The diagram also handles the AN-enabled case (entry to SYNC_DISABLE on mr_autoneg_enable), which the scoping sentence assigns to Clause 98 - making it ambiguous whether this diagram or the Clause 98 state machine governs the PHY when AN is enabled.

SuggestedRemedy

Define power_on and mr_main_reset (and any reset/enable conditions the Link Synchronization machine requires) independently of 98.5.1 for the AN-not-implemented case, or state that they are instantiated regardless of whether Clause 98 is implemented. Clarify the handoff between Figure 191-38 and the Clause 98 state machine when mr_autoneg_enable is asserted, so the AN-enabled behavior is defined in exactly one place.

Proposed Response *Response Status* **O**

Cl **191** *SC* **191.5.2.8** *P* **135** *L* **44** # 288

Lo, Willliam — Axonne Inc.

Comment Type **E** *Comment Status* **D** *late - EZ*

LEADER TX case incorrect

SuggestedRemedy

Change to Leader TX

Proposed Response *Response Status* **W**

Cl **191** *SC* **191.5.2.8** *P* **138** *L* **35** # 289

Lo, Willliam — Axonne Inc.

Comment Type **E** *Comment Status* **D** *late - EZ*

Block of text above SYNC_DISABLE wrong font

SuggestedRemedy

Fix font and remove underline.

Proposed Response *Response Status* **W**

Cl **191** *SC* **191.5.2.8.2** *P* **136** *L* **19** # 300

Razavi, Alireza Eliyan

Comment Type **E** *Comment Status* **X** *late*

In 191.5.2.8.2, the timer is defined as "break_link_timer_[HSM]" with a cross-reference to 98.5.2,. Figure 191-38 uses the bare name break_link_timer / break_link_timer_done with no subscript,

SuggestedRemedy

change the definition in 191.5.2.8.2

Proposed Response *Response Status* **O**

Cl **191** *SC* **191.5.2.8.4** *P* **138** *L* **15** # 299

Razavi, Alireza Eliyan

Comment Type **T** *Comment Status* **X** *late*

In Figure 191-38, the SIGDET_WAIT exit to REPLY_PAUSE is qualified by "send_s_sigdet * single_send_s_detect". Per 191.5.2.8.1, send_s_sigdet = TRUE indicates sufficient SEND_S pulses were detected, and single_send_s_detect = TRUE indicates at least one SEND_S pulse was detected. Any reasonable definition of "sufficient" is >= 1 pulse, so send_s_sigdet = TRUE implies single_send_s_detect = TRUE, making the single_send_s_detect term redundant (it cannot be FALSE while send_s_sigdet is TRUE). The corresponding Leader transitions in LEADER_PAUSE use bare send_s_sigdet without this qualifier, so the two roles express the same "sufficient pulses detected" decision inconsistently.

SuggestedRemedy

Remove single_send_s_detect from the SIGDET_WAIT exit so it reads "send_s_sigdet" (matching the Leader side).

Proposed Response *Response Status* **O**

Cl **191** *SC* **191.5.2.8.4** *P* **138** *L* **33** # 298

Razavi, Alireza Eliyan

Comment Type **T** *Comment Status* **X** *late*

In Figure 191-38, the global transition into SYNC_DISABLE includes a term asserted when force_phy_type equals none of the six defined values (2.5G+100M, 5G+100M, 10G+100M, 100M+2.5G, 100M+5G, 100M+10G). However, the only exit from SYNC_DISABLE is qualified solely by !mr_autoneg_enable; it does not require force_phy_type to be valid. Because the entry is a global (continuously evaluated) transition, a PHY configured with an unsupported force_phy_type while mr_autoneg_enable = FALSE will leave SYNC_DISABLE on !mr_autoneg_enable and be immediately returned by the global arc. The state machine can never reach TRANSMIT_DISABLE, so it is held in (or oscillates around) SYNC_DISABLE with no productive exit. Entry is gated on invalid configuration but exit is not gated on valid configuration - an asymmetry creating a reachability/liveness defect.

SuggestedRemedy

Gate the SYNC_DISABLE exit on a supported force_phy_type. Change the exit condition from "!mr_autoneg_enable" to "!mr_autoneg_enable * (force_phy_type = 2.5G+100M + force_phy_type = 5G+100M + force_phy_type = 10G+100M + force_phy_type = 100M+2.5G + force_phy_type = 100M+5G + force_phy_type = 100M+10G)".

Proposed Response *Response Status* **O**

Cl **191** *SC* **191.5.2.8.4** *P* **138** *L* **41** # 302

Razavi, Alireza Eliyan

Comment Type **T** *Comment Status* **X** *late*

In Figure 191-38, state LINK_GOOD_CHECK has two exit transitions that are not mutually exclusive: "link_status = OK" (to LINK_GOOD) and "fail_inhibit_timer_done + training_failure" (to connector A). If link_status becomes OK at the same evaluation in which fail_inhibit_timer_done becomes true (with training_failure = FALSE), both exit conditions are satisfied and no precedence is defined, making the next state ambiguous. This also contradicts the fail_inhibit_timer definition in 191.5.2.8.2, which states a link is considered failed "only if the fail_inhibit_timer has expired and the link has still not gone into the link_status = OK state" - i.e., timer expiry alone should not force the failure exit when the link is OK.

SuggestedRemedy

Qualify the failure exit so it cannot fire when the link is good. Change the LINK_GOOD_CHECK -> A transition from "fail_inhibit_timer_done + training_failure" to "(fail_inhibit_timer_done * link_status = FAIL) + training_failure". Since link_status is exhaustively OK or FAIL, this makes the two LINK_GOOD_CHECK exits mutually exclusive and aligns the diagram with the fail_inhibit_timer definition in 191.5.2.8.2.

Proposed Response *Response Status* **O**

Cl **191** *SC* **191.6.2.4** *P* **145** *L* **39** # 290

Lo, Willliam Axonne Inc.

Comment Type **T** *Comment Status* **D** *late - EZ*

Does testmode 2 using a free running clock make sense at all? At the high speed transmit rate the Follower high speed Transmitter should never output at a frequency that is +1/-20%. The only time this frequency variation is allowed is during linksync and outputting DME SEND_S pulses.

SuggestedRemedy

Propose we remove the text

Proposed Response *Response Status* **W**

Cl **191** *SC* **191.14** *P* **165** *L* **43** # 304

Razavi, Alireza Eliyan

Comment Type **T** *Comment Status* **X** *late*

191.14 places a normative limit (Table 191-24) only on the end-to-end HS_PATH and LS_PATH delays, each of which is defined across two PHYs (e.g., HS_PATH is measured from the PHY_S XGMII to the PHY_D XGMII). There is no normative limit on the individual transmit-portion (XGMII-to-MDI) or receive-portion (MDI-to-XGMII) delay of a single PHY; the allocation between TX and RX is provided only as informative guidance in Annex 191A. Two consequences follow: (1) an individual PHY cannot be tested for delay conformance in isolation, because the only normative limit spans a second, independently-designed PHY; and (2) two PHYs that each assume a different TX/RX allocation can, when paired, exceed the Table 191-24 total even though each PHY individually claims conformance. This undermines multi-vendor interoperability, which is the purpose of the standard. Optional delay reporting detects such a mismatch but does not prevent it, since two conforming-on-paper PHYs can still fail to interoperate.

SuggestedRemedy

Introduce a normative per-PHY delay allocation so that interoperability holds by construction. In Clause 191 (e.g., 191.14 / Table 191-24), specify normative maximum values for the individual transmit-portion and receive-portion delay of each PHY, for both HS_PATH and LS_PATH, chosen such that the sum of the TX and RX sub-limits does not exceed the corresponding Table 191-24 total. This guarantees that any conforming TX paired with any conforming RX meets the end-to-end limit. Retain Annex 191A as informative, illustrating the allocation and the TX_Delay/RX_Delay measurement method (Figure 191A-1). The specific split values should be agreed within the Task Force; the normative requirement is that per-PHY TX and RX sub-limits exist and sum to no more than the Table 191-24 total. Alternatively, add two columns to Table 191-24 (maximum TX delay and maximum RX delay per path) rather than prose sub-limits.

Proposed Response *Response Status* **O**

Cl **192** *SC* **192.1.3** *P* **192** *L* **52** # 306

Maguire, Valerie Copperopolis; aff'l w/ CME Consulting, Microchip, and

Comment Type **E** *Comment Status* **X** *late*

Correct E-Z typos and grammar issues

SuggestedRemedy

P192, L51 and P251, L42:
Replace, "back the PMA TRANSMIT”with “back to the PMA TRANSMIT”

P195, L42:
Replace, "The MDI for a" with "The MDIs for a"

P204, L35:
Replace, "are preceded" with " is preceded"

P208, L31:
Replace, "shown in shown in" with "shown in"

P245, L6:
Replace, "proceed to load in the next" with "proceed to load the next"

P246, L9 and P247, L21:
Replace, "whether MultiGBASE-A OAM message" with "whether the MultiGBASE-A OAM message"

P247, L4:
Replace, "whether valid MultiGBASE-A OAM" with "whether a valid MultiGBASE-A OAM"

P247, L21:
Replace, "in previous MultiGBASE-A OAM frame" with "in the previous MultiGBASE-A OAM frame"

P248, L5:
Replace, "begin transmitting them" with "begin transmitting it"

P254, L28:
Replace, "rollover to zero" with "roll over to zero"

P257, L2:
Replace, "either management configuration " with "either the management configuration "

P257, L2:
Replace, "or selecting the highest mutually" with "or selection of the highest mutually"

P263, L32:
Replace, "currently in either in a silent mode" with "currently in either a silent mode"

P299, L18:

Replace, "one OAM symbols is" with "one OAM symbol is"

Proposed Response *Response Status* **O**