RFER_CNT_LIMIT counts per RFRX_CNT_LIMIT period since the RFER_BAD_RF state can be entered a maximum of RFER_CNT_LIMIT times per RFRX_CNT_LIMIT window.

201.4.8 100M+MultiGBASE-T1/V1 operations, administration, and maintenance (OAM)

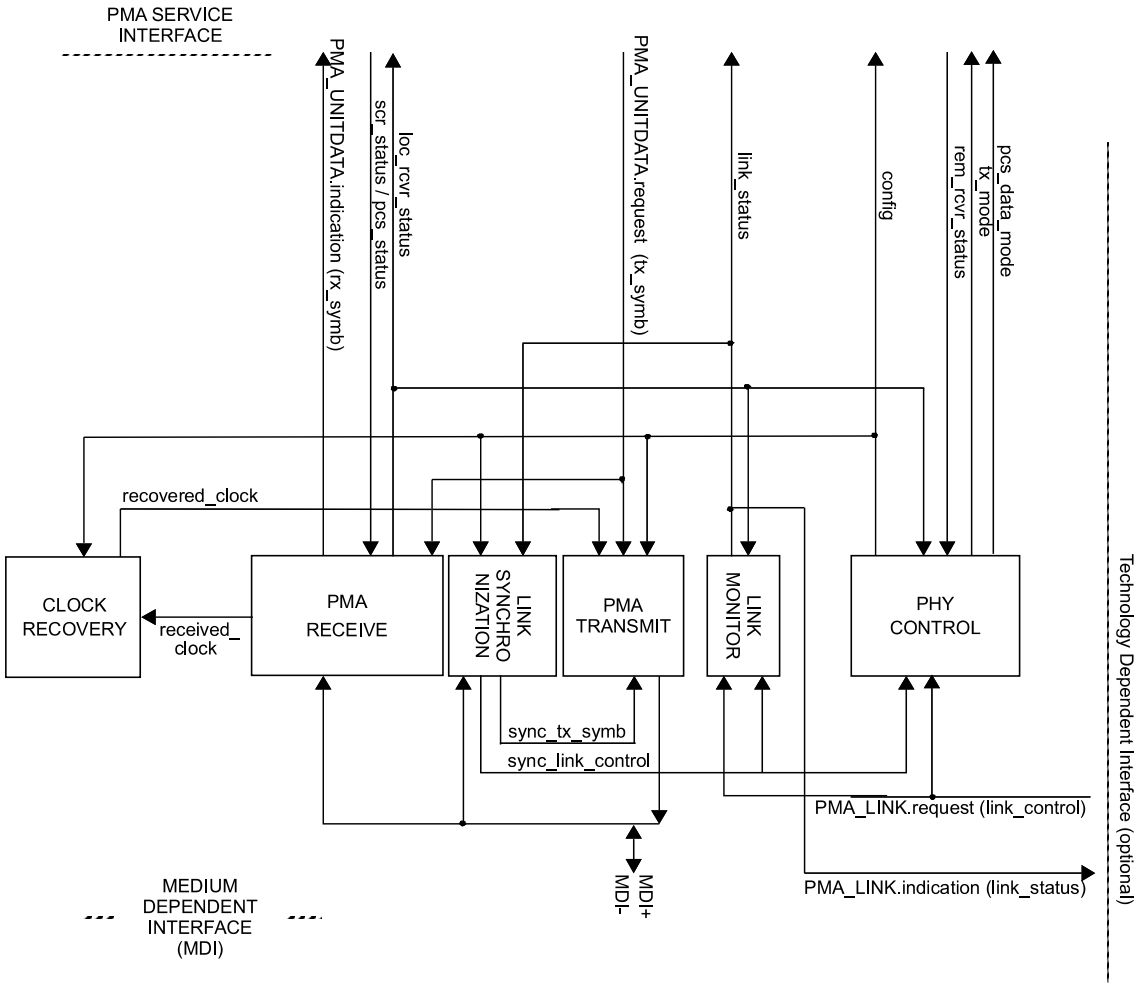
As specified for MultiGBASE-T1 PHYs in 149.3.9.

201.5 Physical Medium Attachment (PMA) sublayer, high speed path (HS_PATH)

201.5.1 PMA functional specifications

The PMA couples messages from the PMA service interface specified in 201.2.2 to the MultiG+100M/100M+MultiGBASE-T1 baseband medium, specified in 201.11 and to the MultiG+100M/100M+MultiGBASE-V1 baseband medium specified in 201.12.

The interface between the PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 201.13 for -T1 and in 201.14 for -V1.



NOTE—The recovered_clock arc is shown to indicate delivery of the recovered clock signal back to PMA TRANSMIT for loop timing.

Figure 201–17—PMA reference diagram

201.5.2 PMA functions

The PMA sublayer comprises one PMA Reset function and five simultaneous and asynchronous operating functions. The PMA operating functions are PHY Control, PMA Transmit, PMA Receive, Link Monitor, and Clock Recovery. All operating functions are started immediately after the successful completion of the PMA Reset function.

The PMA reference diagram, Figure 201–17, shows how the operating functions relate to the messages of the PMA service interface and the signals of the MDI. Connections from the management interface, comprising the signals MDC and MDIO, to other layers are pervasive and are not shown in Figure 201–17.

201.5.2.1 PMA Reset function

The PMA Reset function shall be executed whenever one of the two following conditions occur:

a) Power for the device containing the PMA has not reached the operating state.
b) The receipt of a request for reset from the management entity.

PMA Reset sets pma_reset = ON while any of the above reset conditions hold TRUE. All state diagrams take the open-ended pma_reset branch upon execution of PMA Reset. The reference diagrams do not explicitly show the PMA Reset function.

The MultiG+100M/100M+MultiGBASE-T1/V1 PMA takes no longer than 100 ms to enter the PCS_DATA state after exiting from reset or low power mode (see Figure 201–21).

201.5.2.2 PMA Transmit function

The PMA Transmit function comprises a transmitter to generate a four-level modulated signal for PAM4 and a two-level modulated signal for PAM2 on the single balanced pair of conductors for -T1 or the single coax for -V1. When the PHY Control state diagram (Figure 201–21) is not in the DISABLE_TRANSMITTER state, PMA Transmit shall continuously transmit pulses modulated by the symbols given by tx_symb onto the MDI. During Link Synchronization, when sync_link_control = DISABLE and Auto-Negotiation is either not enabled or is not implemented, the sync_tx_symb output by the PHY Link Synchronization function shall be used in place of tx_symb as the data source for PMA Transmit. When lpi_tx_mode = ALERT, the PN sequence defined in 201.7.3 shall be used in place of tx_symb as the data source for PMA Transmit. The signals generated by PMA Transmit shall comply with the electrical specifications given in 201.8.2.

When the PMA_CONFIG.indication parameter config is LEADER, the PMA Transmit function shall source TX_TCLK from a local clock source while meeting the transmit jitter requirements of 201.8.2.3. The LEADER-FPOLLOWER relationship shall include loop timing. If the PMA_CONFIG.indication parameter config is FOLLOWER, the PMA Transmit function shall source TX_TCLK from the recovered clock of 201.7.4 while meeting the jitter requirements of 201.8.2.3.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

201.5.2.2.1 Global PMA transmit disable

When the PMA_transmit_disable variable is set to TRUE, this function shall turn off the transmitter so that the average launch power of the transmitter is less than –53 dBm.

201.5.2.3 PMA Receive function

The PMA Receive function comprises a receiver for PAM4 and PAM2 on the single balanced pair of conductors for -T1 or the single coax for -V1. PMA Receive contains the circuits necessary to both detect symbol sequences from the signals received at the MDI over the receive pair and to present these sequences to the PCS Receive function. The PMA translates the signals received on the pair into the PMA_UNITDATA.indication parameter rx_symb. The quality of these symbols shall allow RFER of less than 2×10^{-10} after RS-FEC decoding, over a channel meeting the requirements of 201.11 for -T1 and in 201.12 for -V1.

To achieve the indicated performance, it is highly recommended that PMA Receive includes the function of signal equalization .

The PMA Receive function uses the parameters pcs_status and scr_status, and the state of the equalization, and estimation functions to determine the quality of the receiver performance, and generates the loc_rcvr_status variable accordingly. The loc_rcvr_status variable is expected to become NOT_OK when the link partner's tx_mode changes to SEND_Z from any other value (see the PHY Control state diagram in Figure 201–21). The precise algorithm for generation of loc_rcvr_status is implementation dependent.

The receiver uses the sequence of symbols during the training sequence to detect and correct for pair polarity swaps for -T1.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = FAIL and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5 and 45.2.1.250.7.

201.5.2.4 PHY Control function

PHY Control generates the control actions that are needed to bring the PHY into a mode of operation during which frames can be exchanged with the link partner. PHY Control shall comply with the state diagram in Figure 201–21.

During PMA training (TRAINING and COUNTDOWN states in Figure 201–21), PHY Control information is exchanged between link partners with a 12-octet Infofield, which is XORed with the first 96 bits of the 16th partial PHY frame (bits 6750 to 6845). The Infofield is also denoted IF. The link partner is not required to decode every IF transmitted but is required to decode IFs at a rate that enables the correct actions prior to the PAM2 to PAM4 transition.

The 12-octet Infofield shall include the fields in 201.5.2.4.2 through 201.5.2.4.8, also shown in Figure 201–18 and Figure 201–19. Infofield shall be transmitted at least 256 times with each change to octets 7 to 10.

PMA_state = 00

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	PHY Capability Bits	CRC16

Figure 201–18—Infofield TRAINING format

PMA_state = 01

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	DataSwPFC24	CRC16

Figure 201–19—Infofield COUNTDOWN format

201.5.2.4.1 Infofield notation

For all the Infofield notations in the following subclauses, Reserved<bit location> represents any unused values and shall be set to zero on transmit and ignored when received by the link partner. The Infofield is transmitted following the notation where the LSB of each octet is sent first and the octets are sent in increasing number order (that is, the LSB of Oct1 is sent first).

201.5.2.4.2 Start of Frame Delimiter

The start of Frame Delimiter consists of three octets [Octet 1<7:0>, Octet 2<7:0>, Octet 3<7:0>] and shall use the hexadecimal value 0xBBA700. 0xBB corresponds to Octet 1<7:0> and so forth.

201.5.2.4.3 Partial PHY frame count (PFC24)

The partial PHY frame count consists of 3 octets [Oct4<7:0>, Oct5<7:0>, Oct6<7:0>] and indicates the running count of partial PHY frames sent LSB first. There are 16 partial PHY frames per PHY frame and the Infofield is embedded within the 16th partial PHY frame. The first partial PHY frame is zero, thus the first partial PHY frame count field after a reset is 15.

PFC24 continues to run uninterrupted for the duration of the link. The resolution of PFC24 is large enough that it does not rollover during the allotted training time. However, it will rollover if allowed to run indefinitely. PFC24 is defined to rollover to 0 after it reaches 16 776 959.

201.5.2.4.4 Message Field

The Message Field is one octet. For the LEADER, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, en_slave_tx<4>, reserved<3:0>}. For the FOLLOWER, this field is represented by Oct7{PMA_state<7:6>, loc_rcvr_status<5>, timing_lock_OK<4>, reserved<3:0>}.

The two state-indicator bits PMA_state<7:6> shall communicate the state of the transmitting transceiver to the link partner. PMA_state<7:6> = 00 indicates TRAINING, and PMA_state<7:6> = 01 indicates COUNTDOWN.

All possible Message Field settings are listed in Table 201–5 for the LEADER and Table 201–6 for the FOLLOWER. Any other value shall not be transmitted and shall be ignored at the receiver. The Message Field setting for the first transmitted PMA frame shall be the first row of Table 201–5 for the LEADER and the first or second row of Table 201–6 for the FOLLOWER. Moreover, for a given Message Field setting, the next Message Field setting shall be the same Message Field setting or the Message Field setting corresponding to a row below the current setting. When loc_rcvr_status = OK the Infofield variable is set to loc_rcvr_status<5> = 1 and set to 0 otherwise.

Table 201–5—Infofield message field valid LEADER settings

PMA_state<7:6>	loc_rcvr_status	en_slave_tx	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

201.5.2.4.5 PHY capability bits

When PMA_state<7:6> = 00, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the PHY capability bits. Each octet is sent LSB first. See Table 201–7 for the details.

The format of PHY capability bits is Oct10<2:1> = InterleaverDepth[1:0], Oct10<4:3> = PrecodeSel[1:0], Oct10<7> = OAMen, Oct8<7:0> = VendorSpecificData[7:0], and Oct9<7:0> = VendorSpecificData[15:8].

Table 201–6—Infofield message field valid FOLLOWER settings

PMA_state<7:6>	loc_rcvr_status	timing_lock_OK	reserved	reserved	reserved	reserved
00	0	0	0	0	0	0
00	0	1	0	0	0	0
00	1	1	0	0	0	0
01	1	1	0	0	0	0

Table 201–7—PHY capability bits

octet 8								octet 9								octet 10							
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
VendorSpecificData																Reserved	InterleaverDepth		PrecodeSel		Reserved	Reserved	OAMen

OAMen indicates MultiGBASE-T1 OAM capability enable, respectively. The PHY shall indicate the support of these two optional capabilities by setting the corresponding capability bits.

The optional MultiGBASE-T1 OAM capability shall be enabled only if both PHYs set the capability bit OAMen = 1. InterleaverDepth indicates the requested data mode interleaving depth. PrecodeSel indicates the requested precoder, available for 10G only.

The capability bit values shall be considered as valid only when the loc_rcvr_status bit is 1.

The remaining bits shall be reserved and set to 0.

201.5.2.4.6 Data switch partial PHY frame count

When PMA_state<7:6> = 01, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains the data switch partial PHY frame count (DataSwPFC24) sent LSB first. DataSwPFC24 indicates the partial PHY frame count when the transmitter switches from PAM2 to PAM4, which occurs at the start of an RS-FEC superframe. The last value of PFC24 prior to the transition is DataSwPFC24 – 1. DataSwPFC24 shall be set to an integer multiple of 16. When the value of DataSwPFC24 is a multiple of 16 the switch from PAM2 to PAM4 occurs on a PHY frame boundary. DataSwPFC24 shall be a minimum of 4081 and a maximum of 4785 from the current PFC24 value.

201.5.2.4.7 Reserved fields

When PMA_state<7:6> is greater than 01, then [Oct8<7:0>, Oct9<7:0>, Oct10<7:0>] contains a reserved field. All Infofield fields denoted reserved are reserved for future use.

201.5.2.4.8 CRC16

CRC16 (2 octets) shall implement the CRC16 polynomial $(x + 1)(x^{15} + x + 1)$ of the previous 7 octets, Oct4<7:0>, Oct5<7:0>, Oct6<7:0>, Oct7<7:0>, Oct8<7:0>, Oct9<7:0>, and Oct10<7:0>. The CRC16 shall produce the same result as the implementation shown in Figure 201–20. In Figure 201–20 the 16 delay elements S0,..., S15, shall be initialized to zero. After initialization, the switch is set to CRCgen, as shown in Figure 201–20, and Oct4 through Oct10 are used to compute the CRC16 output. After all 7 octets have been processed, the switch is disconnected (setting CRCout) and the 16 values stored in the delay elements are transmitted in the order illustrated, first S15, followed by S14, and so on, until the final value S0.

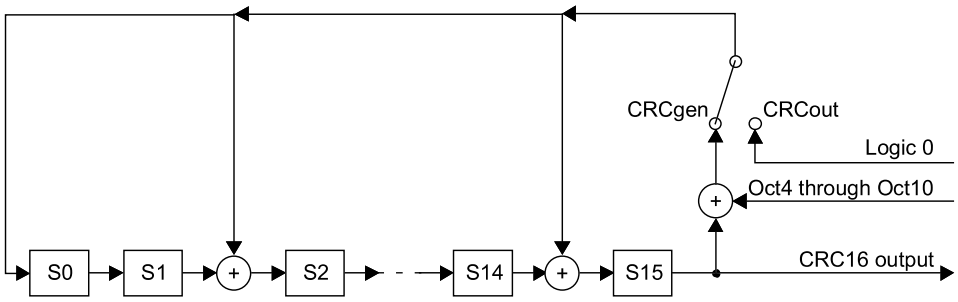


Figure 201–20—CRC16

201.5.2.4.9 PMA MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA. Mapping of MDIO control variables to PMA control variables is shown in Table 201–8. Mapping of MDIO status variables to PMA status variables is shown in Table 201–9.

Table 201–8—MDIO/PMA control variable mapping

MDIO control variable	PMA register name	Register/bit number	PMA control variable
Reset	PMA/PMD control 1 register/ MultiGBASE-T1/V1 PMA control register	1.0.15 / 1.2309.15	pma_reset
Transmit disable	MultiGBASE-T1/V1 PMA control register	1.2309.14	PMA_transmit_disable

Table 201–9—MDIO/PMA status variable mapping

MDIO status variable	PMA register name	Register/bit number	PMA status variable
Receive fault	MultiGBASE-T1/V1 PMA status register	1.2310.1	PMA_receive_fault

201.6 Physical Medium Attachment (PMA) sublayer, low speed path (LS_PATH)

The low speed PMA Transmit function comprises a transmitter to generate a DME signal on the MDI interface. See 201.4.2.2.16 for details on the DME symbols.