TDD Baseline Proposal for Supporting Longer Cable Lengths

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Introduction

- **While the maximum link segment delay of the current TDD proposal supports 20m coaxial cables, some participants have expressed interest in supporting cable lengths up to 30m**

- **This contribution proposes a modification to the TDD proposal to allow propagation delays of up to 160ns, which has been shown to enable 30m coaxial cable support**
  - This matches the ACT maximum link segment delay

- **The additional reach is achieved with no change to the proposed TDD upstream and downstream symbol rates**
  - Consequently, there is no change to the analysis (e.g., for the AFE and PoC filters) that has been submitted for the current TDD proposal

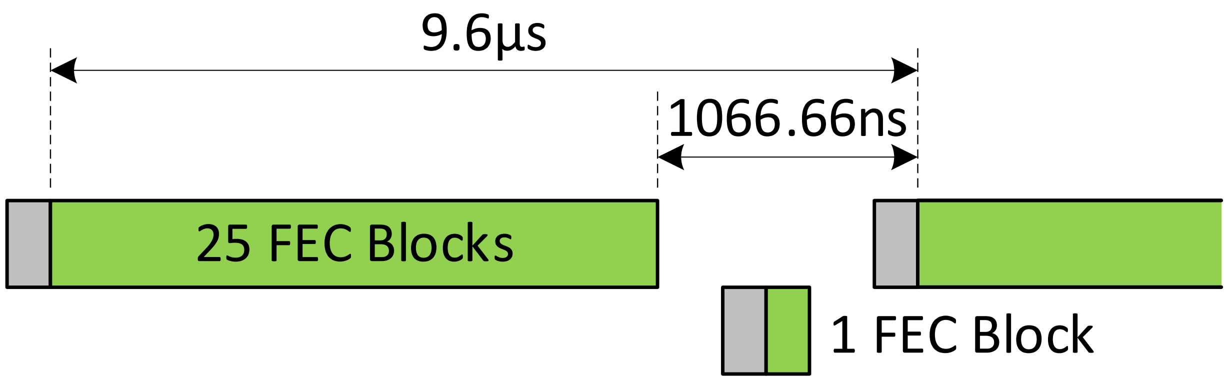
Analysis

- **The inter-burst gap (IBG) time between the upstream and downstream bursts restricts the cable length that can be supported without interference between the bursts**

- **We note that an RS(128,122) is simply a shorted version of the FEC RS(130,124) FEC of the current TDD baseline for the low-speed direction.**
  - Using the RS(128,122) FEC for the HS instead of the current RS(130,122) reduces the HS burst length
  - Consequently, the IBG can be increased without changing the transmitted burst symbol rates
  - Since the RS(128,122) is a shortened version of the RS(130,124) used in the LS direction, the performance will be equivalent for both directions.

- **Rather than having support for both the current and new formats, it is proposed that all TDD interfaces use the version shown in this presentation**

TDD Baseline for Longer Reach



Ethernet Packets Boundary	64b/65b encoding
Speed Grades (@ xMII)	**Forward Link:** 2.5Gbps, 5Gbps & 10Gbps **Reverse Link:** 100Mbps (PAM2, 2.5Gbps line rate)
Modulation	**PAM2** for 2.5Gbps and 5Gbps **PAM4** for 10Gbps
Baud Rate	3.0Gsps for 2.5Gbps (forward and reverse link) 6.0Gsps for 5Gbps and 10Gbps (forward link)
TDD Cycle	9.6µs for ALL speed grades
FEC Block Period	341.33ns DS and 346.66ns US for ALL speed grades

Longer Reach TDD Baseline (cont.)

HS FEC Type	**S = 8bit Reed-Solomon Code** RS(128S, 122S), L=1 for 2.5Gbps (120Byte at XGMII, 15 x 65b+1b OAM) RS(128S, 122S), L=2 for 5.0Gbps (240Byte at XGMII, 30 x 65b+2b OAM) RS(128S, 122S), L=4 for 10Gbps (480Byte at XGMII, 60 x 65b+4b OAM) L= 2 and 4 shows number of interleaved RS codes
LS FEC Type	**S = 8bit Reed-Solomon Code** RS(130S, 124S), L=1 for 100Mbps (120Byte at XGMII, 15 x 65b+17b OAM)
IBG (Inter Burst Gap) normal mode transmit gap	2 x 176ns per TDD cycle
Total Refresh (Resync) Sequence per TDD cycle	368ns for all rates

- Notes:
  - The resulting TDD cycle length is:
= (HS burst data length) + (LS burst data length) + (total resync) + (total IBG)
= (25 x 341.33) + 346.66 + 368 + (2 x 176) = 9.6µs
  - In order to maintain integer multiples of (16 bits / 3 Gbps) for the bursts and IBG, the LS refresh header is decreased from 640 to 624 bits

Proposed Clause 202 Updates (1)

Note that the proposed updates in this presentation are based on 802.3dm D0pa

- **Clause 202.1.4.1, pp. 147, update the two paragraphs beginning at line 10:**

  Next, a 1-bit OAM field is appended to form a 976-bit block. A number, L (L = 1 for 2.5 Gb/s, L = 2 for 5 Gb/s, L = 4 for 10 Gb/s), of these 976-bit blocks are formed into an RS-FEC input superframe, then encoded by the RS-FEC ~~(130, 122, 2^8)~~ (128, 122, 8) and the round-robin interleaving as described in 202.3.2.2.15. The RS-FEC output superframe consists of L × 1040 bits. The duration of the superframe is ~~1040~~ 1024 / 3 ns.

  NOTE—Duration = L × ~~1040~~ 1024 bits / modulation order / baud rate. For 10 Gb/s, L Duration = 4 × ~~1040~~ 1024 / 2 / 6 GHz; for 5 Gb/s, Duration = 2 × ~~1040~~ 1024 / 1 / 6 GHz; for 2.5 Gb/s, DurationL = 1 × ~~1040~~ 1024 / 1 / 3 GHz.

- **Clause 202.3.2.2, pp. 162, update the paragraph beginning at line 45:**

  For HS_TX, … L-interleaved RS-FEC(~~130~~128,122) superframe which adds L × 64 parity bits, shown in Figure 202–6. 25 such superframes are formed for one data payload. L = 1 for 2.5 Gb/s and L = 2 for 5 Gb/s. For 2.5 Gb/s and 5 Gb/s PAM2 transmission, the resulting L × ~~1040~~ 1024 × 25 bits are then scrambled. These bits are then mapped, one at a time, into a PAM2 symbol. L = 4 for 10 Gb/s PAM4 transmission. The resulting L × ~~1040~~ 1024 × 25 bits are then scrambled. …

Proposed Clause 202 Updates (2)

- **Clause 202.3.2.2**

pp. 162 update the paragraph beginning at line 45:

For HS_TX, … L-interleaved RS-FEC (~~130~~128,122) superframe which adds L × 64 parity bits, shown in Figure 202–6. 25 such superframes are formed for one data payload. L = 1 for 2.5 Gb/s and L = 2 for 5 Gb/s. For 2.5 Gb/s and 5 Gb/s PAM2 transmission, the resulting L × ~~1040~~ 1024 × 25 bits are then scrambled. These bits are then mapped, one at a time, into a PAM2 symbol. L = 4 for 10 Gb/s PAM4 transmission. The resulting L × ~~1040~~ 1024 × 25 bits are then scrambled. …

pp. 163 update the paragraph beginning at line 19:

… For HS_TX PHY, during transmission, the 15 blocks of 65B encoded bits are appended with a 1-bit OAM field to form the RS-FEC input frame. During data encoding, HS_TX PCS Transmit utilizes L-interleaved (L = 1 for 2.5 Gb/s, L = 2 for 5 Gb/s, or L = 4 for 10 Gb/s) Reed-Solomon encoders to generate and append ~~64~~48 parity check bits to form ~~1040~~ 1024 -bit (~~130~~128,122) RS-FEC frames that are interleaved into an L-interleaved RS-FEC Superframe.

Proposed Clause 202 Updates (3)

- **Clause 202.3.2.2.2, pp. 165, line 21:**
  Replace “RS-FEC(130,122)” with “RS-FEC(128,122)”

- **Clause 202.3.2.2.2, pp. 165, line 23:**
  Replace “64-bit parity” with “48-bit parity”

- **Clause 202.3.2.2.2, pp. 165, line 27:**
  Replace “1040 symbols” with “1024 symbols”

- **Clause 202.3.2.2.2, pp. 165, line 28:**
  Change the labels of the last two symbol blocks from $PAM2_{1038}$ and $PAM2_{1039}$ to be $PAM2_{1022}$ and $PAM2_{1023}$

- **Clause 202.3.2.2.2, pp. 165, line 34:**
  Replace “520 symbols” with “512 symbols”

- **Clause 202.3.2.2.2, pp. 165, line 35:**
  Change the labels of the last two symbol blocks from $PAM4_{518}$ and $PAM4_{519}$ to be $PAM4_{510}$ and $PAM4_{511}$

Proposed Clause 202 Updates (4)

- **Clause 202.3.2.2.13, pp. 170, line 8:**
  Replace "1040" with "1024"

- **Clause 202.3.2.2.13, pp. 170, line 10:**
  Replace "520" with "512"

- **Clause 202.3.2.2.14, pp. 170, line 27:**
  Replace "1040" with "1024"

- **Clause 202.3.2.2.16, pp. 171, line 10:**
  Replace "$m_{122 \times L-1}, m_{122 \times L-1}, \ldots, m_1, m_0, p_{1,7}, \ldots, p_{L,7}, \ldots, p_{1,0}, \ldots, p_{L,0}$" with
  "$m_{122 \times L-1}, m_{122 \times L-1}, \ldots, m_1, m_0, p_{1,5}, \ldots, p_{L,5}, \ldots, p_{1,0}, \ldots, p_{L,0}$" **(i.e., change the second subscripts of the first two "*p*" terms from 7 to 5)**

Proposed Clause 202 Updates (4)

- **Clause 202.3.2.2.16, pp. 171, line 20:**

  Change the last two terms of the Encoder #1 output string from "$p_{1,7}$, …, $p_{1,0}$" to "$p_{1,5}$, …, $p_{1,0}$"

- **Clause 202.3.2.2.16, pp. 171, line 25:**

  Change the last two terms of the Encoder #2 output string from "$p_{2,7}$, …, $p_{1,0}$" to "$p_{2,5}$, …, $p_{1,0}$"

- **Clause 202.3.2.2.16, pp. 171, line 33:**

  Replace "$m_{122 \times L-1}$, $m_{122 \times L-2}$, …, m_1, m_0, $p_{1,7}$, …, $p_{L,7}$, …, $p_{1,0}$, …, $p_{L,0}$" with "$m_{122 \times L-1}$, $m_{122 \times L-2}$, …, m_1, m_0, $p_{1,5}$, …, $p_{L,5}$, …, $p_{1,0}$, …, $p_{L,0}$"

- **Clause 202.3.2.2.16, pp. 171, line 36:**

  Change the last two terms of the Encoder #1 output string from "$p_{L,7}$, …, $p_{L,0}$" to "$p_{L,5}$, …, $p_{L,0}$"

Proposed Clause 202 Updates (5)

- **Clause 202.3.2.2.16, pp. 171, line 45:**

  Replace this paragraph as follows:

  "The PCS sublayer employs a Reed-Solomon code operating over the Galois Field GF(28) where the symbol size is 8 bits. In the LS direction, the encoder processes k 8-bit RS FEC message symbols to generate (130-k) 8-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of 130 8-bit RS-FEC symbols. In the HS direction, the encoder processes k 8-bit RS FEC message symbols to generate (128-k) 8-bit RS-FEC parity symbols, which are then appended to the message to produce a codeword of 128 8-bit RS-FEC symbols. k = 124 ~~and k = 122 are~~ is adopted for 100M+MultiG BASE-T1/V1LEADER and k = 122 is adopted for the ~~are~~ MultiG+100MBASE-T1/V1FOLLOWER ~~respectively~~. For the purposes of this clause, ~~a~~ the respective particular Reed-Solomon code is denoted RS(~~130~~n,k), where n designates the FEC code block with n=130 for the LS and n=128 for the HS direction."

- **Clause 202.3.2.2.16, pp. 172, line 3:**

  In equation 202-1, replace "130" with "n" in three places and "129" with "n-1" in two places

- **Clause 202.3.2.2.16, pp. 172, line 13:**

  Replace equation 202-2 with "$m(x) = m_{k-1}x^{n-1} + m_{k-2}x^{n-2} + \ldots + m_1 x^{n-k+1} + m_0 x^{n-k}$"

Proposed Clause 202 Updates (6)

- ❑ **Clause 202.3.2.2.16, pp. 172, line 33:**

  Replace “130” with “128”

- ❑ **Clause 202.3.2.2.16, pp. 172, line 40:**

  Replace “$p_{130\text{-}k\text{-}1}$” with “$p_{n\text{-}k\text{-}1}$”

- ❑ **Clause 202.3.2.2.16, pp. 172, line 44:**

  In equation 202-3, replace “130” with “*n*” (three places)

- ❑ **Clause 202.3.2.2.16, pp. 173, line 14:**

  In Figure 202-9, replace “130” with “*n*” (three places) and at the Output, replace C_{129} and C_{128} with $C_{n\text{-}1}$ and $C_{n\text{-}2}$

- ❑ **Clause 202.3.2.2.16, pp. 173, line 37:**

  In Table 202-4, replace “RS-FEC(130,122)” with “RS-FEC(128,122)” in the heading of the third column

Proposed Clause 202 Updates (7)

- **Clause 202.3.2.2.16, pp. 173, line 38:**

  Since the RS(130,124) and RS(128,122) FEC share the same generator polynomial coefficients, replace the coefficient data in the last column of Table 202-4 to be identical with the current middle column. Alternatively, delete the last column and modify the table header and/or table caption to indicate that the values in the resulting single coefficient column apply to both the RS(130,124) and RS(128,122).

Proposed Clause 202 Updates (8)

- **Clause 202.3.2.2.17, pp. 171-173, update as follows:**

  Replace “1040” with “1024”

- **Clause 202.3.5.1, pp. 182, line 33:**

  In the middle column of Table 202-5, replace “640” with “624” in the last two table rows

- **Clause 202.3.2.3, pp. 178, line 15:**

  Replace “RS-FEC(130,122)” with “RS-FEC(128,122)”

- **Clause 202.3.2.3, pp. 178, line 19:**

  Replace “1040” with “1024”

- **Clause 202.3.2.4, pp. 178, line 20:**

  Change the labels of the last two symbol blocks from $PAM2_{1038}$ and $PAM2_{1039}$ to be $PAM2_{1022}$ and $PAM2_{1023}$

Proposed Clause 202 Updates (9)

- **Clause 202.3.2.4, pp. 178, line 24:**
  Replace “$PAM2_{n+1039}$“ with “$PAM2_{n+1023}$“
- **Clause 202.3.2.3, pp. 178, line 26:**
  Replace “520” with “512”
- **Clause 202.3.2.3, pp. 178, line 27:**
  Change the labels of the last two symbol blocks from $PAM4_{518}$ and $PAM4_{519}$ to be $PAM4_{510}$ and $PAM4_{511}$
- **Clause 202.3.2.3, pp. 178, line 31:**
  Replace “$PAM2_{n+519}$“ with “$PAM2_{n+511}$“
- **Clause 202.3.2.3.1, pp. 178, line 48:**
  Replace “rx_PAM2_1039” with “rx_PAM2_1023”
- **Clause 202.3.2.3.1, pp. 178, line 50:**
  Replace “rx_PAM4_519” with “rx_PAM4_511“

Proposed Clause 202 Updates (10)

- **Clause 202.7.1.6, pp. 178, line 7:**
  Consistent with 201.11.1.6, replace the current sentence with: "The maximum link delay of each MultiG+100M/100M+MultiGBASE-T1 link shall be 160 ns"

- **Clause 202.7.1.6, pp. 230, line 15:**
  Consistent with 201.12.1.6, replace the current sentence with : "The maximum link delay of each MultiG+100M/100M+MultiGBASE-T1 link shall be 160 ns"

Conclusions

- Key points:
  - The proposed TDD modification supports propagation delays of up to 160ns, which matches the ACT link segment delay parameter.
  - The proposed modification has no impact on the TDD transmitted symbol rate
- Since the proposed FEC provides identical performance for both transmission directions, we recommend adopting this proposal as the single option for TDD

Thank You