

Complexity and Integration of TDD-based PHY at the Camera Side

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Contributors

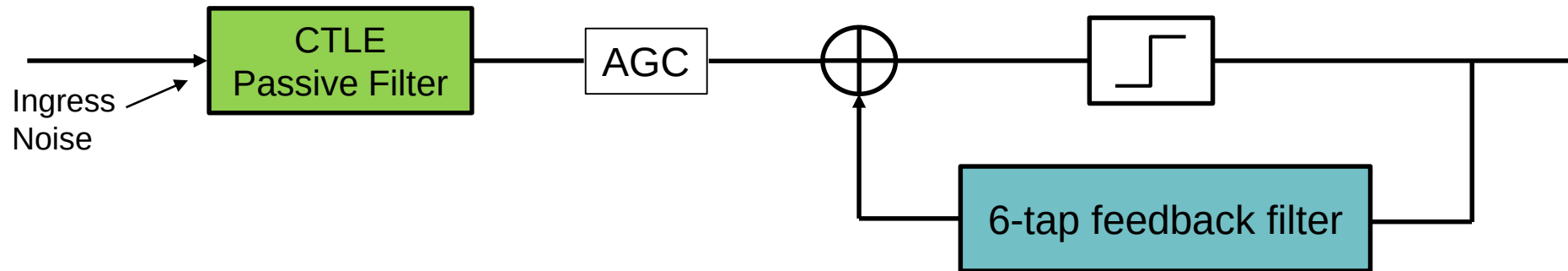
- Kambiz Vakilian, Broadcom Corporation

Foreword

- A TDD-based PHY design was proposed for 802.3dm camera Link¹. The TDD reverse link runs at 3Gsps with PAM2 modulation and ~6% duty cycle (effective bit rate of 100Mbps).
- A camera side equalizer with 6-tap DFE was verified in simulations to provide better than 30dB decision point SNR for a typical link segment . The simulation includes PoC filter distortion, link segments with multiple inline connectors and assumes a noise floor of -145dBm/Hz.
- The implementation complexity (area) and power is estimated for the 3Gsps Camera side transceiver in this presentation.
- A comparison with incumbent discrete PHY implementations and integration with image sensors is discussed for multiple technology node sizes.

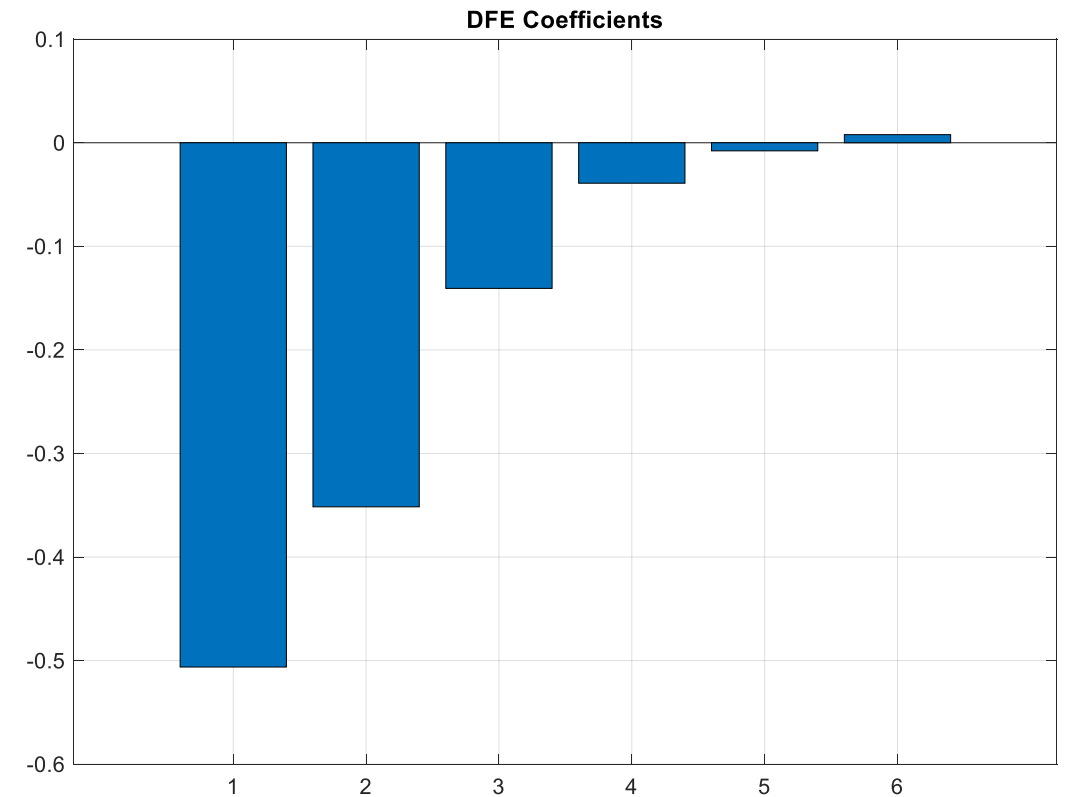
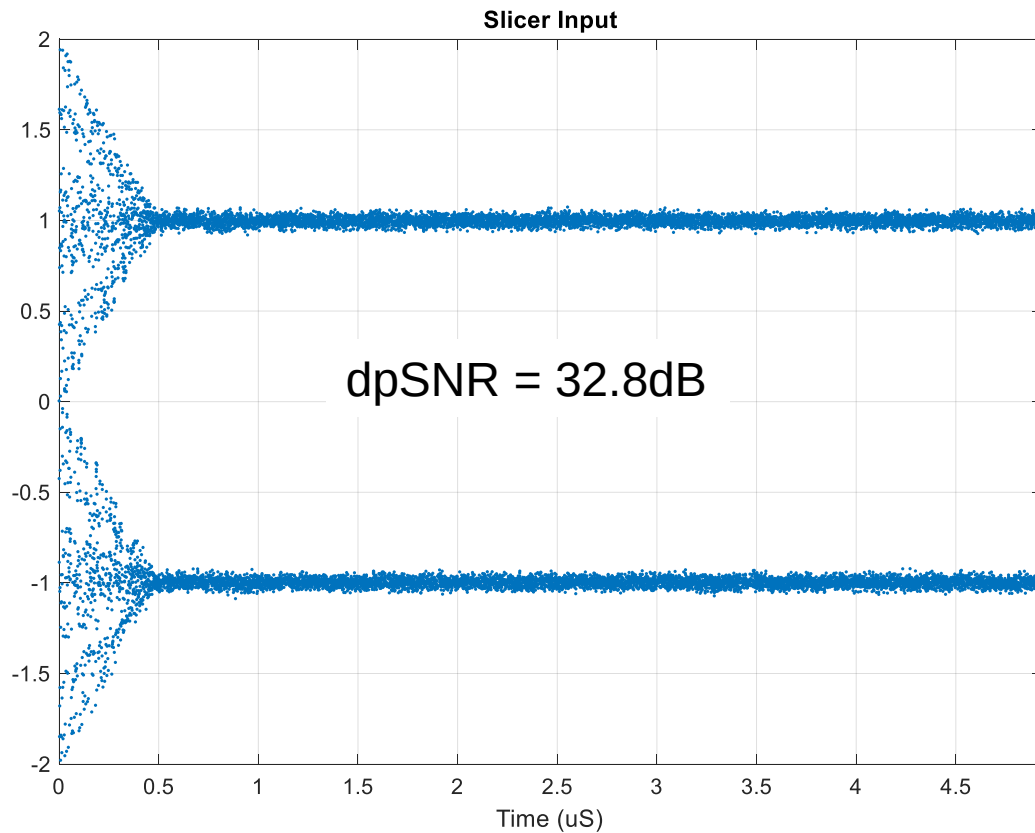
1- https://www.ieee802.org/3/dm/public/0125/Chini_3dm_01a_0125.pdf

3Gbps Equalizer



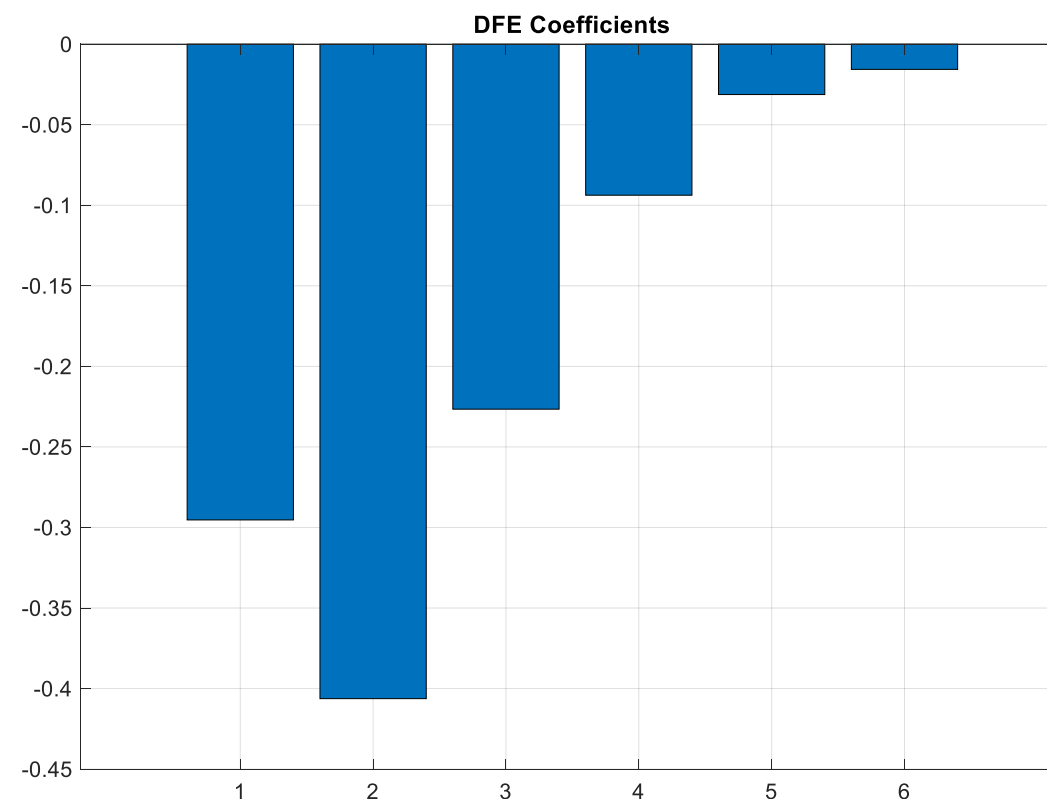
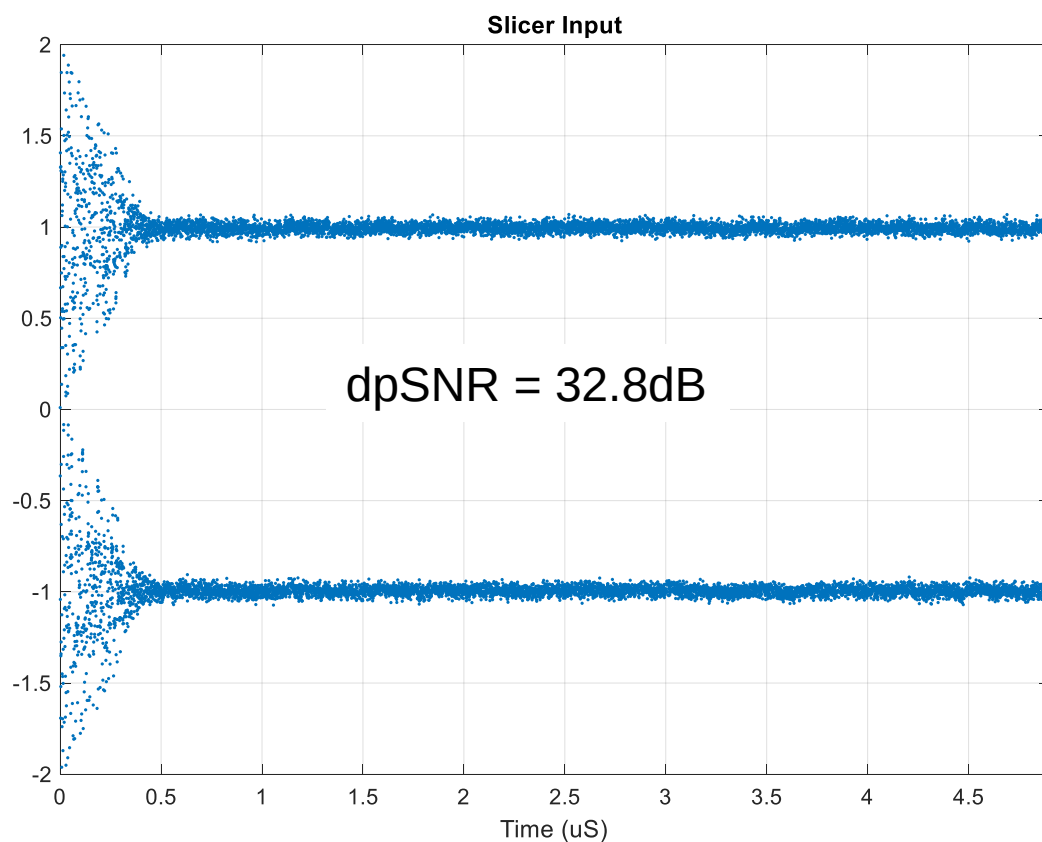
- The CTLE is a passive filter and not adapted to the cable length (high pass and low pass).
- The feedback filter is adapted to the cable length using sign-LMS algorithm.
- The adaptation is performed once every 8 symbols at 375MHz. After initial adaptation, the filter updates may be reduced to periods longer than 1ms.
- Given no FFE taps used and baud rate is 3Gbps, the transceiver can be implemented with a mixed mode technology and feedback filter without unrolling the DFE taps.
- The power consumed in the 6-tap filter is mostly scaled with the baud rate and it drops during the reverse link silent periods.
- The same equalizer type can operate in both sides of the link when operating at 2.5Gbps/100Mbps mode.

Simulation results: Link Segment of 3m



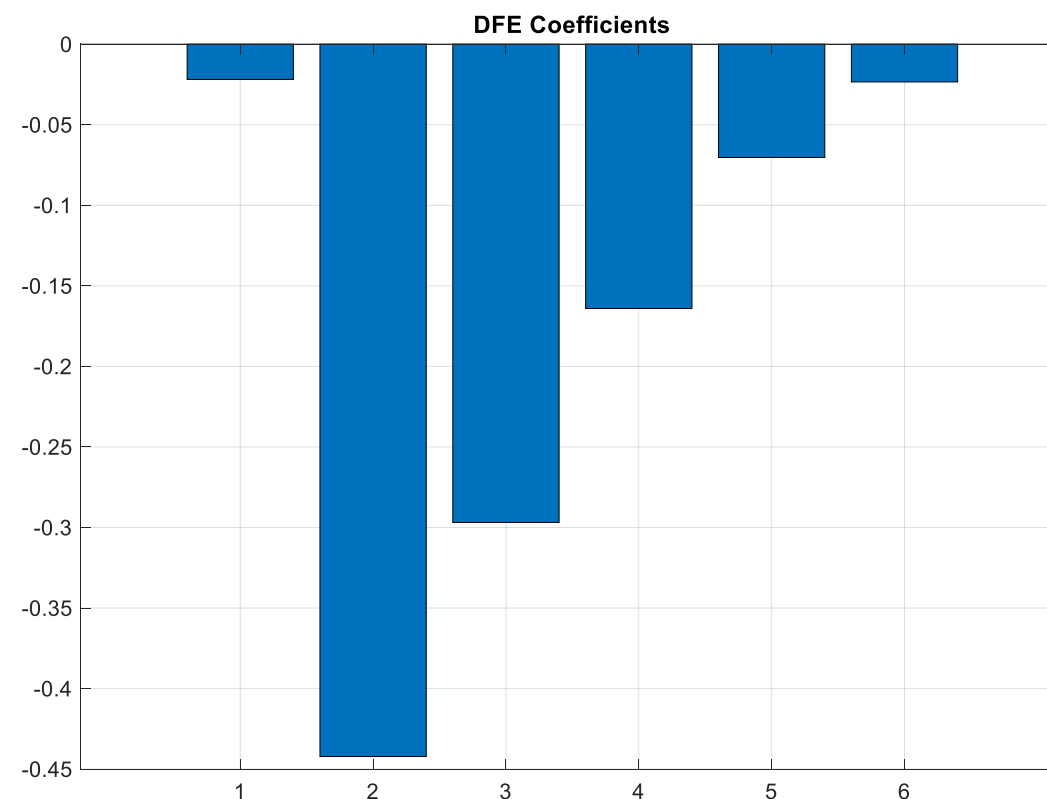
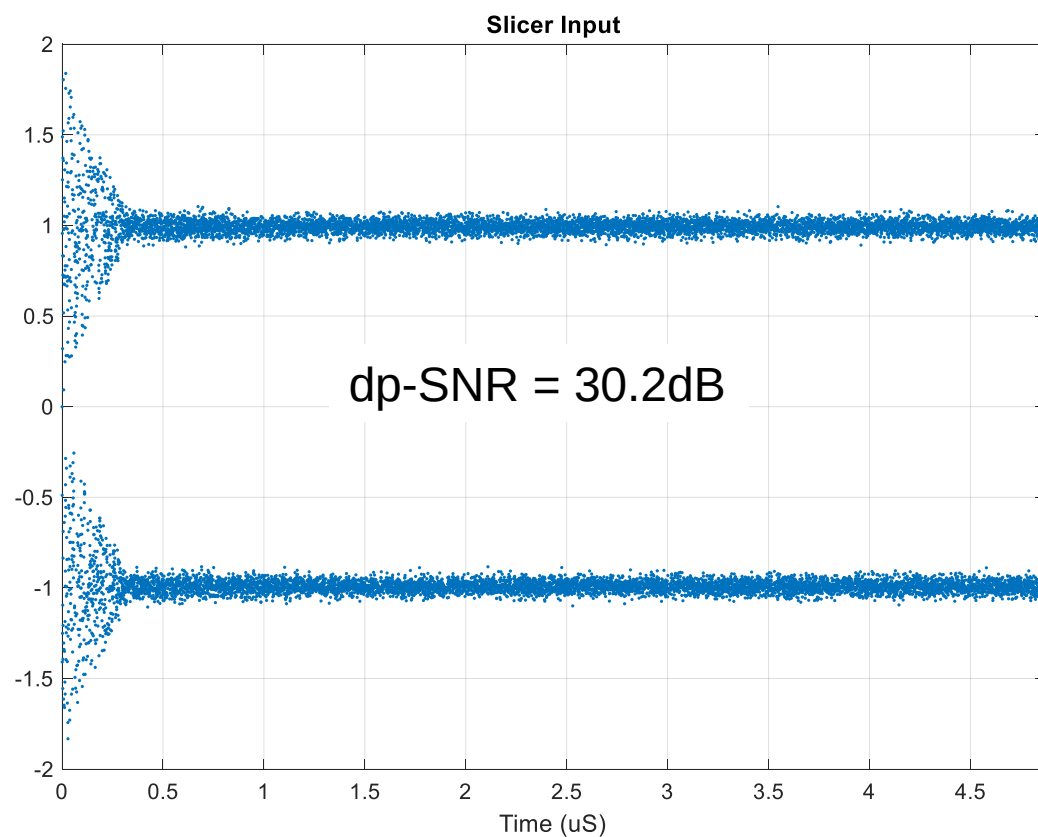
- The Link Segment is a 3m cable with no inline connector

Simulation results: Link Segment of 10.2m



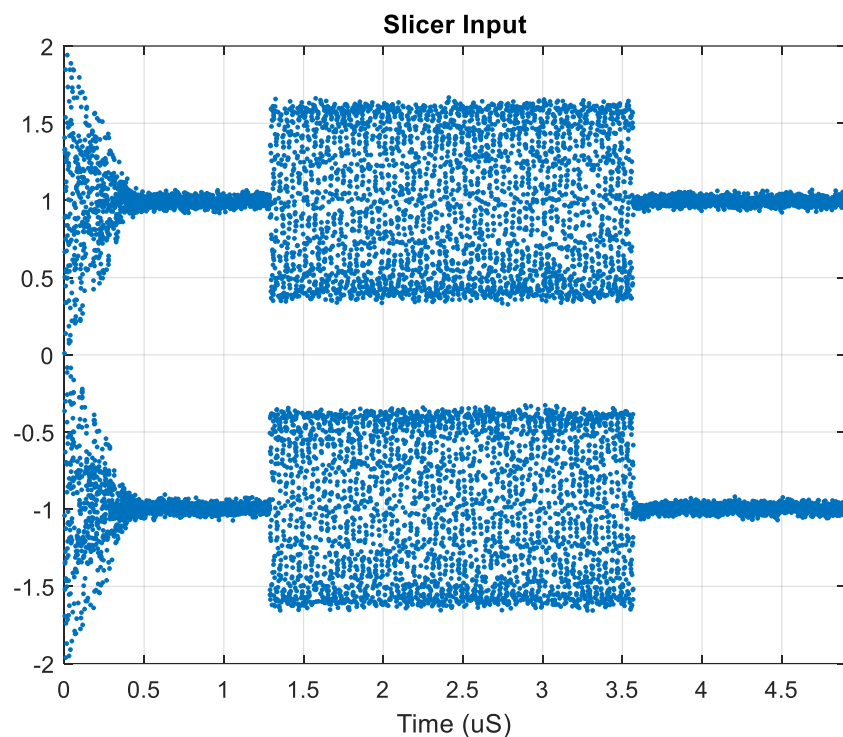
- The Link Segment is a concatenation of smaller cables: $3\text{m} + 0.6\text{m} + 3\text{m} + 0.6\text{m} + 3\text{m} = 10.2\text{m}$

Simulation results: Link Segment of 17.4m

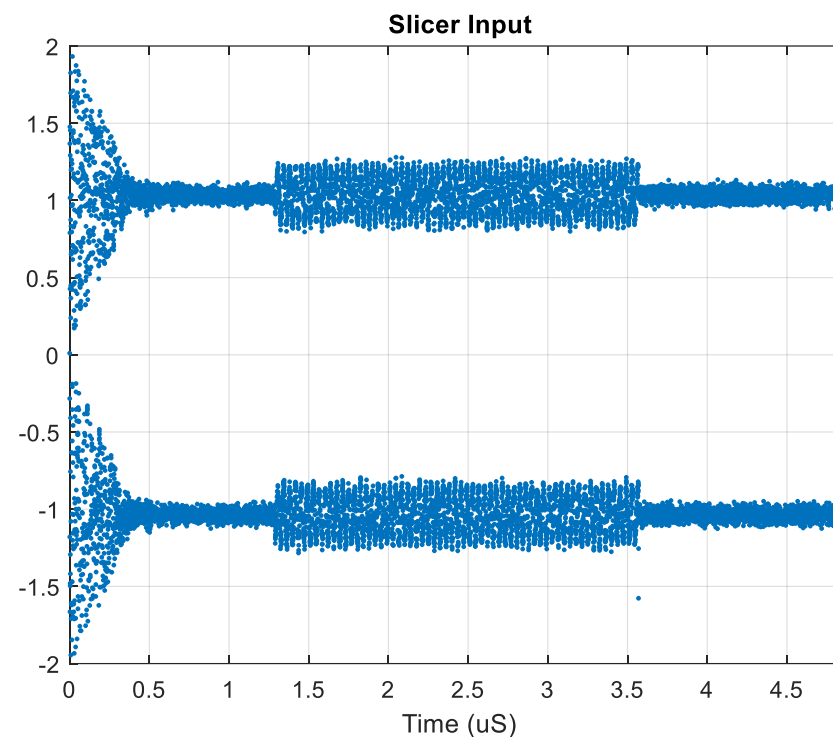


- The Link Segment is a concatenation of smaller cables: $3\text{m} + 0.6\text{m} + 3\text{m} + 0.6\text{m} + 3\text{m} + 0.6\text{m} + 3\text{m} + 0.6\text{m} + 3\text{m} = 17.4\text{m}$

Ingress noise effect, Link Segment of 10.2m



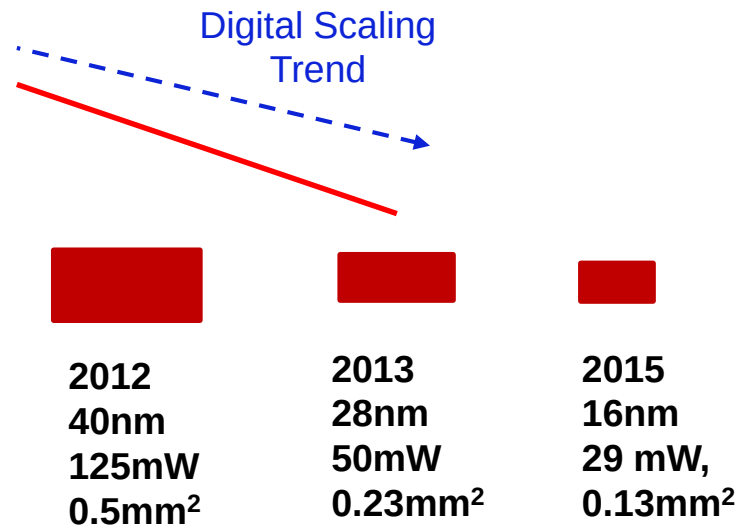
100mVpp Ingress noise at 425MHz



400mVpp Ingress noise at 27MHz

- CTLE or passive filter attenuates low frequency noises, therefore larger ingress noise levels are tolerated.

Receiver Area and Power Estimation



Reference: “Evolution of Multi-Gigabit Wireline Transceivers in CMOS”, Ichiro Fujimori, IEEE CSICS, 2014

- The plot shown on the left shows area and power for a 10Gbps SerDes transceiver evolution and it is referenced from CSICS 2014 paper.
- For 16nm technology, the numbers are estimated using digital scaling.
- The red line shows improved design practice beyond technology node size which could be used to build lower area and power transceivers even for larger technology nodes.
- Transceiver has three major blocks, TX, PLL and RX. RX side area and power is estimated to be about 50% of total area and power.
- For a 3Gsps receiver, only some portions of the receiver design is expected to scale down compared to a 10Gbps receiver. With that, the receiver power is expected to be below 10mW for a 16nm technology process and below 17mW for a 28nm technology. That is if it runs at 3Gsps continuously.
- For a TDD receiver with about 6% duty cycle, the power control mechanisms may be used to bring the average power to a level unmatched with any other technology (< 2-3mW with 16nm silicon and scales up for larger technology nodes).

Integration with Image Sensor

From Dr. Mario Heid, see the link below.
On requirements for Integration with Image sensors.

Parameter	Worst case	Improved
Tx location and shape	Corner block	Edge strip
Tx logic IP power	400mW	< 200mW 
Si thickness	150μm	> 200μm
Thermal design	w/o thermal via	w/ thermal via
Pixel ΔT	> 5°C	< 2°C

https://www.ieee802.org/3/ISAAC/public/091423/2023-09-18_Automotive%20camera%20PHY%20requirements%20study_V2.3.pdf

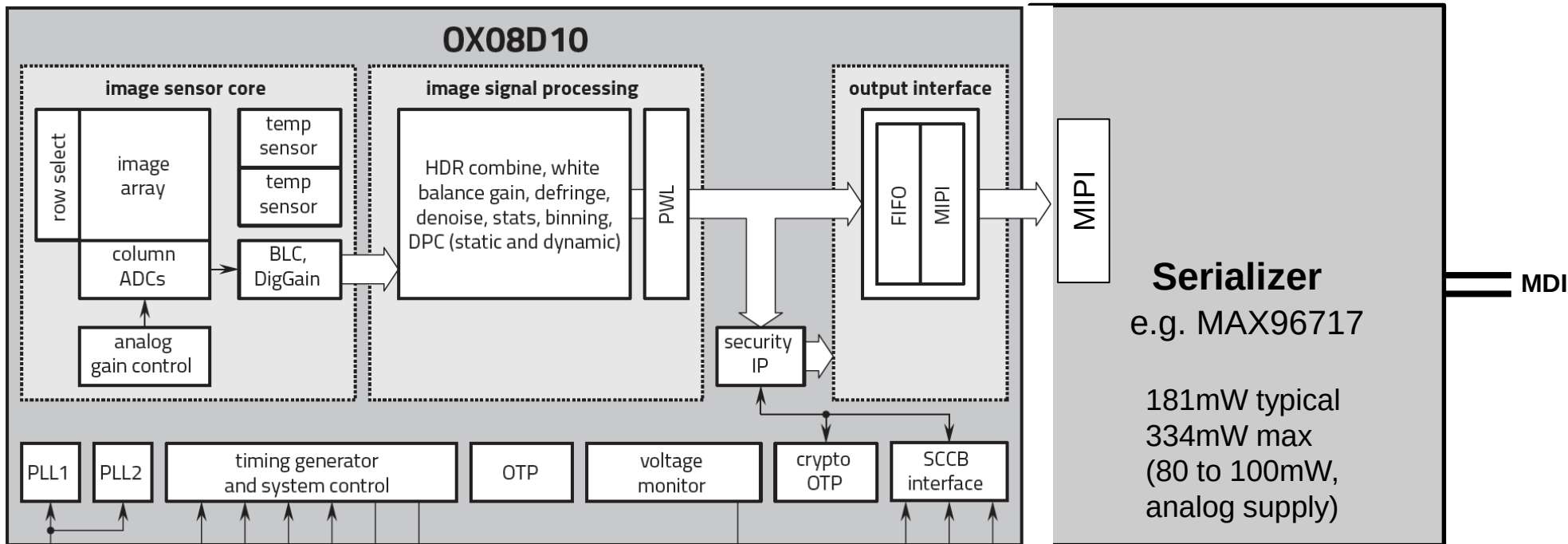
Estimated Power Consumption of TDD Transceiver

	3Gsps Receiver with TDD power control	3Gsps Receiver with no Power control	Transmitter and PLL
16nm	< 3 mW	< 10 mW	~15 mW
28nm	< 5.5 mW	< 17 mW	~26 mW
40nm	< 7.5mW	< 25 mW	~37.5 mW

- TDD-based camera transceiver meets the <200mW power requirements for <2C temperature change even for technology sizes larger than 16nm given TDD with very low power consumption in the receiver.
- Power levels estimated for 16nm technology and scaled up for 28nm and 40nm.

Camera side TDD-PHY versus Incumbents

880mW @45fps
742mW @36fps



<https://www.ovt.com/products/ox08d10/>

https://www.ieee802.org/3/dm/public/0724/Chini_Tazebay_3dm_01a_0724.pdf

- As a discrete serializer chip, TDD provides a competitive solution in cost and power by eliminating echo cancellation, small duty factor and low power PoC¹.

1- https://www.ieee802.org/3/dm/public/0924/Chini_Tazebay_3dm_01a_0924.pdf

Summary

- An architecture of a 3Gsp/s equalizer is discussed which could be implemented in mixed mode technology and there is no need for unrolling of the DFE taps.
- The simulated performance of the link is provided when using a short, a medium and a long cable. In all cases, the decision point SNR of 30dB or more is achieved using low cost filtering techniques.
- The same receiver architecture may be used on both sides of a link operating at 2.5Gbps/100Mbps.
- The area and power of a 3Gsp/s SerDes transceiver and in particular, the camera side receiver is discussed. TDD-based PHY provides for extremely low power receiver design:
 - Very competitive with incumbent discrete solutions.
 - Well-suited for integration into image sensors.

Thank you for your attention

Questions?